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April 1st, 2010
Renesas Electronics Corporation

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M16C/80 Group

Operation of Serial I/O (reception in UART mode)

1.0 Abstract

In receiving data in UART mode, choose functions from those listed in Table 1. Operations of the circled items are described below.

Table 1. Chosen functions

Item	Set-up	Item	Set-up
Transfer clock source (Note 2)	<input type="radio"/> Internal clock (f ₁ / f ₈ / f ₃₂)	Data logic select function (Note 3)	<input type="radio"/> No reverse
	<input type="radio"/> External clock (CLKi pin)		<input type="radio"/> Reverse
RTS function	<input type="radio"/> $\overline{\text{RTS}}$ function enabled	Tx/D, Rx/D I/O polarity reverse bit (Note 3)	<input type="radio"/> No reverse
	<input type="radio"/> $\overline{\text{RTS}}$ function disabled		<input type="radio"/> Reverse
CTS / $\overline{\text{RTS}}$ separation function (Note 1)	<input type="radio"/> Pin shared by CTS and $\overline{\text{RTS}}$	Bus collision detection function (Note 3)	<input type="radio"/> Not selected
	<input type="radio"/> CTS and $\overline{\text{RTS}}$ separate		<input type="radio"/> Selected
Sleep mode (Note 2)	<input type="radio"/> Sleep mode off		
	<input type="radio"/> Sleep mode selected		

Note 1: UART0 only. (UART1 CTS/RTS function cannot be used when this function is selected.)

Note 2: UART0, UART1 only.

Note 3: UART2 to UART4 only.

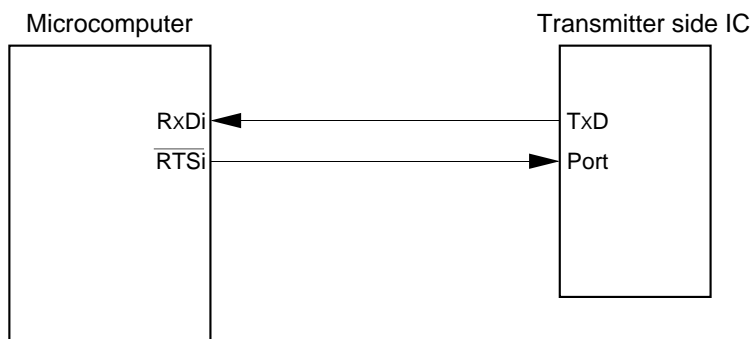
2.0 Introduction

- Operation
- (1) Setting the receive enable bit to "1" readies data-receivable status. At this time, output from the $\overline{\text{RTSi}}$ pin goes to "L" level to inform the transmission side that the receivable status is ready.
 - (2) When the first bit (the start bit) of reception data is received from the RxDi pin, output from the $\overline{\text{RTS}}$ goes to "H" level. Then, data is received, bit by bit, in sequence: LSB, ..., MSB, and stop bit(s).
 - (3) When the stop bit(s) is (are) received, the content of the UARTi receive register is transmitted to the UARTi receive buffer register.
At this time, the receive complete flag goes to "1" to indicate that the reception is completed, the UARTi receive interrupt request bit goes to "1", and output from the $\overline{\text{RTS}}$ pin goes to "L" level.
 - (4) The receive complete flag goes to "0" when the lower-order byte of the UARTi buffer register is read.

- Note
- Select $\overline{\text{RTSi}}$ outputs with the function select register A and B.
 - Set RxDi pin's function select register A to I/O port and port direction register to "0".
 - When setting the function select registers A, B, and C, sets the function select registers B and/or C first, and then sets the function select register A.

Figure 1 shows the operation timing

Example of wiring



Example of operation

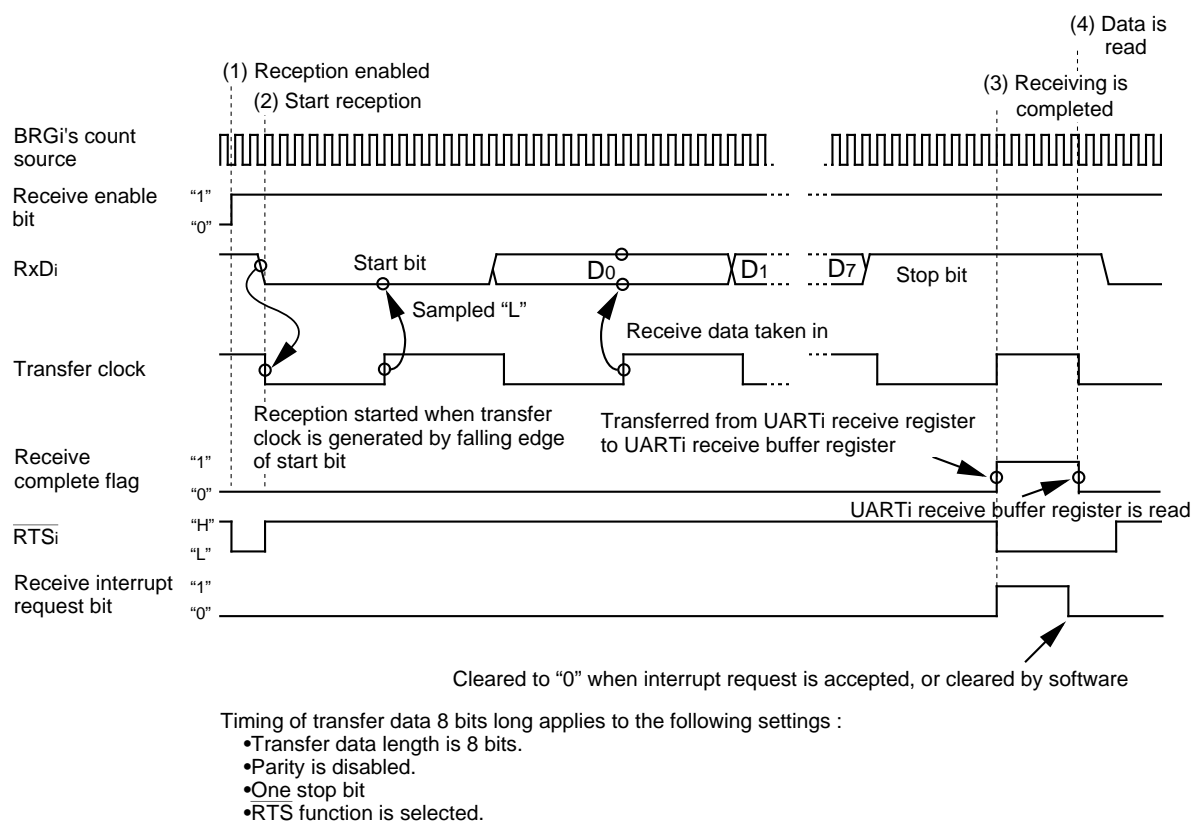
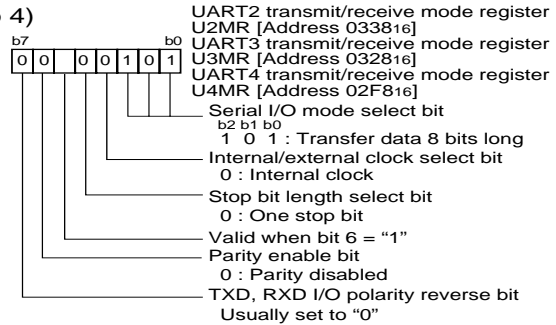
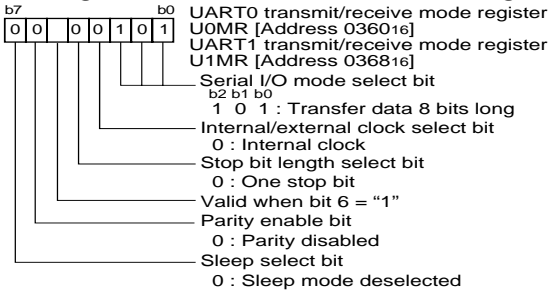


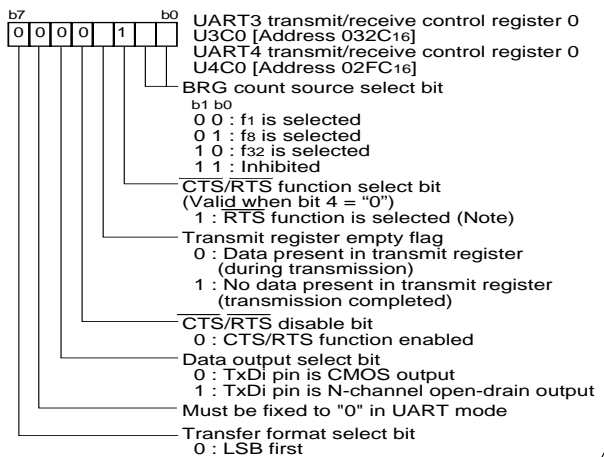
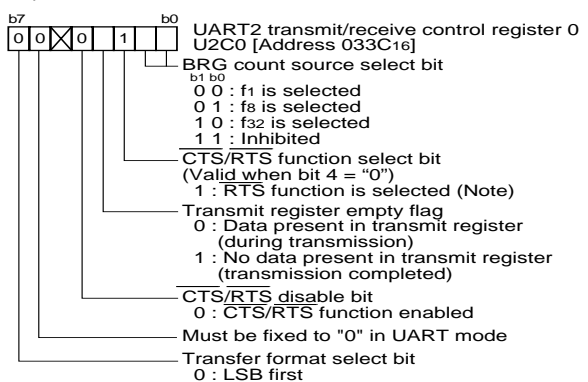
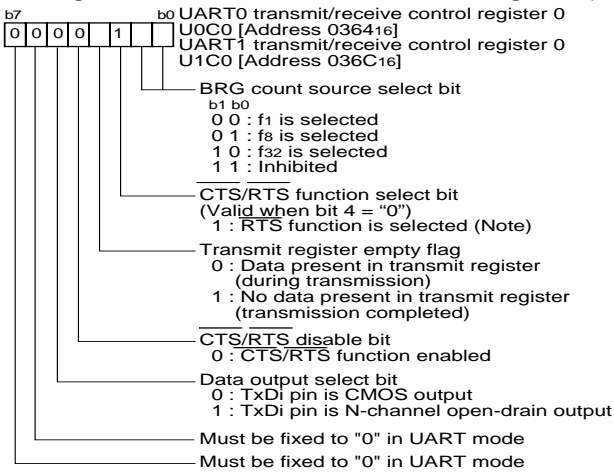
Figure 1. Operation timing of reception in UART mode

3.0 Set-up procedure

Setting UART_i transmit/receive mode register (i=0 to 4)

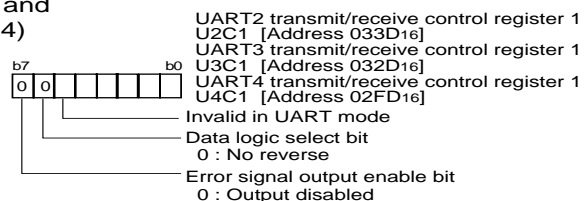
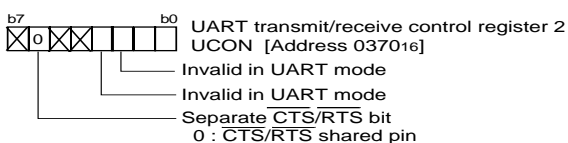


Setting UART_i transmit/receive control register (i=0 to 4)



Note: Select $\overline{\text{RTS}}$ output with the corresponding function select registers A and B.

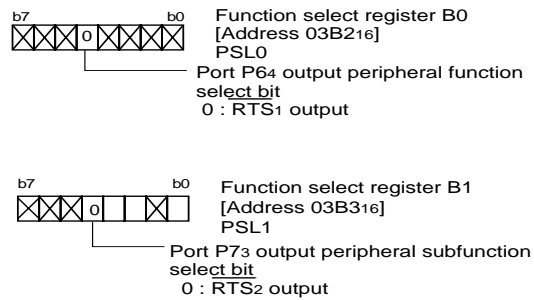
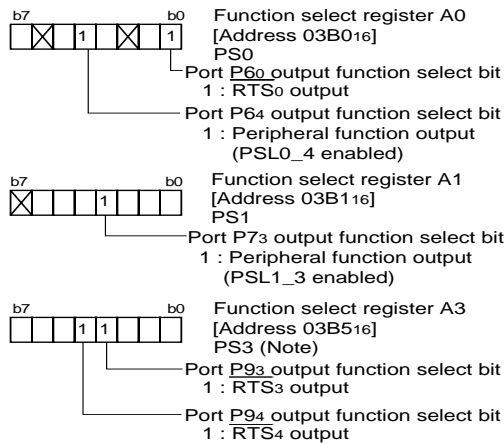
Setting UART transmit/receive control register 2 and UART_i transmit/receive control register 1 (i=2 to 4)



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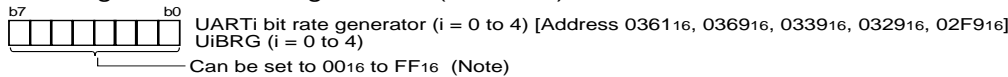
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Setting function select register



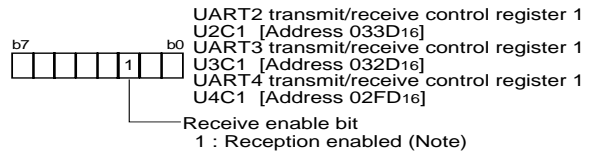
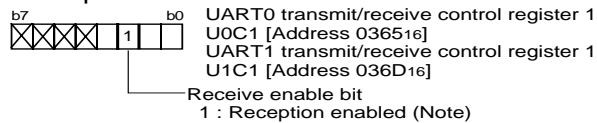
Note: Set bit 2 of the protect register (address 000A₁₆) to "1" when writing new value to this register.

Setting UARTi bit rate generator (i = 0 to 4)



Note: Write to UARTi bit rate generator when transmission/reception is halted.

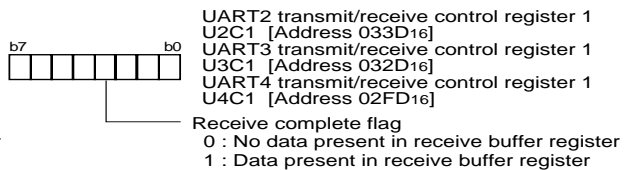
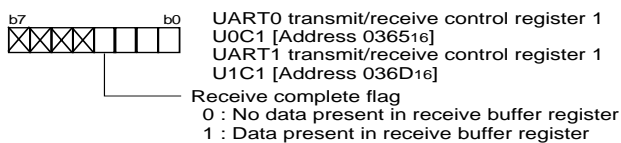
Reception enabled



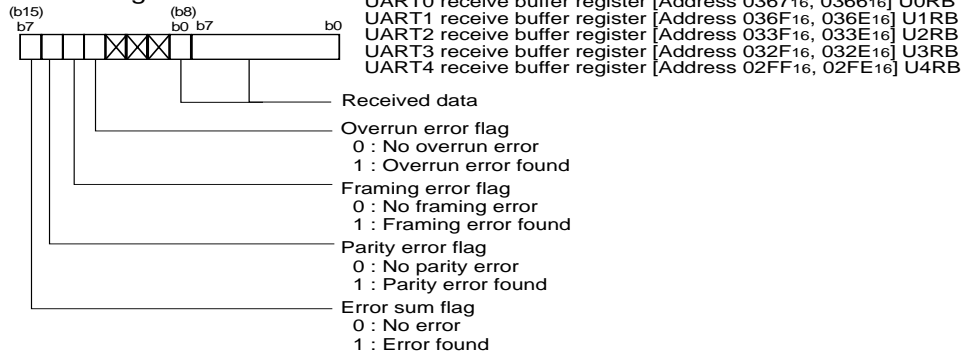
Note: Set the corresponding function select register A to I/O port and port direction register to "0".

Start reception

Checking completion of data reception



Checking error



Processing after reading out received data

4.0 Programming Code

```

;*****
;
;   M16C/80 Program Collection
;
;   FILE NAME : rjj05b0142_src.a30
;   CPU       : M16C/80 Group
;   FUNCTION  : Operation of Serial I/O
;               (reception in UART mode)
;   HISTORY   : 2004.02.16 Ver 1.00
;
;   Copyright(C)2003, Renesas Technology Corp.
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;
;*****
;*****
;   Include
;*****
;   .LIST      OFF          ;Stops outputting lines to the assembler list file
;   .INCLUDE   sfr80100.inc ;Reads the file that defined SFR
;   .LIST      ON           ;Starts outputting lines to the assembler list file
;
;*****
;   Symbol definition
;*****
ROM_TOP      .EQU    0FFC000H ;Start address of ROM
FIXED_VECT_TOP .EQU    0FFFFDCH ;Start address of fixed vector
;
;*****
;   Program area
;*****
;=====
;   Start up
;=====
;   .SECTION   PROGRAM, CODE ;Declares section name and section type
;   .ORG       ROM_TOP       ;Declares start address
RESET:
;   ; Sets Processor mode, System clock and Main clock division
MOV.B    #03H, prcr    ;Removes protect
MOV.B    #10000000B, pm0 ; Single-chip mode
MOV.B    #11000000B, pm1 ; Flash memory version
MOV.B    #00001000B, cm0 ; Xcin-Xcout High
MOV.B    #00100000B, cm1 ; Xin-Xout High
MOV.B    #00010010B, mcd ; No division mode
MOV.B    #00H, prcr     ;Protects all registers
;

```

```

=====
;      Serial I/O (reception in UART mode)
=====
;      Setting UART0 transmit/receive mode register
MOV.B   #00000101B, u0mr
;      ||| |++-----;Serial I/O mode select bit (101:Transfer data 8 bits long)
;      ||| |+-----;Internal/external clock select bit (0:Internal clock)
;      || |+-----;Stop bit length select bit (0:One stop bit)
;      ||+-----;Valid when bit 6="1"
;      |+-----;Parity enable bit (0:Parity disabled)
;      +-----;Sleep select bit (0:Sleep mode deselected)
;      Setting UART0 transmit/receive control register 0
MOV.B   #00001100B, u0c0
;      ||| |++-----;BRG count source select bit (00:f1 is selected)
;      ||| |+-----;RTS function is selected (Valid when bit 4="0") (Note)
;      || |+-----;Transmit register empty flag (Written value is invalid)
;      ||+-----;CTS/RTS disable bit (0:CTS/RTS function enabled)
;      |+-----;Data output select bit (0:TxDi pin is CMOS output)
;      +-----;Must be fixed to "0" in UART mode
;      Setting UART transmit/receive control register 2
MOV.B   #00000000B, ucon
;      ||| |++-----;Invalid in UART mode
;      || |+-----;Nothing is assigned
;      |+-----;Separate CTS/RTS bit (0:CTS/RTS shared pin)
;      +-----;Nothing is assigned
;      Setting function select register
;      (Note) Select RTS output with the corresponding function select register A and B
BSET    ps0_0          ;RTS0[P60] output
;      (Note) Set the corresponding function select register A to I/O port
;      and port direction register to "0"
BCLR    pd6_2          ;RxD0[P62] is input direction
;      Setting UART0 bit rate generator
MOV.B   #129, u0brg    ;(Approx. 9600bps : fi/16(129+1) @20MHz,f1)
;      ;(Note) Write to UARTi bit rate generator when
;      ;      transmission/reception is halted
;      Reception enabled
MOV.B   #00000100B, u0c1
;      +-----;Receive enable bit (1:Reception enabled) (Note)
;
=====
;      Main program
=====
WAIT_RECEIVE:
;      Checking completion of data reception
BTST    ri_u0c1
JNC     WAIT_RECEIVE
;
CHK_ERR:
;      Reading out error information and received data to R0 register
;      (ex)
MOV.W   u0rb, R0
;      Check error (ex. Check error sum flag)
BTST    7, R0H
JC      ERR_REC
;
;      No error
;      Processing after reading out reception data
JMP     WAIT_RECEIVE

=====
;      Error found
=====
ERR_REC:
NOP
JMP     ERR_REC
;

```



```

=====
;      Dummy interrupt processing program
=====
dummy:
    REIT
;
;*****
;      Setting of fixed vector
;*****
    .SECTION    F_VECT, ROMDATA
    .ORG        FIXED_VECT_TOP
;
    .LWORD      dummy    ;Undefined instruction
    .LWORD      dummy    ;Overflow
    .LWORD      dummy    ;BRK instruction execution
    .LWORD      dummy    ;Address match
    .LWORD      dummy    ;
    .LWORD      dummy    ;Watchdog timer
    .LWORD      dummy    ;
    .LWORD      dummy    ;NMI
    .LWORD      RESET    ;Reset
;
    .END

```

5.0 Reference

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Data Sheet

M16C/80 group Rev. E3
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M16C/80 group Rev. B
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