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April 1st, 2010
Renesas Electronics Corporation

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M16C/80 Group

Operation of Serial I/O (reception in clock-synchronous serial I/O mode)

1.0 Abstract

In receiveing data in clock-synchronous serial I/O mode, choose functions from those listed in Table 1. Operations of the circled items are described below.

Table 1. Choosed functions

Item	Set-up		Item	Set-up	
Transfer clock source		Internal clock (f_1 / f_8 / f_{32})	Continuous receive mode	O	Disabled
	O	External clock (CLKi pin)			Enabled
$\overline{RTS}$ function	O	$\overline{RTS}$ function enabled	Output transfer clock to multiple pins (Note 1)	O	Not selected
		$\overline{RTS}$ function disabled			Selected
CLK polarity	O	Input reception data at the rising edge of the transfer clock	$\overline{CTS}$ / $\overline{RTS}$ separation function (Note 2)	O	Pin shared by $\overline{CTS}$ and $\overline{RTS}$
					$\overline{CTS}$ and $\overline{RTS}$ separated
		Input reception data at the falling edge of the transfer clock	Data logic select function (Note 3)	O	No reverse
					Reverse
Transfer clock	O	LSB first	TxD, RxD I/O polarity reverse bit (Note 3)	O	No reverse
		MSB first			Reverse

Note 1: This can be selected only when UART1 is used in combination with the internal clock. When this function is selected, neither UART1 $\overline{CTS}$/$\overline{RTS}$ function, nor UART0 $\overline{CTS}$/$\overline{RTS}$ separation function can be utilized. Set the UART1 $\overline{CTS}$/$\overline{RTS}$ disable bit to “1”.

Note 2: UART0 only. (UART1 $\overline{CTS}$/$\overline{RTS}$ function cannot be used when this function is selected.)

Note 3: UART2 to 4only.

2.0 Introduction

Operation (1) Writing dummy data to the UARTi transmit buffer register, setting the receive enable bit to “1”, and the transmit enable bit to “1”, makes the data receivable status ready. At this time, the output from the $\overline{RTSi}$ pin goes to “L” level, which informs the transmission side that the data receivable status is ready (output the transfer clock from the IC on the transmission side after checking that the $\overline{RTS}$ output has gone to “L” level).

(2) In synchronization with the first rising edge of the transfer clock, the input signal to the RxDi pin is stored in the highest bit of the UARTi receive register. Then, data is taken in by shifting right the content of the UARTi reception data in synchronization with the rising edges of the transfer clock.

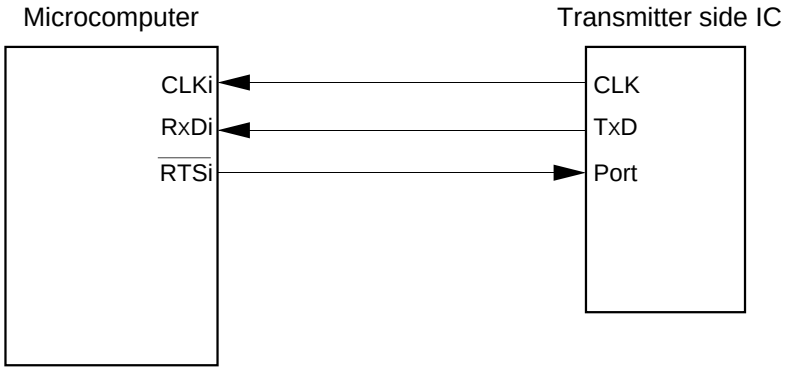
(3) When 1-byte data lines up in the UARTi receive register, the content of the UARTi receive register is transmitted to the UARTi receive buffer register. The transfer clock stops at “H” level. At this time, the receive complete flag and the UARTi receive interrupt request bit goes to “1”.

(4) The receive complete flag goes to “0” when the lower-order byte of the UARTi buffer register is read.

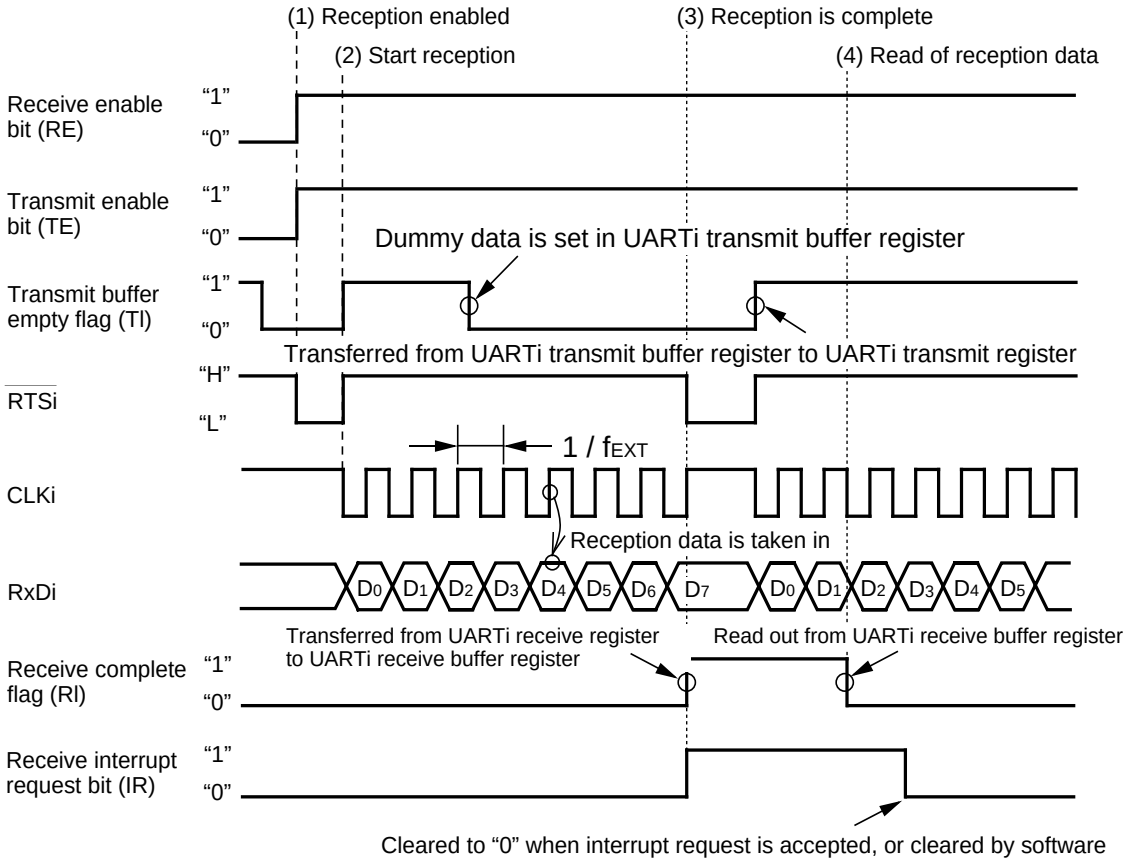
Note
- Select $\overline{RTSi}$ outputs with the function select register A and B.
- Set CLKi and RxDi pins' function select register A to I/O port and port direction register to “0”.
- When setting the function select registers A, B, and C, sets the function select registers B and/or C first, and then sets the function select register A.

Figure 1 shows the operation timing

Example of wiring



Example of operation



Shown in ( ) are bit symbols.

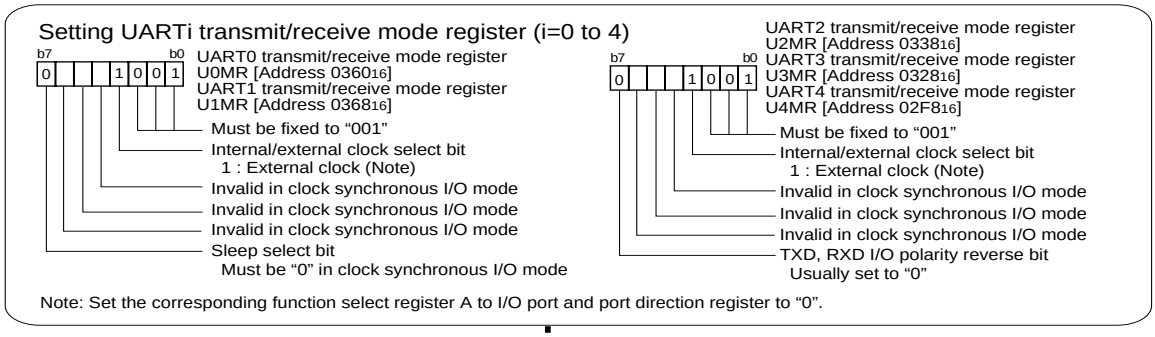
The above timing applies to the following settings:
- External clock is selected.
- $\overline{\text{RTS}}$ function is selected.
- CLK polarity select bit = "0".

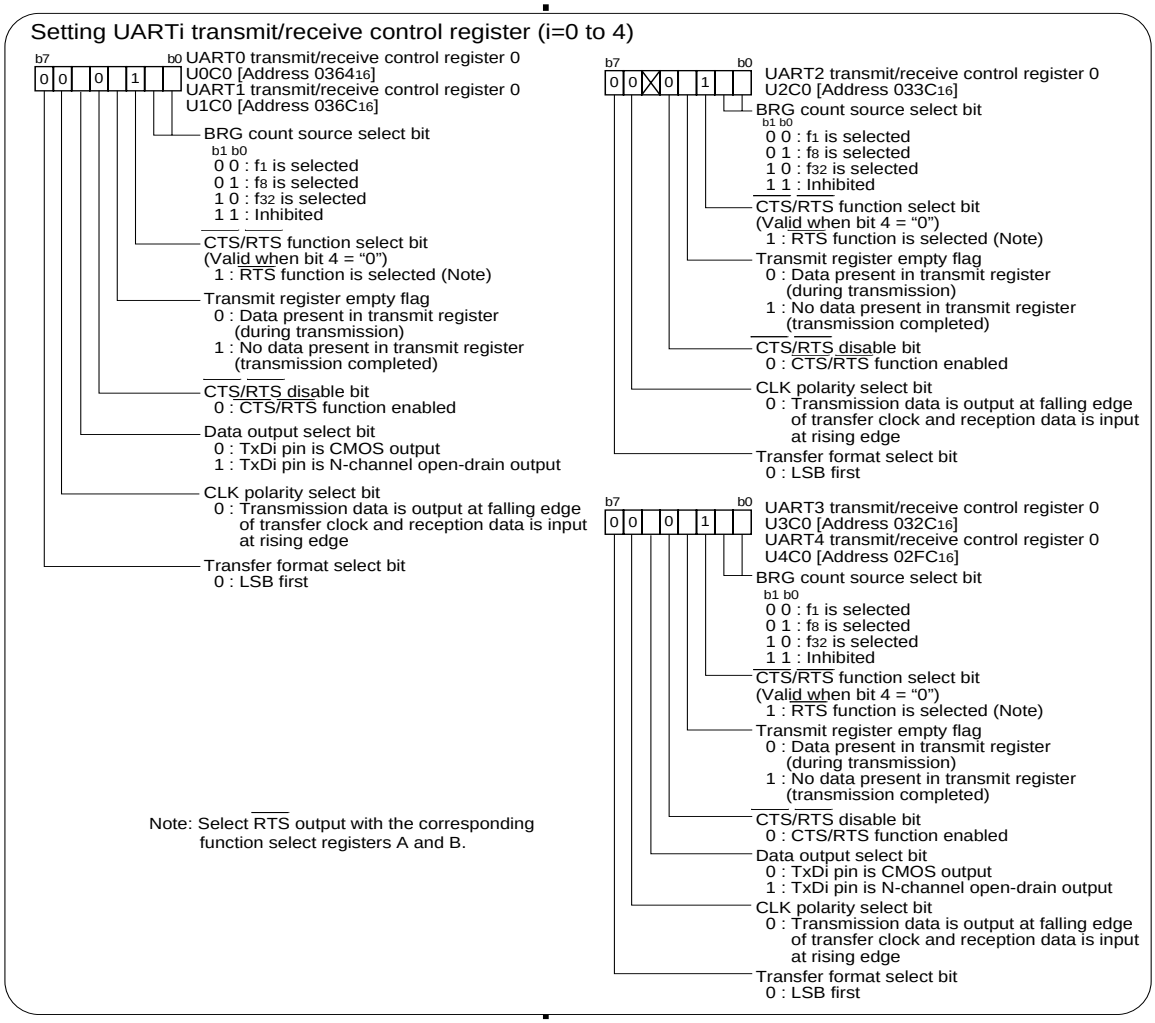
f_{EXT}: frequency of external clock

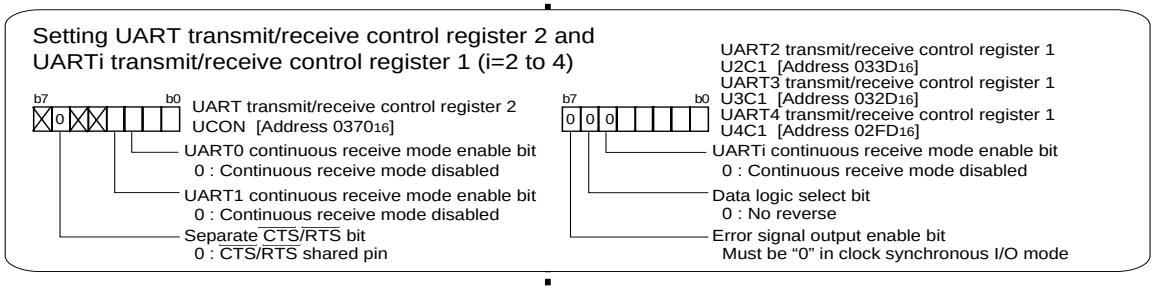
Make sure that the following conditions are met when the CLKi pin input ="H" before data reception
- Transmit enable bit → "1"
- Receive enable bit → "1"
- Dummy data write to UARTi transmit buffer register

Figure 1. Operation timing of reception in clock-synchronous serial I/O mode

3.0 Set-up procedure







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Setting function select register

Function select register A0 [Address 03B0$_{16}$]
PS0
Port P6$_0$ output function select bit
1 : RTS$_0$ output
Port P6$_4$ output function select bit
1 : Peripheral function output (PSL0_4 enabled)

Function select register A1 [Address 03B1$_{16}$]
PS1
Port P7$_3$ output function select bit
1 : Peripheral function output (PSL1_3 enabled)

Function select register A3 [Address 03B5$_{16}$]
PS3 (Note)
Port P9$_3$ output function select bit
1 : RTS$_3$ output
Port P9$_4$ output function select bit
1 : RTS$_4$ output

Function select register B0 [Address 03B2$_{16}$]
PSL0
Port P6$_4$ output peripheral function select bit
0 : RTS$_1$ output

Function select register B1 [Address 03B3$_{16}$]
PSL1
Port P7$_3$ output peripheral subfunction select bit
0 : RTS$_2$ output

Note: Set bit 2 of the protect register (address 000A$_{16}$) to "1" when writing new value to this register.

Reception enabled

UART0 transmit/receive control register 1
U0C1 [Address 0365$_{16}$]
UART1 transmit/receive control register 1
U1C1 [Address 036D$_{16}$]
Transmit enable bit
1 : Transmission enabled
Receive enable bit
1 : Reception enabled (Note)

UART2 transmit/receive control register 1
U2C1 [Address 033D$_{16}$]
UART3 transmit/receive control register 1
U3C1 [Address 032D$_{16}$]
UART4 transmit/receive control register 1
U4C1 [Address 02FD$_{16}$]
Transmit enable bit
1 : Transmission enabled
Receive enable bit
1 : Reception enabled (Note)

Note: Set the corresponding function select register A to I/O port and port direction register to "0".

Writing dummy data

UART0 transmit buffer register [Address 0363$_{16}$, 0362$_{16}$] U0TB
UART1 transmit buffer register [Address 036B$_{16}$, 036A$_{16}$] U1TB
UART2 transmit buffer register [Address 033B$_{16}$, 033A$_{16}$] U2TB
UART3 transmit buffer register [Address 032B$_{16}$, 032A$_{16}$] U2TB
UART2 transmit buffer register [Address 02FB$_{16}$, 02FA$_{16}$] U2TB
Setting dummy data

Start reception

Checking completion of data reception

UART0 transmit/receive control register 1
U0C1 [Address 0365$_{16}$]
UART1 transmit/receive control register 1
U1C1 [Address 036D$_{16}$]
Receive complete flag
0 : No data present in receive buffer register
1 : Data present in receive buffer register

UART2 transmit/receive control register 1
U2C1 [Address 033D$_{16}$]
UART3 transmit/receive control register 1
U3C1 [Address 032D$_{16}$]
UART4 transmit/receive control register 1
U4C1 [Address 02FD$_{16}$]
Receive complete flag
0 : No data present in receive buffer register
1 : Data present in receive buffer register

Checking error

UART0 receive buffer register [Address 0367$_{16}$, 0366$_{16}$] U0RB
UART1 receive buffer register [Address 036F$_{16}$, 036E$_{16}$] U1RB
UART2 receive buffer register [Address 033F$_{16}$, 033E$_{16}$] U2RB
UART3 receive buffer register [Address 032F16, 032E$_{16}$] U3RB
UART4 receive buffer register [Address 02FF$_{16}$, 02FE$_{16}$] U4RB
Received data
Overrun error flag
0 : No overrun error
1 : Overrun error found

Processing after reading out received data

4.0 Programming Code

```
;***********************************************************************************
;
;   M16C/80 Program Collection
;
;   FILE NAME : rjj05b0140_src.a30
;   CPU       : M16C/80 Group
;   FUNCTION  : Operation of Serial I/O
;               (reception in clock-synchronous serial I/O mode)
;   HISTORY   : 2004.02.16  Ver 1.00
;
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;
;***********************************************************************************
;***********************************************************************************
;       Include
;***********************************************************************************
        .LIST       OFF             ;Stops outputting lines to the assembler list file
        .INCLUDE    sfr80100.inc    ;Reads the file that defined SFR
        .LIST       ON              ;Starts outputting lines to the assembler list file
;***********************************************************************************
;       Symbol definition
;***********************************************************************************
ROM_TOP         .EQU    0FFC000H    ;Start address of ROM
FIXED_VECT_TOP  .EQU    0FFFFDCH    ;Start address of fixed vector
C_DUMMY_DATA    .EQU    0AAh
;***********************************************************************************
;       Program area
;***********************************************************************************
;=================================================================================
;       Start up
;=================================================================================
        .SECTION    PROGRAM, CODE  ;Declares section name and section type
        .ORG        ROM_TOP        ;Declares start address
RESET:
        ; Sets Processor mode, System clock and Main clock division
        MOV.B    #03H, prcr        ;Removes protect
        MOV.B    #10000000B, pm0   ; Single-chip mode
        MOV.B    #11000000B, pm1   ; Flash memory version
        MOV.B    #00001000B, cm0   ; Xcin-Xcout High
        MOV.B    #00100000B, cm1   ; Xin-Xout High
        MOV.B    #00010010B, mcd   ; No division mode
        MOV.B    #00H, prcr        ;Protects all registers
;
```

```
;=============================================================================
;       Serial I/O (reception in clock-synchronous serial I/O mode)
;=============================================================================
        ; Setting UART0 transmit/receive mode register
        MOV.B    #00001001B, u0mr
;                 |||||+++---------;Must be fixed to "001"
;                 ||||+------------;Internal/external clock select bit (1:External clock) (Note)
;                 |+++-------------;Invalid in clock synchronous I/O mode
;                 +----------------;Sleep select bit
;                                   (Must always be "0" in clock synchronous I/O mode)
        ; (Note) Set the corresponding function select register A to I/O port
        ; and port direction register to "0"
        BCLR     pd6_1             ;Port P61 is input direction
        BCLR     ps0_1             ;CLK0[P61] is I/O port
        ; Setting UART0 transmit/receive control register 0
        MOV.B    #00001100B, u0c0
;                 ||||||++---------;BRG count source select bit (00:f1 is selected)
;                 |||||+-----------;RTS function selected (Valid when bit 4="0") (Note)
;                 ||||+------------;Transmit register empty flag (Written value is invalid)
;                 |||+-------------;CTS/RTS disable bit (0:CTS/RTS function enabled)
;                 ||+--------------;Data output select bit (0:TxDi pin is CMOS output)
;                 |+---------------;CLK polarity select bit
;                 |                 (0:Transmission data is output at falling edge of
;                 |                  transfer clock and
;                 |                  reception data is input at rising edge)
;                 +----------------;Transfer format select bit (0:LSB first)
        ; Setting UART transmit/receive control register 2
        MOV.B    #00000000B, ucon
;                 |||||+-----------;UART0 continuous receive mode disabled
;                 ||||+------------;UART1 continuous receive mode disabled
;                 ||++-------------;Nothing is assigned (When write, set "0")
;                 |+---------------;Separate CTS/RTS bit (0:CTS/RTS shared pin)
;                 +----------------;Nothing is assigned (When write, set "0")
        ; Setting function select register
        ; (Note) Select RTS output with the corresponding function select register A and B
        BSET     ps0_0             ;Port P60 output function select bit (1:RTS0 output)
        ; Reception enabled
        MOV.B    #00000101B, u0c1
;                      | +---------;Transmission enabled
;                      +-----------;Reception enabled
;
;=============================================================================
;       Main program
;=============================================================================
WRITE_DUMMY:
        ; Writing dummy data to generate a shift clock
        MOV.B    #C_DUMMY_DATA, u0tbl
        ; Start reception
;
WAIT_RECEIVE:
        ; Checking completion of reception
        BTST     ri_u0c1
        JNC      WAIT_RECEIVE
;
CHK_ERR:
        ; Reading out error information and received data to R0 register
        ; (ex)
        MOV.W    u0rb, R0
        ; Check overrun error
        BTST     4, R0H
        JNZ      ERR_REC
;
        ; No overrun error
        ; Processing after reading out reception data
        JMP      WRITE_DUMMY
;
```

```
;=======================================================================
;       Error found
;=======================================================================
ERR_REC:
        NOP
        JMP      ERR_REC
;
;=======================================================================
;       Dummy interrupt processing program
;=======================================================================
dummy:
        REIT
;
;***************************************************************************************
;       Setting of fixed vector
;***************************************************************************************
        .SECTION    F_VECT, ROMDATA
        .ORG        FIXED_VECT_TOP
;
        .LWORD    dummy    ;Undefined instruction
        .LWORD    dummy    ;Overflow
        .LWORD    dummy    ;BRK instruction execution
        .LWORD    dummy    ;Address match
        .LWORD    dummy    ;
        .LWORD    dummy    ;Watchdog timer
        .LWORD    dummy    ;
        .LWORD    dummy    ;NMI
        .LWORD    RESET    ;Reset
;
        .END
```

5.0 Reference

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Data Sheet

M16C/80 group Rev. E3
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