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April 1st, 2010
Renesas Electronics Corporation

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M16C/62A Group

Operation of Serial I/O (reception in clock-synchronous serial I/O mode)

1.0 Abstract

In receiving data in clock-synchronous serial I/O mode, choose functions from those listed in Table 1. Operations of the circled items are described below.

Table 1. Choosed functions

Item	Set-up		Item	Set-up	
Transfer clock source		Internal clock (f_1 / f_8 / f_{32})	Continuous receive mode	**O**	Disabled
	O	External clock (CLKi pin)			Enabled
$\overline{\text{RTS}}$ function	**O**	$\overline{\text{RTS}}$ function enabled	Output transfer clock to multiple pins (Note 1)	**O**	Not selected
		$\overline{\text{RTS}}$ function disabled			Selected
CLK polarity	**O**	Input reception data at the rising edge of the transfer clock	Data logic select function (Note 2)	**O**	No reverse
					Reverse
		Input reception data at the falling edge of the transfer clock	TxD, RxD I/O polarity reverse bit (Note 2)	**O**	No reverse
					Reverse
Transfer clock	**O**	LSB first			
		MSB first			

Note 1: This can be selected only when UART1 is used in combination with the internal clock. When this function is selected, UART1 $\overline{\text{CTS}}$/$\overline{\text{RTS}}$ function can not be utilized. Set the UART1 $\overline{\text{CTS}}$/$\overline{\text{RTS}}$ disable bit to "1".

Note 2: UART2 only.

2.0 Introduction

Operation (1) Writing dummy data to the UARTi transmit buffer register, setting the receive enable bit to "1", and the transmit enable bit to "1", makes the data receivable status ready. At this time, the output from the $\overline{\text{RTSi}}$ pin goes to "L" level, which informs the transmission side that the data receivable status is ready (output the transfer clock from the IC on the transmission side after checking that the $\overline{\text{RTS}}$ output has gone to "L" level).

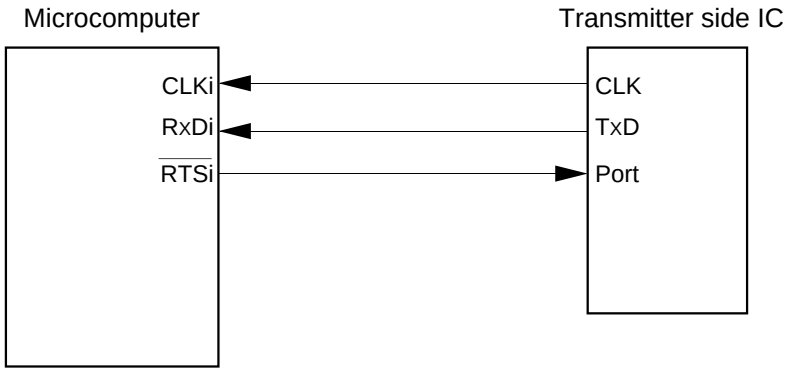
(2) In synchronization with the first rising edge of the transfer clock, the input signal to the RxDi pin is stored in the highest bit of the UARTi receive register. Then, data is taken in by shifting right the content of the UARTi reception data in synchronization with the rising edges of the transfer clock.

(3) When 1-byte data lines up in the UARTi receive register, the content of the UARTi receive register is transmitted to the UARTi receive buffer register. The transfer clock stops at "H" level. At this time, the receive complete flag and the UARTi receive interrupt request bit goes to "1".

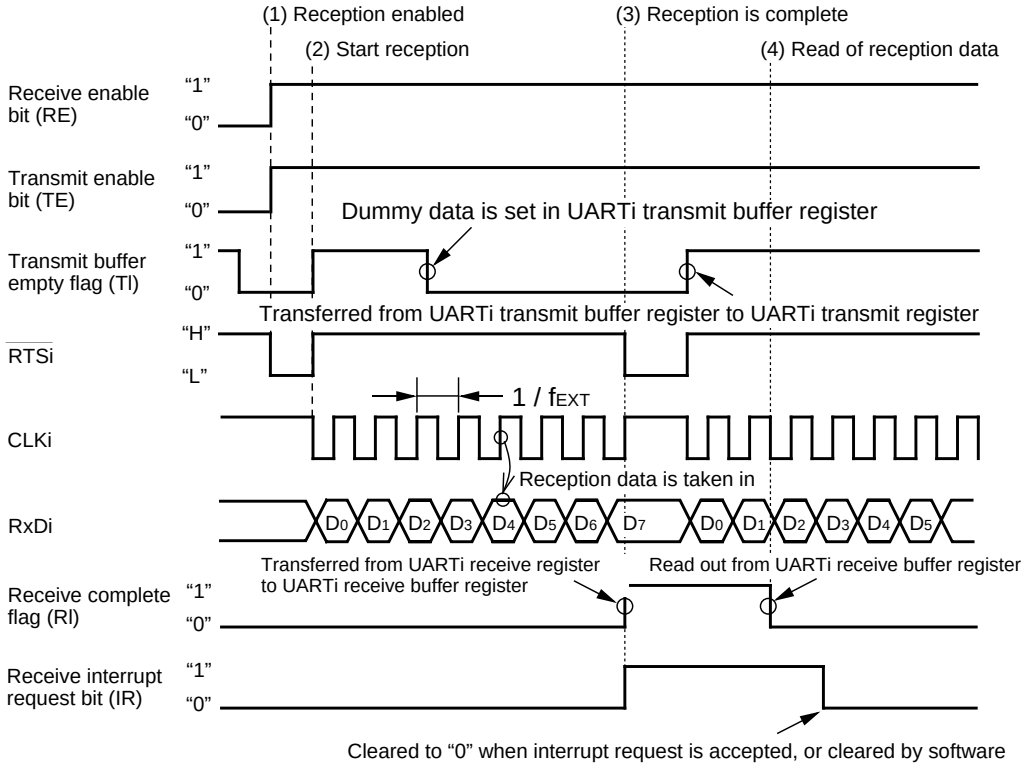
(4) The receive complete flag goes to "0" when the lower-order byte of the UARTi buffer register is read.

Figure 1 shows the operation timing

Example of wiring



Example of operation



Shown in ( ) are bit symbols.

The above timing applies to the following settings:
- External clock is selected.
- RTS function is selected.
- CLK polarity select bit = “0”.

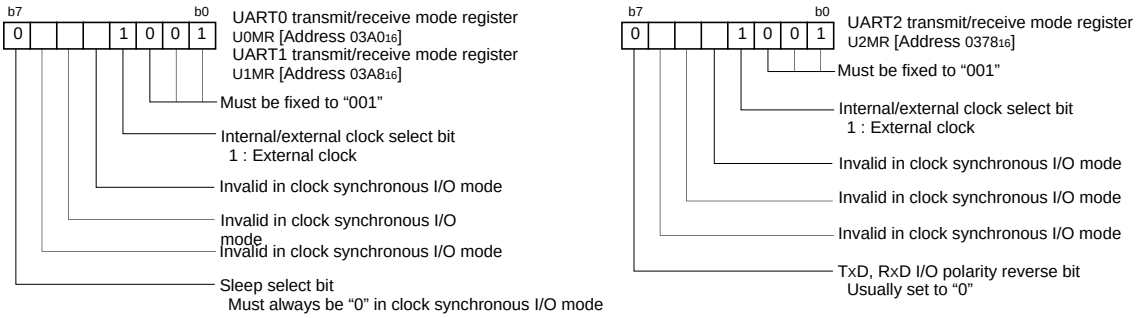
fEXT: frequency of external clock

Make sure that the following conditions are met when the CLKi pin input =“H” before data reception
- Transmit enable bit → “1”
- Receive enable bit → “1”
- Dummy data write to UARTi transmit buffer register

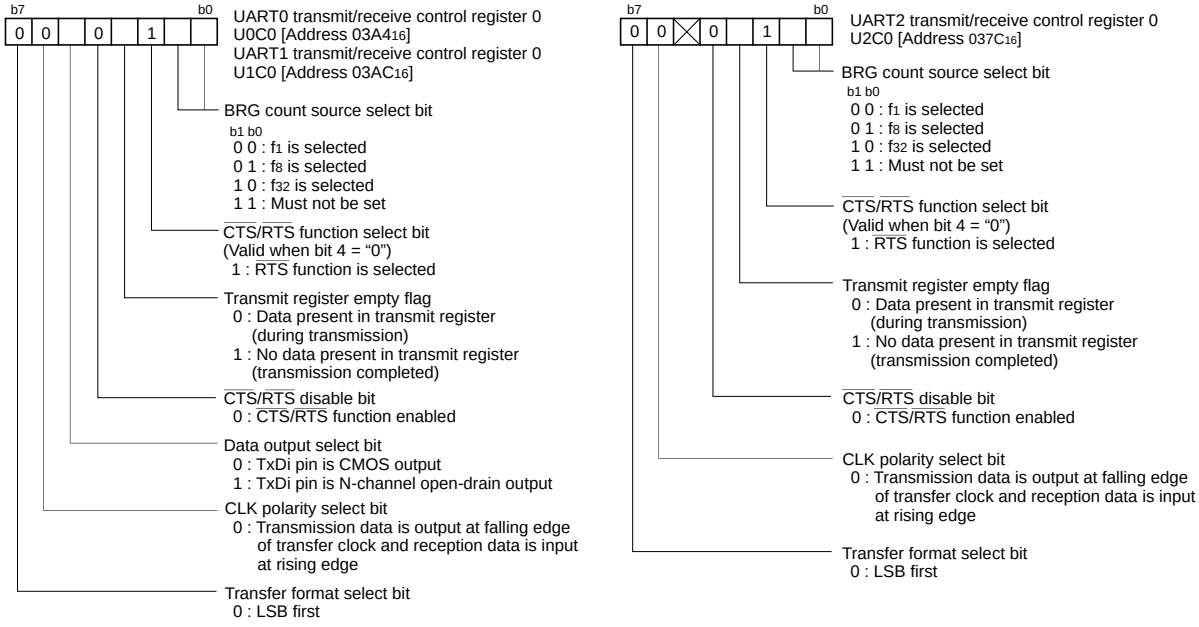
Figure 1. Operation timing of reception in clock-synchronous serial I/O mode

3.0 Set-up procedure

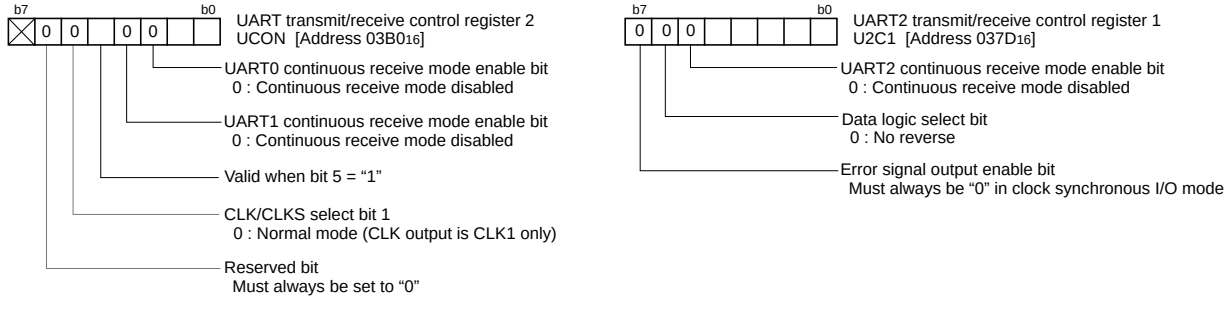
Setting UARTi transmit/receive mode register (i=0 to 2)



Setting UARTi transmit/receive control register 0 (i=0 to 2)



Setting UART transmit/receive control register 2 and UART2 transmit/receive control register 1



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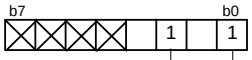
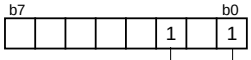
Reception enabled



UART0 transmit/receive control register 1 [Address 03A5$_{16}$] U0C1
UART1 transmit/receive control register 1 [Address 03AD$_{16}$] U1C1

Transmit enable bit
1 : Transmission enabled

Receive enable bit
1 : Reception enabled

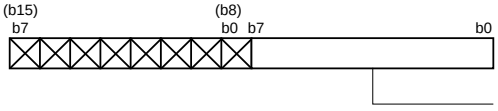


UART2 transmit/receive control register 1 [Address 037D$_{16}$] U2C1

Transmit enable bit
1 : Transmission enabled

Receive enable bit
1 : Reception enabled

Writing dummy data

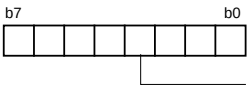


UART0 transmit buffer register [Address 03A3$_{16}$, 03A2$_{16}$] U0TB
UART1 transmit buffer register [Address 03AB$_{16}$, 03AA$_{16}$] U1TB
UART2 transmit buffer register [Address 037B$_{16}$, 037A$_{16}$] U2TB

Setting dummy data

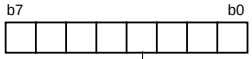
Start reception

Checking completion of reception



UART0 transmit/receive control register 1 [Address 03A5$_{16}$] U0C1
UART1 transmit/receive control register 1 [Address 03AD$_{16}$] U1C1

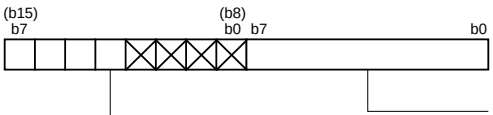
Receive complete flag
0 : No data present in receive buffer register
1 : Data present in receive buffer register



UART2 transmit/receive control register 1 [Address 037D$_{16}$] U2C1

Receive complete flag
0 : No data present in receive buffer register
1 : Data present in receive buffer register

Checking error



UART0 receive buffer register [Address 03A7$_{16}$, 03A6$_{16}$]U0RB
UART1 receive buffer register [Address 03AF$_{16}$, 03AE$_{16}$]U1RB
UART2 receive buffer register [Address 037F$_{16}$, 037E$_{16}$]U2RB

Receive data

Overrun error flag
0 : No overrun error
1 : Overrun error found

Processing after reading out reception data

4.0 Programming Code

```
;*****************************************************************************
;
;   M16C/62A Program Collection
;
;   FILE NAME : rjj05b0047_src.a30
;   CPU       : M16C/62A Group
;   FUNCTION  : Operation of Serial I/O
;               (reception in clock-synchronous serial I/O mode)
;   HISTORY   : 2003.05.16  Ver 1.00
;
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;
;*****************************************************************************
;*****************************************************************************
;       Include
;*****************************************************************************
        .LIST       OFF             ;Stops outputting lines to the assembler list file
        .INCLUDE    sfr62a.inc      ;Reads the file that defined SFR
        .LIST       ON              ;Starts outputting lines to the assembler list file
;
;*****************************************************************************
;       Symbol definition
;*****************************************************************************
ROM_TOP         .EQU    0F8000H     ;Start address of ROM
FIXED_VECT_TOP  .EQU    0FFFDCH     ;Start address of fixed vector
C_DUMMY_DATA    .EQU    0AAh
;
;*****************************************************************************
;       Program area
;*****************************************************************************
;=============================================================================
;       Start up
;=============================================================================
        .SECTION    PROGRAM, CODE  ;Declares section name and section type
        .ORG        ROM_TOP        ;Declares start address
RESET:
        MOV.B    #03H, prcr        ;Removes protect
                                   ;Set processor mode registers 0 and 1
        MOV.B    #00000000B, pm0   ; Single-chip mode
        MOV.B    #00000000B, pm1   ; No expansion, No wait
                                   ;Set system clock control registers 0 and 1
        MOV.B    #00001000B, cm0   ; Xcin-Xcout High
        MOV.B    #00100000B, cm1   ; Xin-Xout High, Main clock is No divison
        MOV.B    #00H, prcr        ;Protects all registers
;
```

```
;=============================================================================
;       Serial I/O (reception in clock-synchronous serial I/O mode)
;=============================================================================
        MOV.B    #00001001B, u0mr  ;Setting UART0 transmit/receive mode register
;                 |||||+++---------;Must be fixed to "001"
;                 ||||+------------;Internal/external clock select bit (1:External clock)
;                 |+++-------------;Invalid in clock synchronous I/O mode
;                 +----------------;Sleep select bit
;                                   (Must always be "0" in clock synchronous I/O mode)
        MOV.B    #00000100B, u0c0  ;Setting UART0 transmit/receive control register 0
;                 ||||||++---------;BRG count source select bit (00:f1 is selected)
;                 |||||+-----------;RTS function selected (Valid when bit 4="0")
;                 ||||+------------;Transmit register empty flag
;                 |||+-------------;CTS/RTS disable bit (0:CTS/RTS function enabled)
;                 ||+--------------;Data output select bit (0:TxDi pin is CMOS output)
;                 |+---------------;CLK polarity select bit
;                 |                 (0:Transmission data is output at falling edge of
;                 |                  transfer clock and
;                 |                  reception data is input at rising edge)
;                 +----------------;Transfer format select bit (0:LSB first)
        MOV.B    #00000000B, ucon  ;Setting UART transmit/receive control register 2
;                  ||||+-----------;UART0 continuous receive mode disabled
;                  |||+------------;UART1 continuous receive mode disabled
;                  ||+-------------;Valid when bit 5="1"
;                  |+--------------;CLK/CLKS select bit 1 (0:Normal mode;CLK output is CLK1 only)
;                  +---------------;Reserved bit (Must always be set to "0")
        MOV.B    #00000101B, u0c1  ;Reception enabled
;                       | +---------;Transmission enabled
;                       +-----------;Reception enabled
;
;=============================================================================
;       Main program
;=============================================================================
WRITE_DUMMY:
        MOV.B    #C_DUMMY_DATA, u0tbl  ;Writing dummy data to generate a shift clock
                                       ;Start reception
;
WAIT_RECEIVE:
        BTST     ri_u0c1               ;Checking completion of reception
        JNC      WAIT_RECEIVE
;
CHK_ERR:
        ; Reading out error information and received data to R0 register
        ; (ex)
        MOV.W    u0rb, R0
        ; Check overrun error
        BTST     12, R0
        JNZ      ERR_REC
;
        ; No overrun error
        ; Processing after reading out reception data
        JMP      WRITE_DUMMY
;
;=============================================================================
;       Error found
;=============================================================================
ERR_REC:
        NOP
        JMP      ERR_REC
;
```

```
;=============================================================================
;       Dummy interrupt processing program
;=============================================================================
dummy:
        REIT
;
;*******************************************************************************
;
;       Setting of fixed vector
;*******************************************************************************
;
        .SECTION    F_VECT, ROMDATA
        .ORG        FIXED_VECT_TOP
;
        .LWORD    dummy    ;Undefined instruction interrupt vector
        .LWORD    dummy    ;Overflow (INT0 instruction) interrupt vector
        .LWORD    dummy    ;BRK instruction interrupt vector
        .LWORD    dummy    ;Address match interrupt vector
        .LWORD    dummy    ;Single-step interrupt vector
        .LWORD    dummy    ;Watchdog timer interrupt vector
        .LWORD    dummy    ;DBC interrupt vector
        .LWORD    dummy    ;NMI interrupt vector
        .LWORD    RESET    ;Sets reset vector
;
        .END
```

5.0 Reference

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Data Sheet

M16C/62A group Rev. C.1
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