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April 1st, 2010
Renesas Electronics Corporation

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M16C/62P Group

Operation of Protect

1. Abstract

This application note describes the protect operation.

2. Introduction

The explanation of this issue is applied to the following condition:
Applicable MCU: M16C/62P Group

The program on this application note can also be used when operating other microcomputers within the M16C Family, provided they have the same SFR (Special Function Registers) as the M16C/62P Group. However, some functions may have been modified. Refer to each device's hardware manual for details. Use functions covered in this application note only after careful evaluation.

3. Operation of Protect

In the event that a program runs out of control, this function protects the important registers so that they will not be rewritten easily.
The following lists the registers protected by the PRC bit.

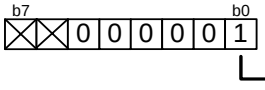
Protect Bit	Registers Protected by the PRC Bit
Protect Bit 0 (prc0)	System clock control register 0 (CM0)
	System clock control register 1 (CM1)
	Oscillation stop detection register (CM2)
	Peripheral clock select register (PCLKR)
	PLL control register 0 (PLC0)
Protect Bit 1 (prc1)	Processor mode register 0 (PM0)
	Processor mode register 1 (PM1)
	Processor mode register 2 (PM2)
	Timer B2 special mode register (TB2SC)
	Three phase PWM control register 0(INVC0)
	Three phase PWM control register 1(INVC1)
Protect Bit 2 (prc2)	Port P9 direction register 0 (PD9)
	SI/O3 control register (S3C)
	SI/O4 control register (S4C)
Protect Bit 3 (prc3)	Voltage detection register 2 (VCR2)
	Voltage down detection interrupt register (D4INT)

3.1 Register Setting

To enable the operation defined in “Section 3. Operation of Protect”, the following register settings must be taken place step by step. For detail configuration of each register, please refer to M16C/62P Group hardware manual.

3.1.1 Protect Bit 0

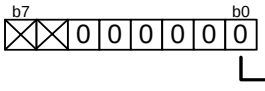
(1) Clearing the protect (set to write enabled state)



Protect Bit 0
1: Write enabled

(2) Alter the value of the register protected by protect bit 0.

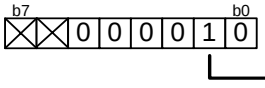
(3) Setting the protect (set to write protected state)



Protect Bit 0
0: Write protected

3.1.2 Protect Bit 1

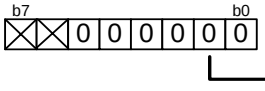
(1) Clearing the protect (set to write enabled state)



Protect Bit 1
1: Write enabled

(2) Alter the value of the register protected by protect bit 1.

(3) Setting the protect (set to write protected state)



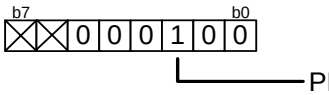
Protect Bit 1
0: Write protected

3.1.3 Protect Bit 2

When writing values to the specified address after setting the protect bit 2 to "1", the protect bit 2 is set to "0". Write instruction immediately after setting the protect bit 2 to "1" to change the registers protected by the protect bit 2. Do not generate any interrupt or DMA transfer between the instruction to set the protect bit 2 to "1" and the following instruction.

3.1.3.1 When an interrupt or a DMA transfer are not generated:

(1) Clearing the protect (set to write enabled state)

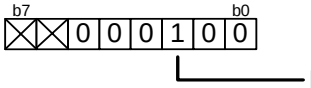


Protect Bit 2
1: Write enabled

(2) Alter the value of the register protected by protect bit 2.

3.1.3.2 When an interrupt or a DMA transfer are generated:

(1) Clearing the protect (set to write enabled state)



Protect Bit 2
1: Write enabled

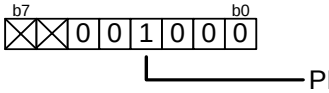
(2) Alter the value of the register protected by protect bit 2.

(3) Read the altered register value.

(4) If the value is not altered, return to (1).

3.1.4 Protect Bit 3

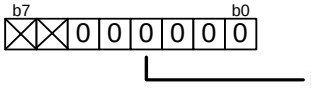
(1) Setting the protect (set to write protected state)



Protect Bit 3
1: Write enabled

(2) Alter the value of the register protected by protect bit 3.

(3) Setting the protect (set to write protected state)



Protect Bit 3
0: Write protected

4. Reference Program

Please find the reference program from the Renesas Technology Web site.
Click Application Note in the left menu of the M16C/60 Series top page.

5. Reference Documents

Hardware manual
M16C/62P Group (M16C/62P, M16C/62PT) Hardware Manual
(Use the most recent version of the document on the Renesas Technology Web site.)

Technical news/Technical update
(Use the most recent version of the document on the Renesas Technology Web site.)

6. Web site and Support

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REVISION HISTORY

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