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Renesas Electronics Corporation

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# M16C/62A Group

## Operation of A-D Converter (in repeat sweep mode 0)

### 1.0 Abstract

In repeat sweep 0 mode, choose functions from those listed in Table 1. Operations of the circled items are described below.

**Table 1. Choosed functions**

| Item | Set-up | | Item | Set-up | |
|---|---|---|---|---|---|
| Operation clock $f_{AD}$ | O | Divided-by-4 $f_{AD}$ / divided-by-2 $f_{AD}$ / $f_{AD}$ | Trigger for starting A-D conversion | O | Software trigger |
| | | | | | Trigger by $\overline{ADTRG}$ |
| Resolution | O | 8-bit / 10-bit | Expanded analog input pin | O | Not used |
| Analog input pin | O | $AN_0$ and $AN_1$ (2 pins) / $AN_0$ to $AN_3$ (4 pins) / $AN_0$ to $AN_5$ (6 pins) / $AN_0$ to $AN_7$ (8 pins) | | | External ope-amp connection mode |
| | | | Sample & Hold | | Not activated |
| | | | | O | Activated |

### 2.0 Introduction

Operation (1) Setting the A-D conversion start flag to “1” causes the A-D converter to start the conversion on voltage input to the $AN_0$ pin.

(2) After the A-D conversion of voltage input to the $AN_0$ pin is completed, the content of the successive comparison register (conversion result) is transmitted to A-D register 0.

(3) The A-D converter converts all pins selected by the user. The conversion result is transmitted to A-D register i corresponding to each pin every time A-D conversion on the pin is completed. The A-D conversion interrupt request bit does not go to “1”.

(4) The A-D converter continues operating until the A-D conversion start flag is set to “0” by software.

Figure 1 shows the operation timing

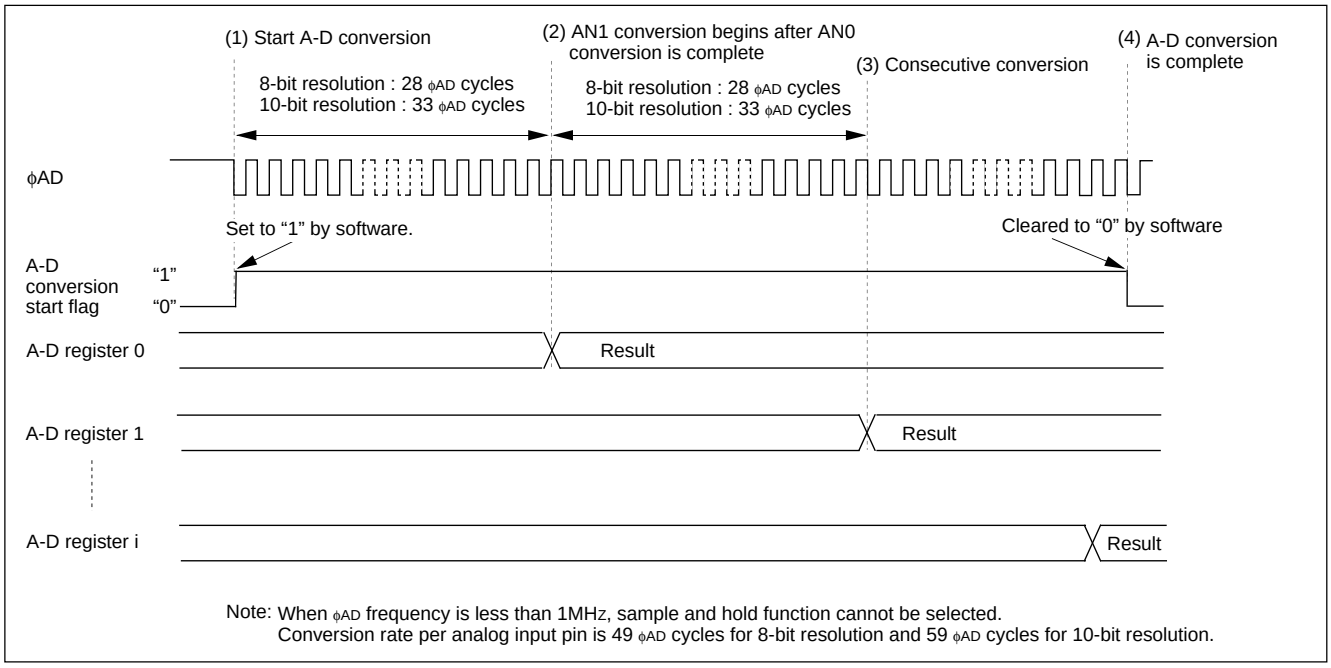
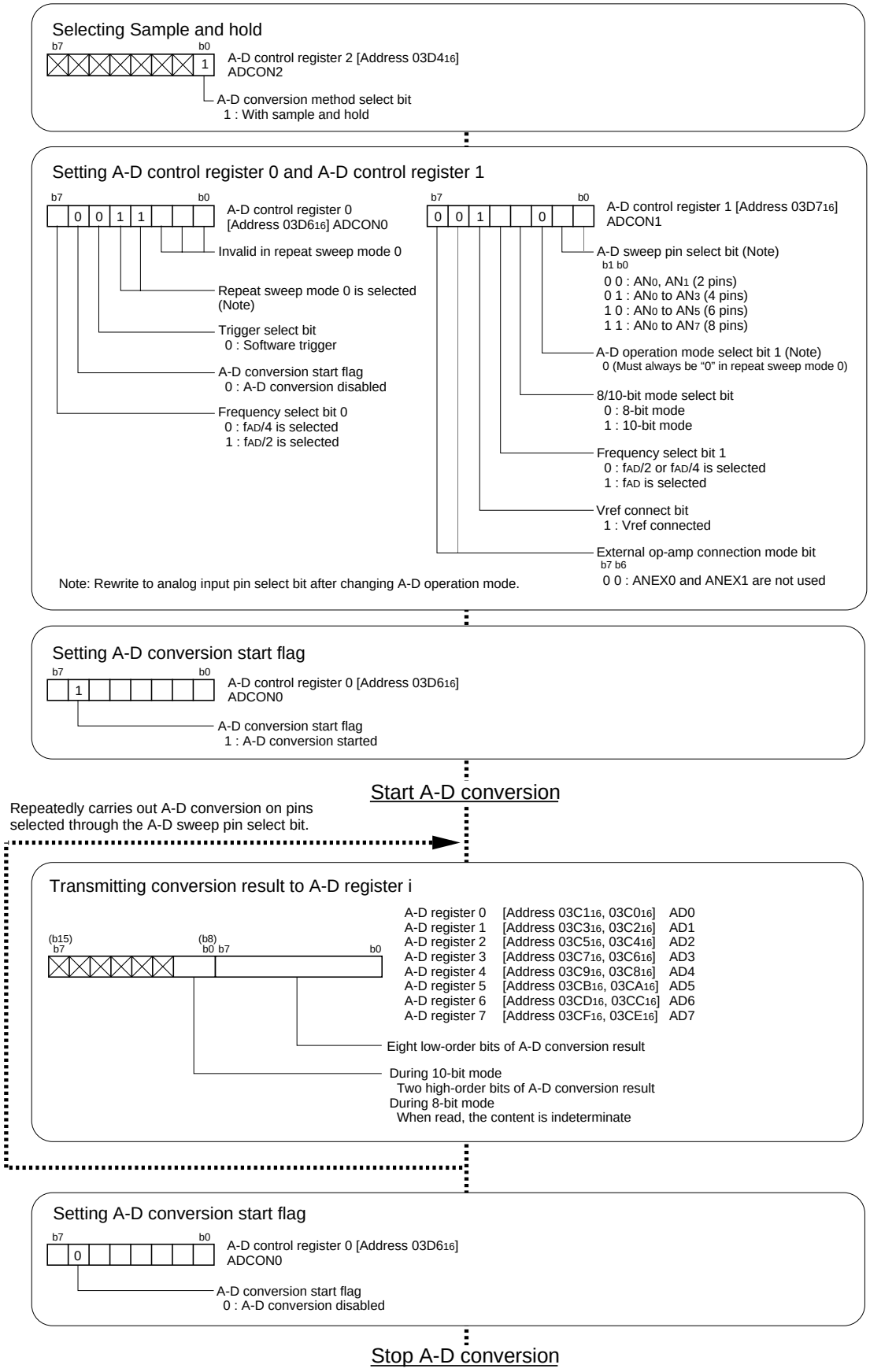



**Figure 1. Operation timing of repeat sweep 0**

## 3.0 Set-up procedure



## 4.0 Programming Code

```
;***************************************************************************************
;
;   M16C/62A Program Collection
;
;   FILE NAME : rjj05b0059_src.a30
;   CPU       : M16C/62A Group
;   FUNCTION  : Operation of A-D Converter
;               (in repeat sweep mode 0)
;   HISTORY   : 2003.05.16  Ver 1.00
;
;   Copyright(C)2003, Renesas Technology Corp.
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;
;***************************************************************************************
;***************************************************************************************
;       Include
;***************************************************************************************
        .LIST       OFF             ;Stops outputting lines to the assembler list file
        .INCLUDE    sfr62a.inc      ;Reads the file that defined SFR
        .LIST       ON              ;Starts outputting lines to the assembler list file
;
;***************************************************************************************
;       Symbol definition
;***************************************************************************************
ROM_TOP         .EQU    0F8000H     ;Start address of ROM
FIXED_VECT_TOP  .EQU    0FFFDCH     ;Start address of fixed vector
;
;
;***************************************************************************************
;       Program area
;***************************************************************************************
;=======================================================================
;       Start up
;=======================================================================
        .SECTION    PROGRAM, CODE  ;Declares section name and section type
        .ORG        ROM_TOP        ;Declares start address
RESET:
        MOV.B    #03H, prcr        ;Removes protect
                                   ;Set processor mode registers 0 and 1
        MOV.B    #00000000B, pm0   ; Single-chip mode
        MOV.B    #00000000B, pm1   ; No expansion, No wait
                                   ;Set system clock control registers 0 and 1
        MOV.B    #00001000B, cm0   ; Xcin-Xcout High
        MOV.B    #00100000B, cm1   ; Xin-Xout High, Main clock is No divison
        MOV.B    #00H, prcr        ;Protects all registers
;
```

```
;===============================================================================
;       A-D Converter (in repeat sweep mode 0)
;===============================================================================
        MOV.B    #00000001B, adcon2    ;Selecting Sample and hold
;                        +-------------;A-D conversion method select bit
;                                       (1:With sample and hold)
        MOV.B    #10011000B, adcon0    ;Setting A-D control register 0
;                 |||||+++-------------;Invalid in repeat sweep mode 0
;                 |||++----------------;Repeat sweep mode 0 is selected
;                 ||+------------------;Trigger select bit (0:Software trigger)
;                 |+-------------------;A-D conversion start flag (0:A-D conversion disabled)
;                 +--------------------;Frequency select bit 0 (1:fAD/2 is selected)
        MOV.B    #00101011B, adcon1    ;Setting A-D control register 1
;                 ||||||++-------------;A-D sweep pin select bit (11:AN0 to AN7 (8pins))
;                 |||||+--------------;Must always be "0" in repeat sweep mode
;                 ||||+---------------;8/10-bit mode select bit (1:10-bit mode)
;                 |||+----------------;Frequency select bit 1 (0:fAD/2 or fAD/4 is selected)
;                 ||+-----------------;Vref connect bit (1:Vref connected)
;                 ++-------------------;External op-amp connection mode bit
;                                      (00:ANEX0 and ANEX1 are not used)
        MOV.B    #00H, pd10            ;Set the direction register of the relevant port to input
                                       ;(AN0-AN7:Analog input pin)
;
;-------------------------------------------------------------------------------
;       Start A-D conversion
;-------------------------------------------------------------------------------
START_AD:
        BSET     adst                  ;Setting A-D conversion start flag
;
REPEAT_AD_CNV:
        ;
        ; Processing of reading A-D conversion result
        ; depending on the application program.
        ;
        JMP      REPEAT_AD_CNV
;
;-------------------------------------------------------------------------------
;       Stop A-D conversion
;-------------------------------------------------------------------------------
STOP_AD:
        BCLR     adst                  ; A-D conversion stop
;
STOPPED_AD:
        JMP      STOPPED_AD
;
```

```
;=======================================================================
;       Dummy interrupt processing program
;=======================================================================
dummy:
        REIT
;
;***************************************************************************************
;
;       Setting of fixed vector
;***************************************************************************************
;
        .SECTION    F_VECT, ROMDATA
        .ORG        FIXED_VECT_TOP
;
        .LWORD    dummy    ;Undefined instruction interrupt vector
        .LWORD    dummy    ;Overflow (INT0 instruction) interrupt vector
        .LWORD    dummy    ;BRK instruction interrupt vector
        .LWORD    dummy    ;Address match interrupt vector
        .LWORD    dummy    ;Single-step interrupt vector
        .LWORD    dummy    ;Watchdog timer interrupt vector
        .LWORD    dummy    ;DBC interrupt vector
        .LWORD    dummy    ;NMI interrupt vector
        .LWORD    RESET    ;Sets reset vector
;
        .END
```

## 5.0 Reference

**Renesas Technology Corporation Semiconductor Home page**

http://www.renesas.com/

**Technical Support**

E-mail: support_apl@renesas.com

**Data Sheet**

M16C/62A group Rev. C.1
(Use the latest version on the Home page: http://www.renesas.com/)

**User's Manual**

M16C/62A group Rev. 1.0
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