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April 1st, 2010
Renesas Electronics Corporation

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APPLICATION NOTE

Normal- and Inverse-Phase PWM Output of Three Signals with Independently Controllable Duty Cycles

Introduction

Applies the counter-reset synchronized PWM mode of the H8/3687's timer Z block to output the normal- and inverse-phase versions of three PWM waveforms that have the same period but individually controllable duty cycles.

Target Device

H8/300H Tiny Series H8/3687

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1. Specifications

1. Applies the counter-reset synchronized PWM mode of the H8/3687's timer Z block to output the normal- and inverse-phase versions of three PWM waveforms that have the same period but individually controllable duty cycles.
2. This sample task involves controlling the H8/3687 to produce outputs of the form shown in figure 1.1: that is, three PWM waveforms, each of which has a controllable duty cycle but the same period, with both normal- and inverse-phase versions of each waveform. The duty cycle is controlled through control of the high-level pulse width.
3. Any duty cycle from 0 to 100% is specifiable for each pair of normal- and inverse-phase signals by the settings in the relevant registers.

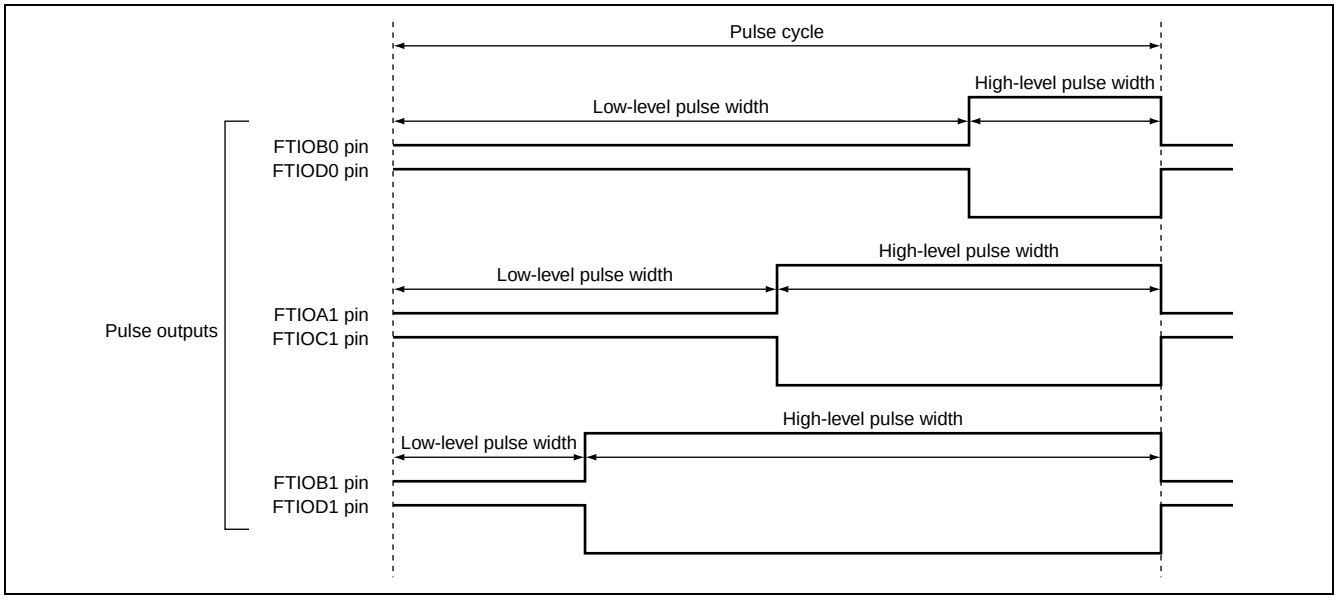


Figure 1.1 Output of Three Normal-Phase/Inverse-Phase Pairs with Independently Controllable Duty Cycles

2. Functional Descriptions

1. In this sample task, the H8/3687 is controlled to produce three PWM waveforms in both normal phase and inverted phase (for a total of six waveforms), with each having an independently controllable duty cycle. This is achieved through the combination of channels 0 and 1 of timer Z (counter-reset synchronized PWM mode).
   1) Figure 2.1 is a block diagram of timer Z, which is used in this sample task.
      In the sample task, the following functions of timer Z are used.

— Clearing of the counter in response to a compare-match (counter clearing).
— The output of paired normal- and inverse-phase PWM waveforms, where the levels of both waveforms in the pair change at the same point; this is achieved through the use in tandem of channels 0 and 1 of timer Z (counter-reset synchronized PWM mode).

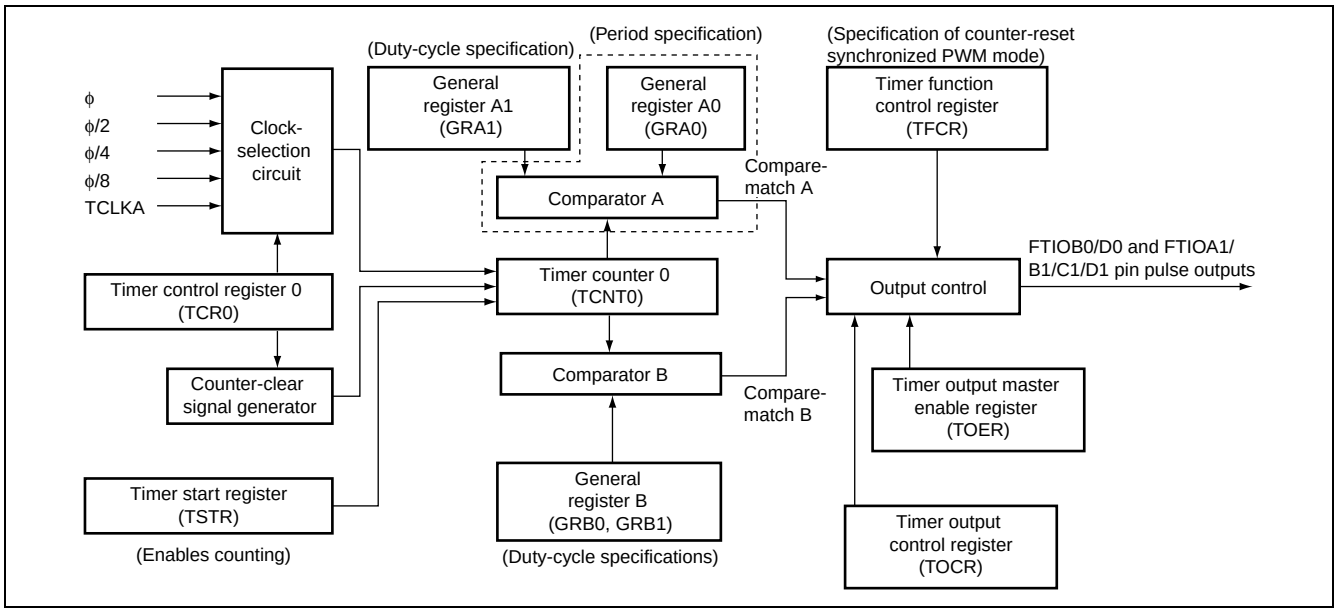


Figure 2.1 Timer Z Channels 0 and 1 in the Counter-Reset Synchronized PWM Mode

2. Table 2.1 shows the function assignments for this task. The three pairs of PWM waveforms are output by assigning the timer Z functions to the pins and registers indicated in table 2.1.

Table 2.1 Function Assignments

Pin or Register Name	Assigned Function
FTIOB0	Pulse-output pins
FTIOD0	
FTIOA1	
FTIOB1	
FTIOC1	
FTIOD1	
TSTR	Enabling and disabling of counting by the channel 0 and channel 1 timers.
TCR0	Selects the input clock and the condition that drives clearing of the channel 0 timer counter.
TFCR	Specifies the counter-reset synchronized PWM mode.
TOCR	Specifies the initial output until the first compare-match occurs.
TOER	Enables and disables the timer output.
GRA0	Specifies the output pulse cycle.
GRB0	Specifies the timing of the level change in the pulses to be output from the FTIOB0 and FTIOD0 pins
GRC0	Specifies the timing of the level change in the pulse to be output from the FTIOA1 and FTIOC1 pins.
GRD0	Specifies the timing of the level change in the pulse to be output from the FTIOB1and FTIOD1 pins.
TCNT0	Channel 0 timer counter

3. Description of Operation

Figure 3.1 shows the principle of operation. Hardware and software processing by the H8/3687 are applied in the way shown in figure 3.1 to produce three pairs of waveforms, each with the same period and an independently controlled duty cycle, and with each pair consisting of a normal-phase signal and the corresponding inverse-phase signal.

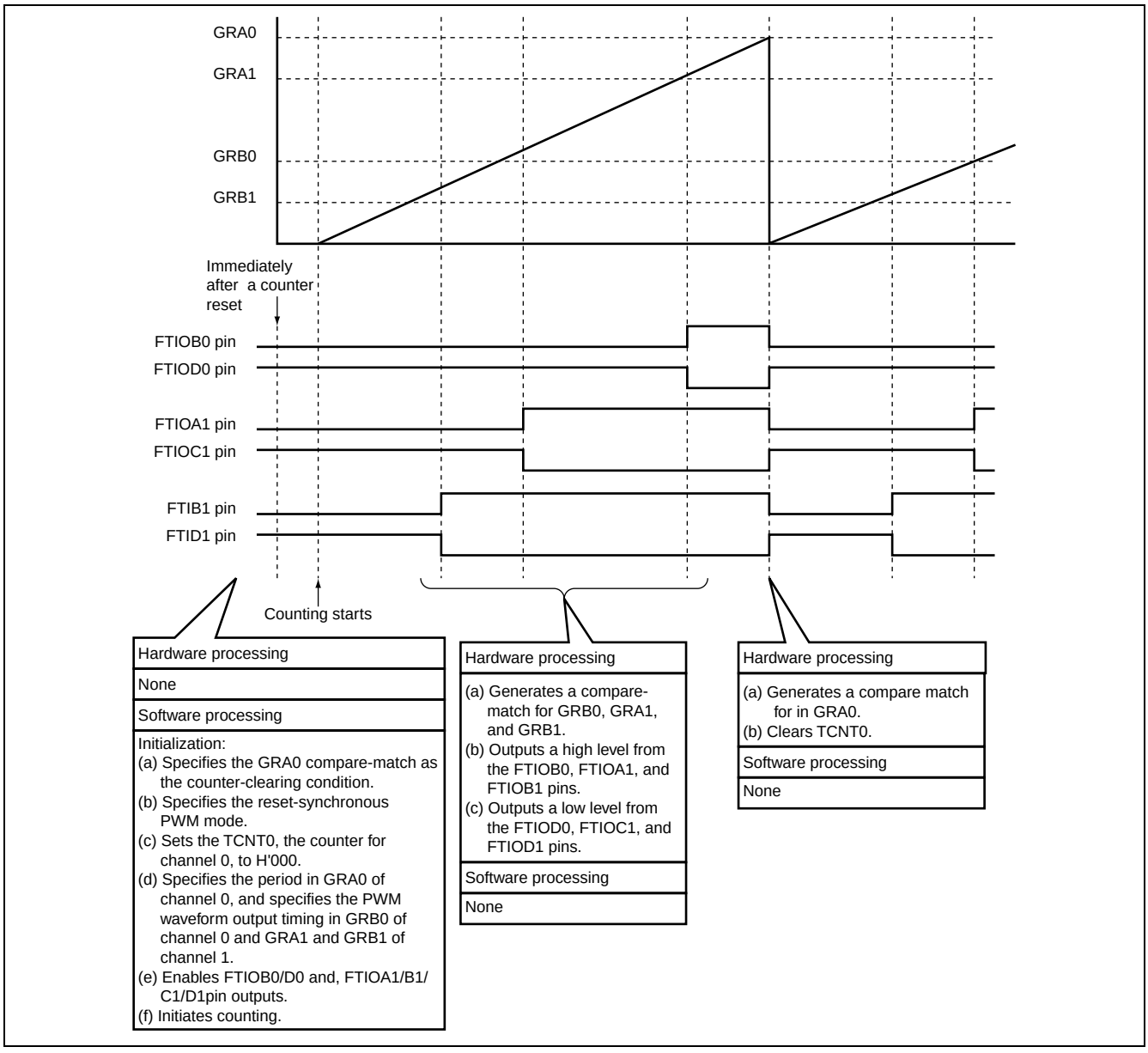


Figure 3.1 Principle of operation for the Output of Three Pairs (Normal/Inverse Phase) of Signals with Independently Controllable Duty Cycles

4. Software Description

4.1 Module

Module Name	Label Name	Assigned Function
Main routine	main	Specifies the timing of the level changes in the three pairs of output pulse waveforms in GRB0, GRC0, and GRD0 and specifies the period for the waveforms in GRA0.

4.2 Arguments

No argument is used in this sample task.

4.3 Internal registers used

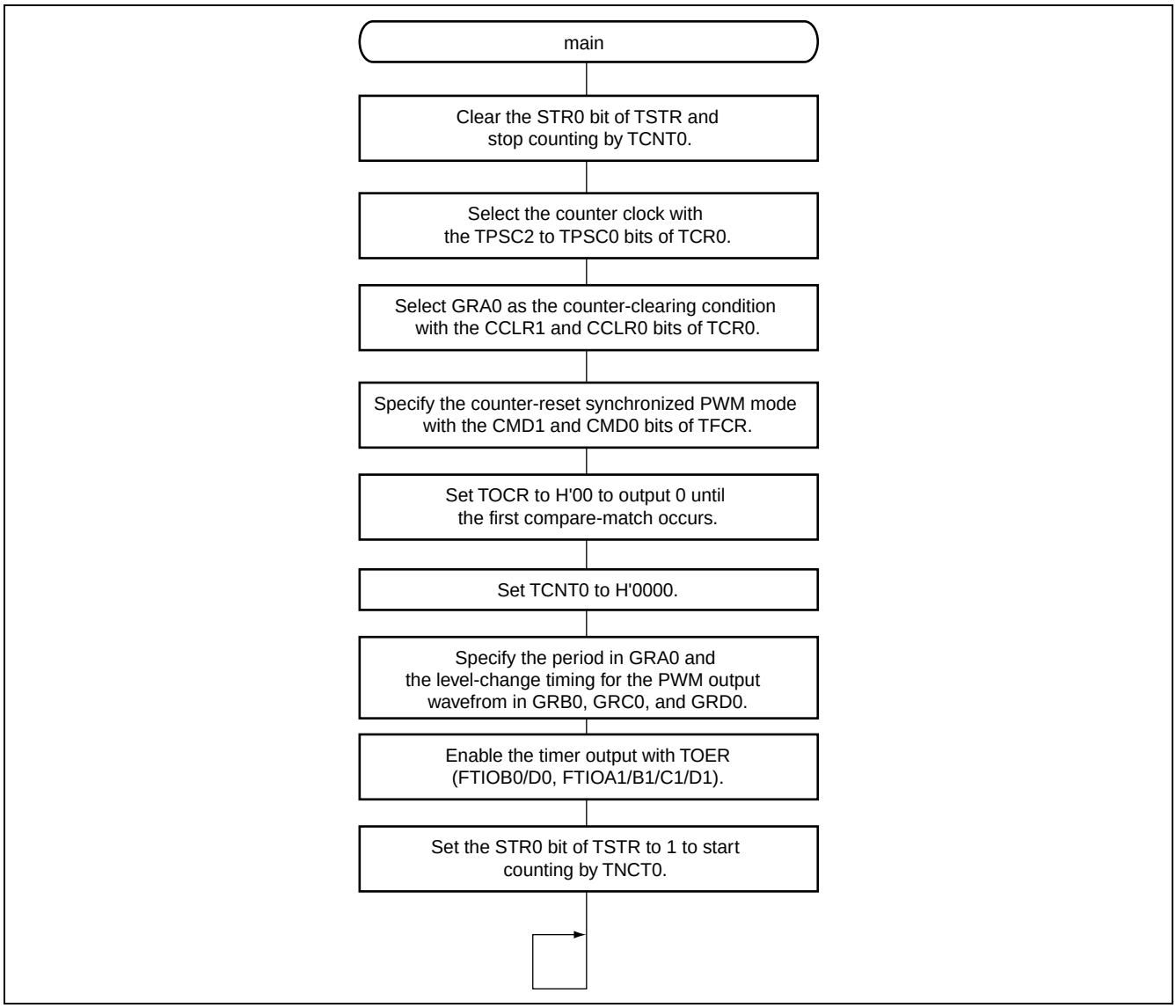
Pin and Register Names	Assigned Function
TSTR	Enables or disables counting by timer channels 0 and 1.
TCR0	Selects the input clock and the condition that clears the channel 0 timer counter.
TFCR	Specifies the reset-synchronous PWM mode.
TOCR	Specifies the initial output until the first compare-match occurs.
TOER	Enables or disables the timer output.
GRA0	Specifies the output pulse cycle.
GRB0	Specifies the timing of the level change for the PWM-output pair on FTIOB0 and FTIOD0 pins.
GRA1	Specifies the timing of the level change for the PWM-output pair on FTIOA1 and FTIOC1 pins.
GRB1	Specifies the timing of the level change for the PWM-output pair on FTIOB1 and FTIOD1 pins.
TCNT0	Channel 0 timer counter

4.4 RAM used

This sample task uses no RAM.

5. Flowchart

1. Main routine



6. Program Listing

```
/************************************************************/
/*                                                          */
/*    H8/300HN Series -H8/3687-                             */
/*    Application Note                                      */
/*                                                          */
/*   PWM Output of Three Normal- and                        */
/*    Inverse-Phase Signal Pairs                            */
/*                                                          */
/*    Function                                              */
/*    :Timer Z Reset Synchronous PWM Mode                   */
/*                                                          */
/*    External Clock: 16 MHz                                */
/*    Sub-clock: 32.768 kHz                                 */
/*                                                          */
/************************************************************/
#include    <C:\ch38\include\machine.h>

/************************************************************/
/*    Symbol Definition                                     */
/************************************************************/

struct BIT {
    unsigned char    b7:1;      /* bit7 */
    unsigned char    b6:1;      /* bit6 */
    unsigned char    b5:1;      /* bit5 */
    unsigned char    b4:1;      /* bit4 */
    unsigned char    b3:1;      /* bit3 */
    unsigned char    b2:1;      /* bit2 */
    unsigned char    b1:1;      /* bit1 */
    unsigned char    b0:1;      /* bit0 */
};

#define        TCR0      *(volatile unsigned char *)0xF700     /* Timer Control Register 0                */
#define        TIORA0    *(volatile unsigned char *)0xF701     /* Timer I/O Control Register A0           */
#define        TIORC0    *(volatile unsigned char *)0xF702     /* Timer I/O Control Register C0           */
#define        TSR0      *(volatile unsigned char *)0xF703     /* Timer Status Register 0                 */
#define        TSR0_BIT  (*(struct BIT *)0xF703)               /* Timer Status Register 0                 */
#define        IMIFA_0   TSR0_BIT.b0                           /* Input Capture/Compare match Flag A      */
#define        TIER0     *(volatile unsigned char *)0xF704     /* Timer Interrupt Enable Register 0       */
```

```
#define        POCR0     *(volatile unsigned char *)0xF705     /* Port Output Level Control Register       */
#define        TCNT0     *(volatile unsigned short *)0xF706    /* Timer Counter 0                          */
#define        GRA0      *(volatile unsigned short *)0xF708    /* General Register A0                      */
#define        GRB0      *(volatile unsigned short *)0xF70A    /* General Register B0                      */
#define        GRC0      *(volatile unsigned short *)0xF70C    /* General Register C0                      */
#define        GRD0      *(volatile unsigned short *)0xF70E    /* General Register D0                      */

#define        TCR1      *(volatile unsigned char *)0xF710     /* Timer Control Register 1                 */
#define        TIORA1    *(volatile unsigned char *)0xF711     /* Timer I/O Control Register A1            */
#define        TIORC1    *(volatile unsigned char *)0xF712     /* Timer I/O Control Register C1            */
#define        TSR1      *(volatile unsigned char *)0xF713     /* Timer Status Register 1                  */
#define        TIER1     *(volatile unsigned char *)0xF714     /* Timer Interrupt Enable Register 0        */
#define        POCR1     *(volatile unsigned char *)0xF715     /* Port Output Level Control Register       */
#define        TCNT1     *(volatile unsigned short *)0xF716    /* Timer Counter 1                          */
#define        GRA1      *(volatile unsigned short *)0xF718    /* General Register A1                      */
#define        GRB1      *(volatile unsigned short *)0xF71A    /* General Register B1                      */
#define        GRC1      *(volatile unsigned short *)0xF71C    /* General Register C1                      */
#define        GRD1      *(volatile unsigned short *)0xF71E    /* General Register D1                      */

#define        TSTR      *(volatile unsigned char *)0xF720     /* Timer Start Register                     */
#define        TMDR      *(volatile unsigned char *)0xF721     /* Timer Mode Register                      */
#define        TPMR      *(volatile unsigned char *)0xF722     /* Timer PWM Mode Register                  */
#define        TFCR      *(volatile unsigned char *)0xF723     /* Timer Function Control Register          */
#define        TOER      *(volatile unsigned char *)0xF724     /* Timer Output Master Enable Register */
/************************************************************/
/* Function definition                                      */
/************************************************************/
extern    void    INIT ( void );                               /* SP Set                                   */
void      main      ( void );

extern void _INITSCT();

/************************************************************/
/*    Vector Address                                        */
/************************************************************/
#pragma    section        V1                                 /* VECTOR SECTION SET                       */
void (*const VEC_TBL1[])(void) = {
/* 0x00 - 0x0f */
    INIT                                                     /* 00 Reset                                 */
};
```

```
#pragma    section/* P                                              */
/*****************************************************************/
/*    Main Program                                                 */
/*****************************************************************/
void main ( void )
{
   _INITSCT();

    set_imask_ccr(1);                                   /* Disable interrupts                      */

     TSTR = 0xFC;                                       /* Stop the timer                          */
    TOCR = 0x07;                                        /* PWM initial output "0"                  */

    TCR0 = 0x20;                                        /* GRA Compare Match Clear Mode            */
    TFCR = 0x01;                                        /* Reset Synchronous PWM Mode              */

    TCNT0 = 0x0000;                                     /*  Initial value                          */

    GRA0 = 0x320;                                       /* Cycle 50us                              */
    GRB0 = 0xF0;                                        /* Duty cycle 30%                          */
    GRA1 = 0xF0;                                        /* Duty cycle 30%                          */
    GRB1 = 0xF0;                                        /* Duty cycle 30%                          */

    TOER = 0x00;                                        /* Enable output on FTIOB0,  */
                                                        /* FTIO00, FTIOA1, FTIOB1,FTIOC1, FTIOD1 */

    TIER0 = 0x00;                                       /* Disable interrupts  */

    TSTR = 0xFD;                                        /* TCNT0       Start         */

    while(1){
        ;
        }
}
```

INIT.SRC (Program Listing)

```
      .EXPORT_INIT
      .IMPORT_main
  ;
      .SECTION    P,CODE
  _INIT:
      MOV.W  #H'FF80,R7
      LDC.B  #B'10000000,CCR
      JMP           @_main
  ;
        .END
```

Link address specification

Section Name	Address
CV1	H'0000
P	H'0100
B	H'F780