RX630 Group

MTU2a Operation in PWM Mode

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Abstract

This document describes operation of RX630 Group multi-function timer pulse unit 2 (MTU) in PWM mode.

Products

RX630 Group

Contents

1. Overview

PWM mode is used to output PWM waveforms.
The output level changes when the counter value matches the value set in the TGR register. The output level can be selected from low, high, or toggle. The TIOR register value determines the initial output level and the output level when the counter value matches the TGR register value.
The PWM waveform period and duty cycle can be set separately for each channel. In addition, when synchronous operation is selected, PWM waveforms with the same period can be output from multiple channels.
PWM mode is divided into PWM mode 1 and PWM mode 2. Figure 1.1 shows an example of output waveforms in each mode.

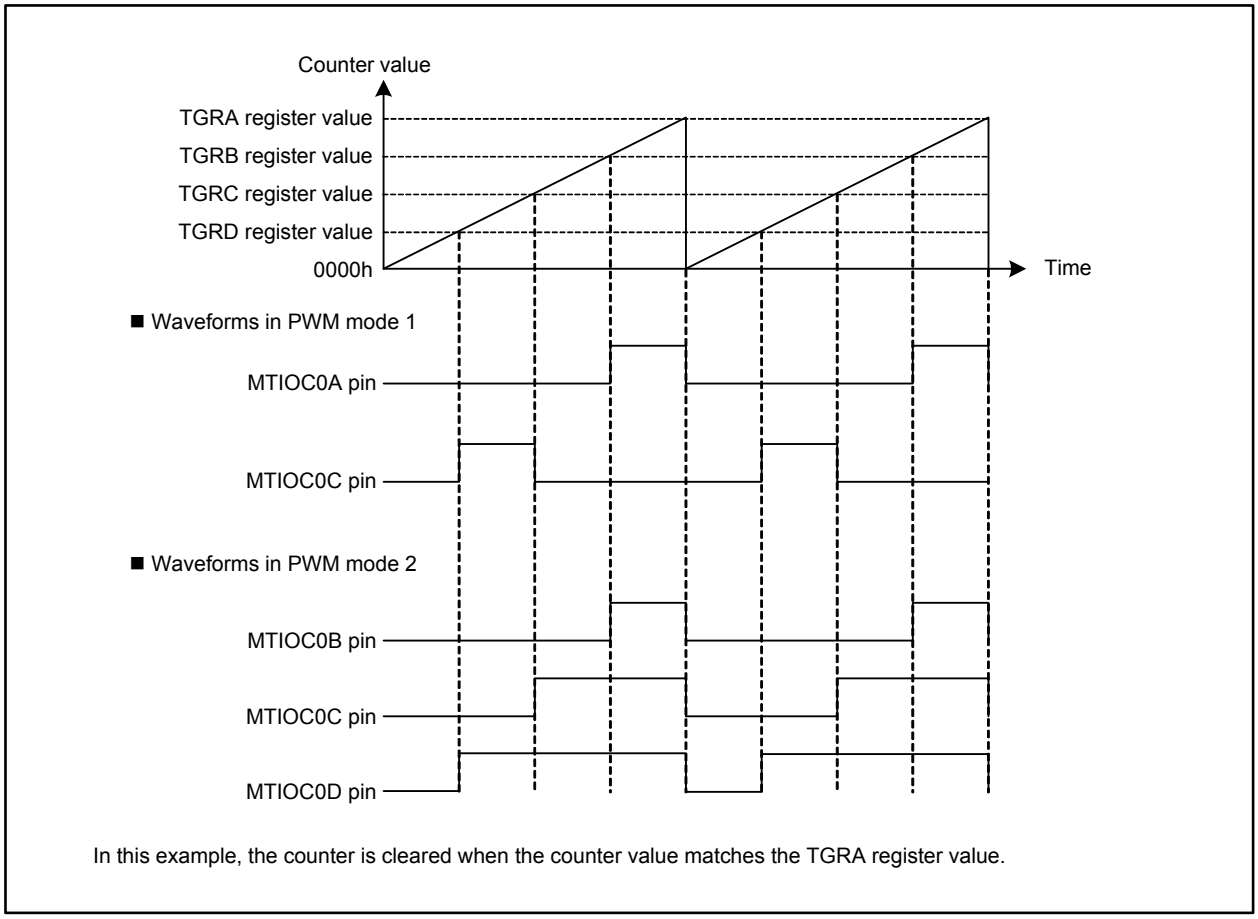

Figure 1.1 Comparison of Waveforms Output in PWM Mode 1 and PWM Mode 2 Using Channel 0

Table 1.1 lists the registers and output pins used in PWM mode 1 and PWM mode 2.

Table 1.1 Channels, Registers, and Output Pins Used in PWM Mode

Channel	Register	Output Pin	
		PWM mode 1	PWM mode 2 (1)
MTU0	TGRA	MTIOC0A	MTIOC0A
	TGRB		MTIOC0B
	TGRC	MTIOC0C	MTIOC0C
	TGRD		MTIOC0D
MTU1	TGRA	MTIOC1A	MTIOC1A
	TGRB		MTIOC1B
MTU2	TGRA	MTIOC2A	MTIOC2A
	TGRB		MTIOC2B
MTU3	TGRA	MTIOC3A	N/A
	TGRB		
	TGRC	MTIOC3C	
	TGRD		
MTU4	TGRA	MTIOC4A	
	TGRB		
	TGRC	MTIOC4C	
	TGRD		

Note:
1. After setting the TCR.CCLR[2:0] bits to select a TGR register as an event to clear the counter, the pin corresponding to the selected TGR register cannot output a PWM waveform in PWM mode 2.

2. Operating Mode

2.1 PWM Mode 1

A maximum of eight PWM waveforms can be output when using MTU0 to MTU4.
Two TGR registers are used for one output pin. The output level changes according to the TIOR register setting when the counter value matches the value set in the TGR register.
The value of the TGR register used to clear the counter determines the PWM waveform period.
When the values of the two TGR registers are the same, the corresponding output level does not change even when there is a match with the counter value.

2.2 PWM Mode 2

A maximum of seven PWM waveforms can be output when using MTU0 to MTU2. When the counter is cleared in synchronization with MTU3 or MTU4, a maximum of eight PWM waveforms can be output.
The output level changes according to the TIOR register setting when the counter value matches the value set in the TGR register. The value of the TGR register used to clear the counter determines the PWM waveform period.
If the value of the register used to clear the counter is the same as any of the other TGR register values, the corresponding output level does not change even when there is a match with the counter value.
A PWM waveform cannot be output from the pin corresponding to the TGR register used to clear the counter.

3. Setting PWM Mode

Figure 3.1 shows an example of the procedure for setting PWM mode.

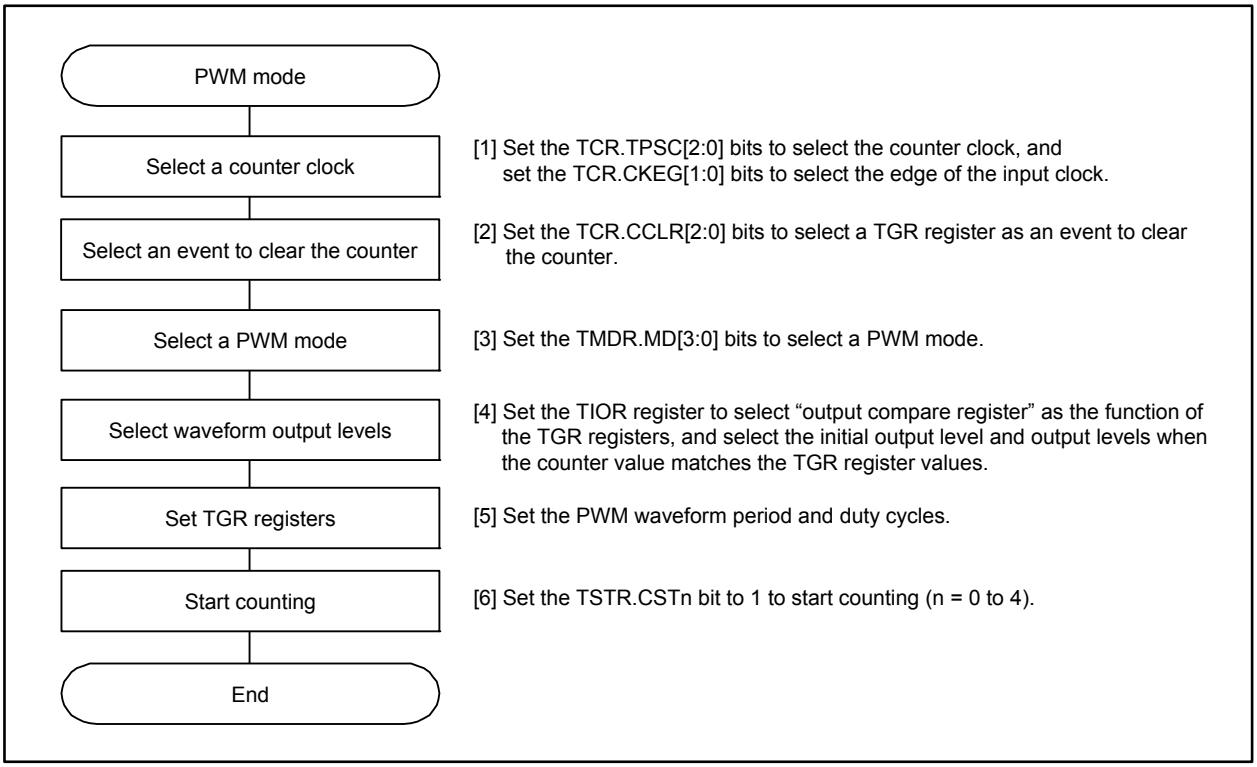

Figure 3.1 Example of Setting PWM Mode

4. Example of Operation in PWM Mode

4.1 Synchronous Operation

Figure 4.1 shows an example of outputting waveforms using synchronous operation between MTU0 and MTU1 (setting bits TSYR.SYNC0 and SYNC1 to 1) in PWM mode 2.

In the figure, five PWM waveforms are output under the following conditions: the counter is cleared when the counter matches the MTU1.TGRB value; initial output levels are low; and the output levels become high when the counter value matches the corresponding TGR register value. In this example, the value set in the MTU1.TGRB register is the PWM waveform period, and the values set in other TGR registers determine duty cycles.

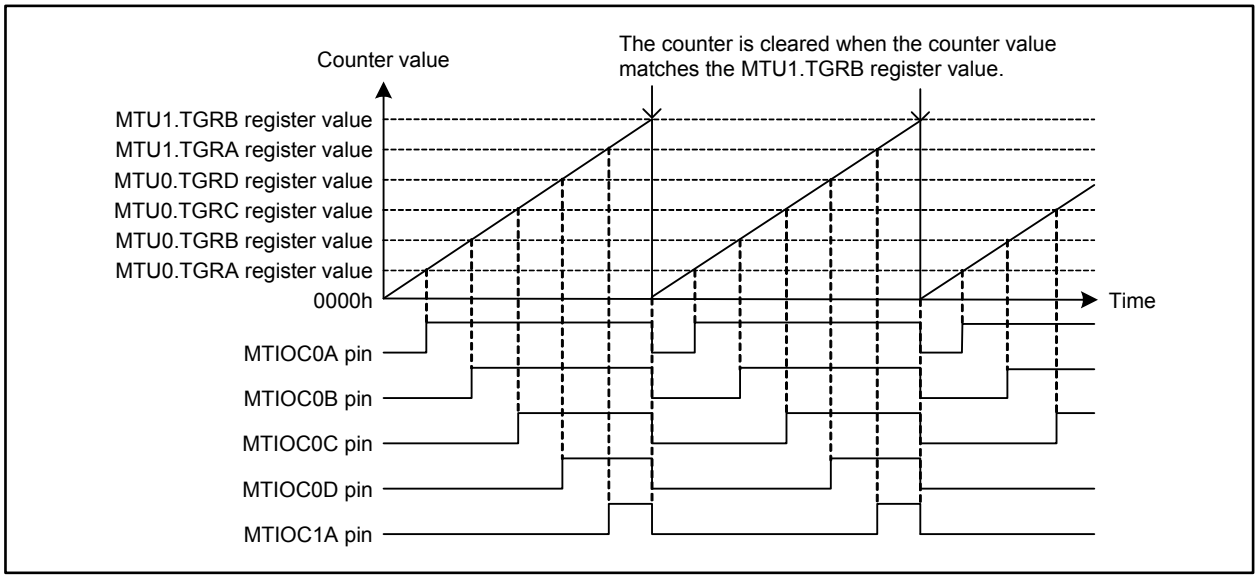

Figure 4.1 Example of Synchronous Operation in PWM Mode

4.2 PWM Waveform Output with 0% and 100% Duty Cycles

Figure 4.2 shows an example of outputting PWM waveforms with 0% and 100% duty cycles in PWM mode. All cases in the figure assume that the output levels become high when the counter value matches the TGRB register value. When the TGRB register value is greater than the TGRA register value, the counter value does not match the TGRB register value, so the output level does not become high. When setting the TGRB register to the same value as the TGRA register after the output pin becomes high, the counter value matches the TGRA register value and the TGRB register value at the same time, so the output level remains high. In this way, a waveform with 0% or 100% duty cycle can be output.

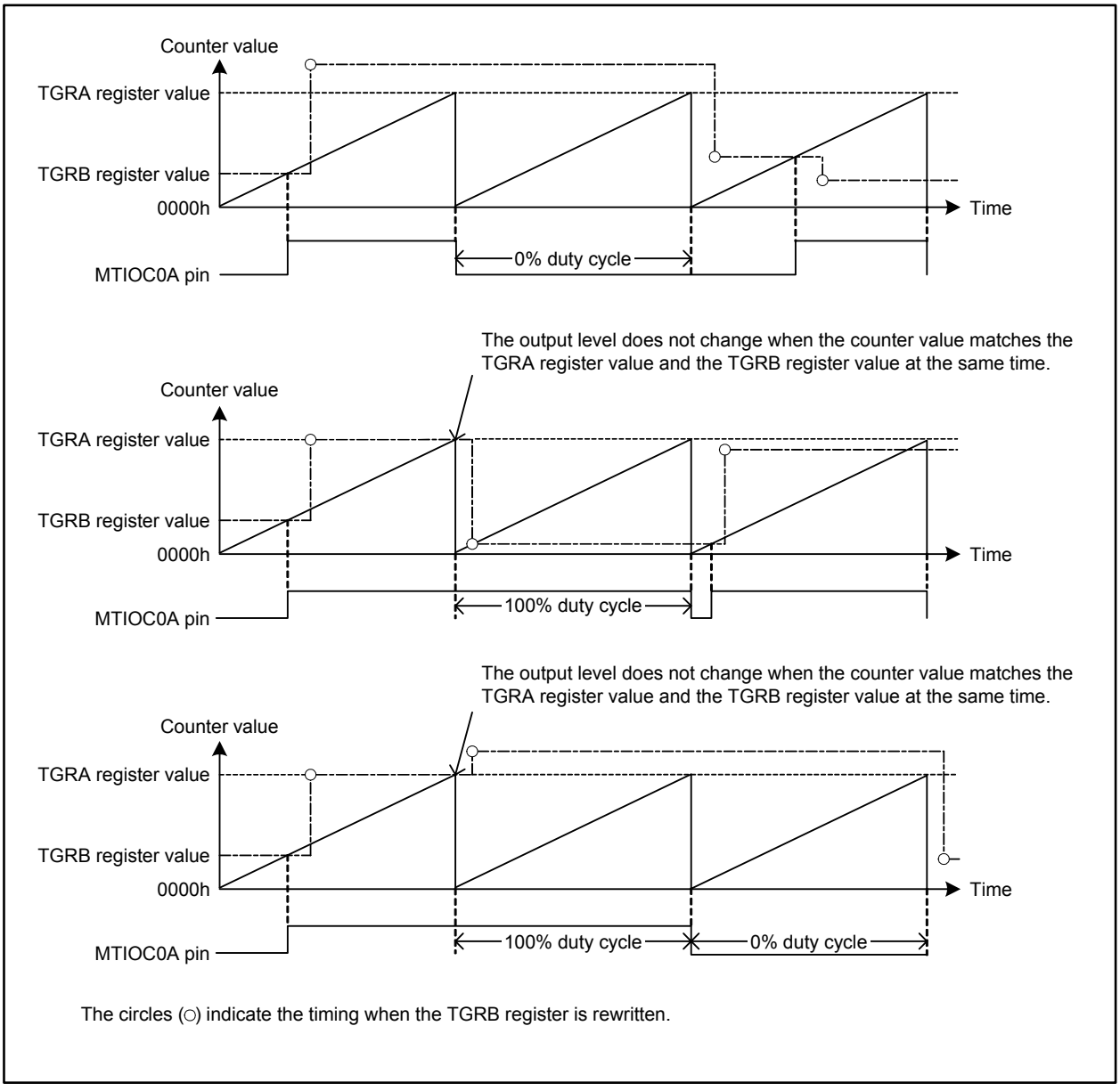

Figure 4.2 Example of Outputting PWM Waveforms with 0% and 100% Duty Cycles

5. Reference Documents

User's Manual: Hardware
RX630 Group User's Manual: Hardware Rev.1.20
The latest version can be downloaded from the Renesas Electronics website.

Technical Update
The latest information can be downloaded from the Renesas Electronics website.

Website and Support

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Revision History	RX630 Group MTU2a Operation in PWM Mode

Rev.	Date	Description	
		Page	Summary
1.00	Oct. 5, 2012	—	Initial release

General Precautions in the Handling of MPU/MCU Products

The following usage notes are applicable to all MPU/MCU products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

1. Handling of Unused Pins

   Handle unused pins in accord with the directions given under Handling of Unused Pins in the manual.

   — The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible. Unused pins should be handled as described under Handling of Unused Pins in the manual.

2. Processing at Power-on

   The state of the product is undefined at the moment when power is supplied.

   — The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the moment when power is supplied.
   In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the moment when power is supplied until the reset process is completed.
   In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the moment when power is supplied until the power reaches the level at which resetting has been specified.

3. Prohibition of Access to Reserved Addresses

   Access to reserved addresses is prohibited.

   — The reserved addresses are provided for the possible future expansion of functions. Do not access these addresses; the correct operation of LSI is not guaranteed if they are accessed.

4. Clock Signals

   After applying a reset, only release the reset line after the operating clock signal has become stable. When switching the clock signal during program execution, wait until the target clock signal has stabilized.

   — When the clock signal is generated with an external resonator (or from an external oscillator) during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Moreover, when switching to a clock signal produced with an external resonator (or by an external oscillator) while program execution is in progress, wait until the target clock signal is stable.

5. Differences between Products

   Before changing from one product to another, i.e. to a product with a different part number, confirm that the change will not lead to problems.

   — The characteristics of an MPU or MCU in the same group but having a different part number may differ in terms of the internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.

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