Modular Baseband Design Enabling a Low Cost, Reusable Wireless Infrastructure Application Note - 415

Notes

Introduction

Over the last decade wireless base station designers have made major strides in their constant struggle to reduce cost, power and footprint. For these designers the goal for 3G base station development is simple: To achieve ten times the bandwidth at one tenth the cost.

The processing power required to handle baseband algorithms continues to increase with new wireless protocols. As shown in figure 1, conventional digital signal processors (DSPs) may not have enough MIPS power to perform baseband processing, resulting in the need for hardware acceleration to supplement the DSPs[2]. A typical architecture may consist of a cluster of DSPs and hardware accelerator blocks on the baseband card where multiple channels are processed.

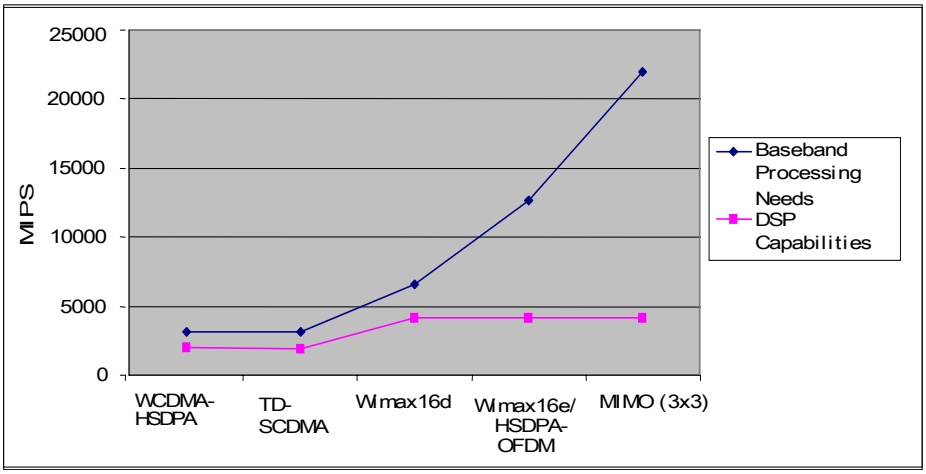

Figure 1: MIPS requirements for different wireless protocols

Today's base station typically relies on a sequential processing scheme, and every block and processing is time aligned[1].The architecture often looks like figure 2. One chip-rate processor (CRP) interfaces to the time-sliced backplane and receives "samples" from the RF card.

In CDMA-related systems (such as WCDMA, CDMA2000) samples are converted to chips and eventually to symbols before transitioning to the DSP, often via the parallel memory interface. The DSP performs the "symbol-rate processing" such as error correction and voice/data channel processing.

In orthogonal frequency division multiplexing (OFDM) systems (such as 802.16x, WiMAX), the CRP is replaced by the OFDM PHY, which performs synchronization and FFT before handing symbols to the DSPs. DSPs perform similar operations to the CDMA architecture.

This architecture is not very scalable as ASIC and DSP processing allocations are fixed at the time of design, and are tightly coupled with the selection of the hardware. As a result, some DSPs and CRPs might be underutilized in some base stations, but this inefficiency is allowed to exist because it is very difficult to shift resources from one processing block to another during run time.

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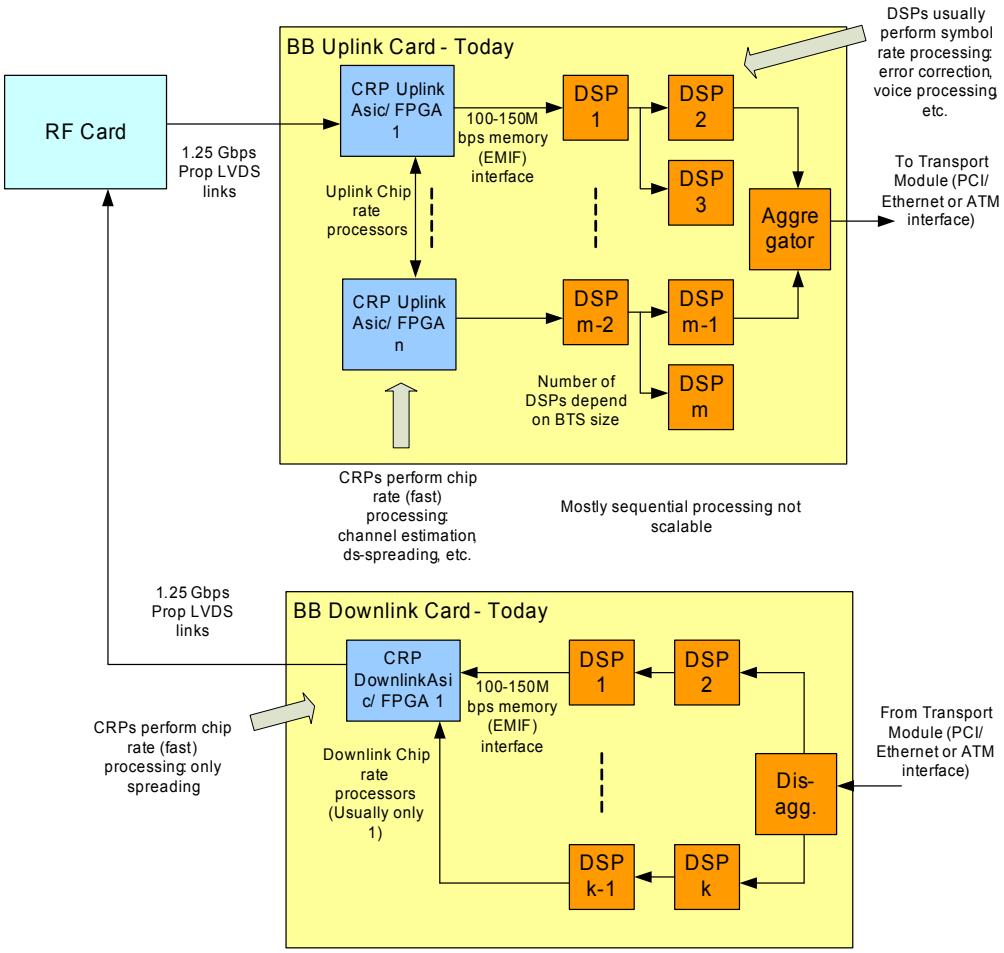

Figure 2: Today's typical base band card architecture

It is also not easy to have the same architecture for pico base station, micro and macro base station, as it is a challenge to scale algorithms developed for the CRPs and DSPs in a given application. For a small performance increment, a whole new group of CRPs and DSPs may need to be added.

In some architectures, one of the CRPs interfaces to the backplane (RF card) and the rest of the CRPs talk to the first CRP (uplink card). This requires a different design for the backplane interface CRP, as one cannot replicate the same design to the subordinate CRPs without reducing their effectiveness and thus decreasing the return on investment for developing the CRPs.

The memory interface between the CRPs and DSPs can also be a problem for the system software. The bi-directional nature of a standard memory interface can make it harder to fully utilize this interconnect. Usually baseband algorithms are sensitive to non- deterministic delay, which may be introduced using a bi-directional interface.

Emerging Standards to the Rescue

In recent years the industry has thrown its support behind a number of standards-based efforts to promote modularity at the system and network levels, allowing for cost-effective reuse of engineering efforts and scalable architectures.

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One of the best examples of this trend is the Open Base Station Architecture Initiative (OBSAI). OBSAI defines modular base station architecture with standardized interfaces between each module in the base station[3].

Six months after OBSAI was launched, a competing standard, Common Public Radio Interface (CPRI) was announced. Far simpler than OBSAI, CPRI focuses on the UMTS base station by dividing it into a RF and control block connected via a standard digital interface[4].

To address the needs of network equipment manufacturers and service providers at the chassis level, the PCI Industrial Computer Manufacturers Group (PCI-MG) has defined a standard chassis form factor called the Advanced Telecom Computing Architecture (ATCA)[5].

DSP blades in wireless base station applications need highly simplified, high-speed interconnects for data transfer and protocol management. These computationally-intense embedded applications require the system to quickly move data between signal processors in a tightly-coupled DSP farm. The serial RapidIO (sRIO)[6] specifications, developed as an open standard, was expressly designed to address the needs of high-performance embedded systems.

The sRIO standard complements the modularity benefits that standards like OBSAI, CPRI and ATCA bring at the chassis and system levels by extending those advantages to the board level. Neither OBSAI nor CPRI define the line-card interface in a base station design.

Moreover, sRIO's highly tuned support for DSP clusters allows equipment designers to develop very flexible and scaleable architectures in a cost-efficient manner that simply cannot be replicated in FPGA or ASIC-based designs. For example, using sRIO a base station designer can build a DSP-intensive system for macro cell applications allowing the rapid deployment of new technology to support wide areas of coverage, and then reuse much of the original design in scaled-down solutions for micro or pico-cellular environments that deliver the desired saturation and density in the most cost-effective manner.

Most importantly, sRIO simplifies inter-processor communications by integrating control and data traffic, offloading simple and time-consuming tasks from the processor, and differentiating between high- and low-priority data traffic.

Putting it all together

Then the next question is: How do we put all of these together for base station development? What is missing to get a complete baseband card design?

Before looking into next-generation architectures, let's look at the algorithm-protocol partitioning for the base stations.

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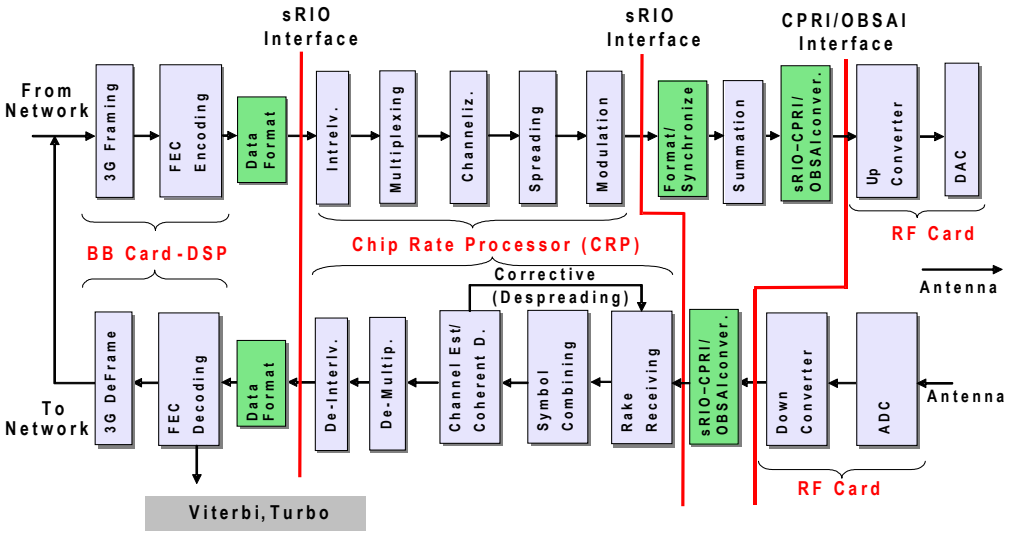

Figure 3: Algorithm-protocol partitioning for CDMA based systems

The light blue blocks are mathematical operations needed for CDMA based (UMTS, CDMA2000, etc.) baseband transceiver. An ideal baseband card has a cluster of DSPs and hardware accelerator blocks (or CRPs) in the form of FPGAs or ASICs. Figure 3 shows partitioning of algorithms to DSP and CRPs. There might be multiple DSPs and CRPs depending on the processing requirements for the baseband card, therefore these blocks need to be connected. A similar partition and observation can be made for OFDM-based algorithms.

Serial RIO and CPRI/OBSAI interfaces are also shown in Figure 3 designated with red lines. Serial RIO is used to connect multiple processing blocks on the baseband card, as shown in figure 4. These interfaces are also shown on figure 3 with algorithm partitioning. Note the green blocks next to the interfaces are necessary for data formatting between the interface and algorithms such as sign extension, packetization of samples/symbols, and multiple-packet alignment (from multiple CRPs) before summation. These functions have to be performed by one of the neighboring devices to this interface. The question is: What is the ideal architecture to handle this partitioning?

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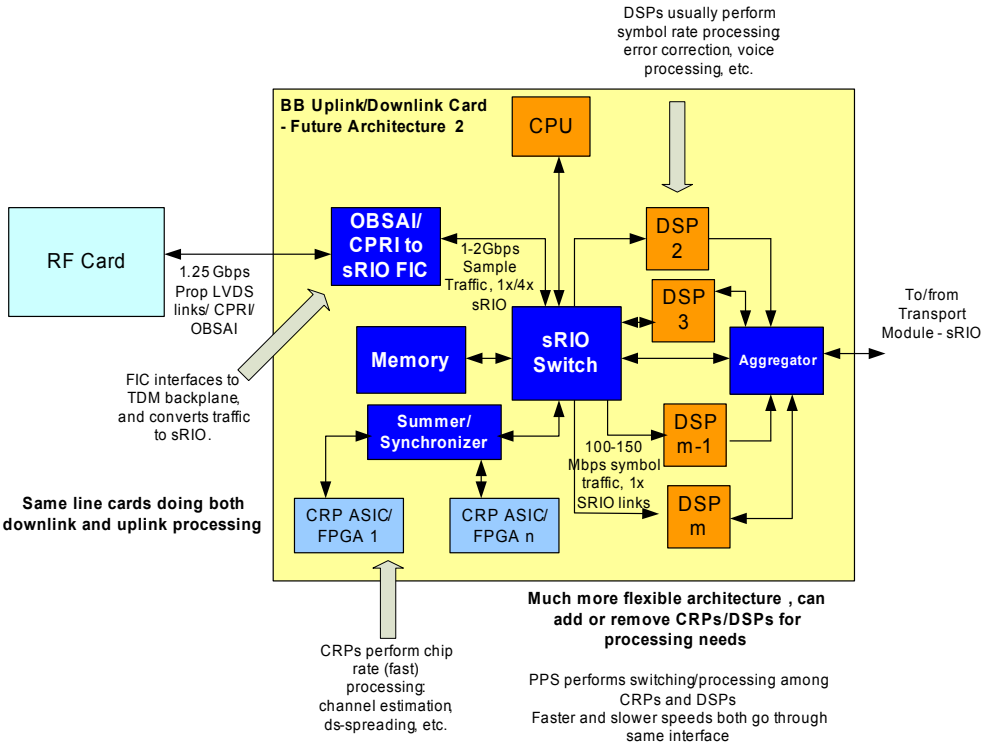

Figure 4: Ideal Baseband Architecture

Figure 4 shows a close-to-ideal architecture for next-generation baseband cards. A fabric interface component (FIC) translates CPRI/OBSAI to sRIO, and the rest of the baseband card interface is sRIO, but a regular sRIO switch will not be enough to handle special operations needed. There are 2 distinct traffic flows on the baseband card:

1) Between the FIC and CRPs: High-speed traffic (spread samples) with deterministic timing. Latency on this link needs to be deterministic to support timing requirements in the base station. Packets are multicast to multiple CRPs on uplink, summed on downlink.
2) Between CRPs and DSPs: Much more flexible in latency, lower bandwidth (symbols) traffic, as well as control and maintenance packets.

A regular sRIO switch needs to be supported with a summer and synchronizer device, which aligns packets from multiple CRPs, sums them on the uplink, and multicasts them to CRPs on the uplink.

Different devices and algorithms work on different sample and symbol sizes. For example, CPRI defines sample size ranging from 8 bits to 40 bits. Processors like to work on sample sizes 8, 16 or 32. Also different algorithms want samples in specific order (I-Q together or separate, over-samples together with regular samples or separate, etc.) therefore these data formatting operations need to be performed in the CRP and the DSP. Depending on selection of DSP and CRP, there are a lot of combinations of these operations that system designer need to be aware of, and processors might spend a lot of MIPS to do these operations.

Baseband card sizes can be small to large depending on the system. Micro-TCA form factor can be close enough for all different cards in the base station. This will give designers the means to build a large and varied selection of interchangeable modules to meet the needs of telecommunications equipment manufacturers.

This architecture also supports flexible and scalable base station designs.

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1) Flexible: Exchanging CRPs with OFDM PHYs; the same design can be used for both CDMA and OFDM based systems
2) Scalable: Number of CRPs and DSPs can be changed easily to adapt the same design for pico to macro base stations. Traffic and processing power can also be shifted from one device to another at run time since the architecture is not tightly coupled with algorithms anymore.

Conclusion

The development of 3G wireless networks is at a crossroads. Subscribers expect higher levels of service at lower cost. Yet the bandwidth and performance requirements implicit in delivering triple-play services will demand increasingly sophisticated and complex base station designs.

The key to meeting those needs while lowering costs will lie in the adoption of modular, standards-based architectures. By embracing emerging industry standards such as ATCA, OBSAI and CPRI and leveraging the high degree of design flexibility and adaptability in DSP-based arrays using the sRIO interface, base station designers can deliver high performance next-generation wireless services at a cost structure users will embrace.

References:

[1] Bertan Tezcan et al, “Advantages of Packet Switched Communication in Next-Generation Wireless Basestation Equipment”, GSPx, September 2004

[2] Andsers Nilsson, et al, “An Accelerator Architecture for Programmable Multi-Standard Baseband Processor”, WNET, 2004

[3] www.obsai.com

[4] www.cpri.info

[5] www.atca.org

[6] www.rapidio.org

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Corporate Headquarters

TOYOSU FORESIA, 3-2-24 Toyosu,
Koto-ku, Tokyo 135-0061, Japan
www.renesas.com

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