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H8/300H Super Low Power Series

Methods for Trimming of LCD 3-V Constant-Voltage Circuit

Introduction

The LCD controller/driver of the H8/38099 has an internal 3-V constant-voltage power supply circuit, so that the LCD panel can be driven at a constant brightness regardless of the Vcc voltage.

This application note describes a method of trimming the 3-V constant-voltage circuit using the A/D converter and another method using the rotary DIP switch.

Target Device

H8/38099

Contents

1. Specifications

1.1 Automatic Trimming Method Using the A/D Converter

1. The V2 output voltage of the 3-V constant-voltage power circuit in the LCD controller/driver is input to the AN0 pin of the A/D converter.
2. The A/D conversion results are reflected in the LCD trimming register, which is used for adjustment of the output voltage of the 3-V constant-voltage power circuit.
3. A/D conversion is performed at 1.024-ms intervals, using the auto reload function of timer C.
4. The 3-V constant-voltage power circuit and the A/D converter are connected as shown in figure 1 to perform trimming of the output voltage of the 3-V constant-voltage power circuit.

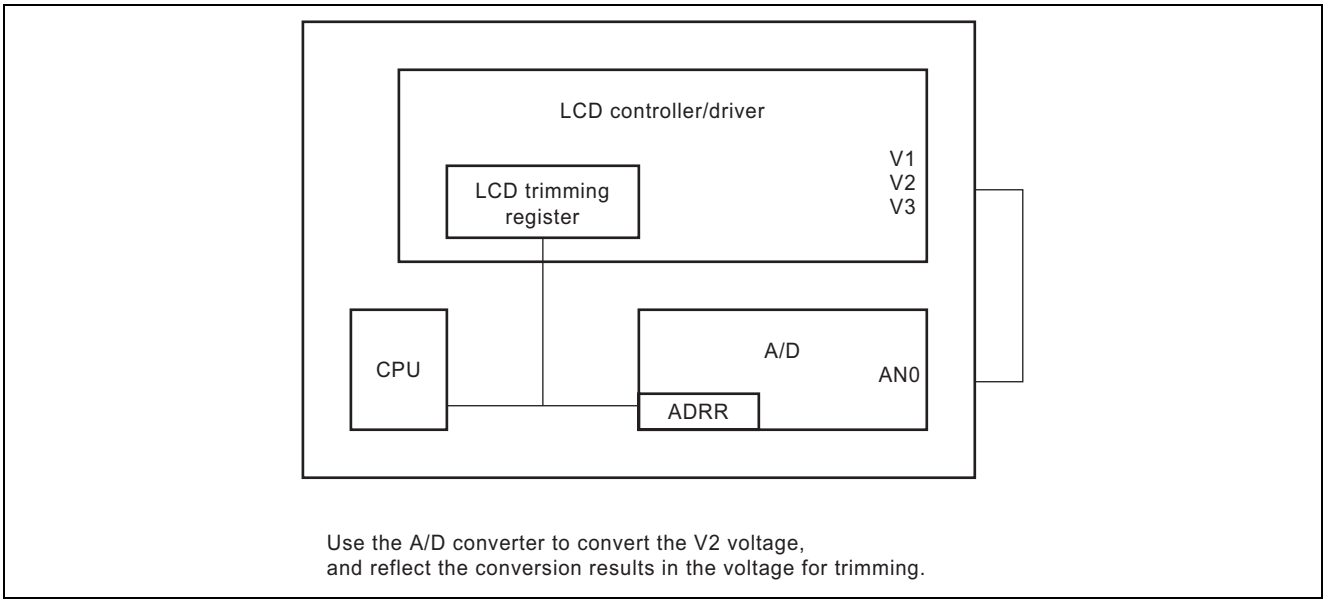


Figure 1 Automatic Trimming Using the A/D Converter

1.2 Method for Trimming by Visual Inspection

1. A rotary DIP switch is connected to port E to change the trimming voltage by changing the switch setting.
2. Port E is configured as an input port, and the value of port data register E is reflected in the LCD trimming register.
3. The auto reload function of timer C is used to scan port data register E at 1.024-ms intervals.
4. When the rotary DIP switch is not operated for 60 seconds, trimming is regarded to have ended.
5. The rotary DIP switch is connected as shown in figure 2 to perform trimming of the output voltage of the 3-V constant-voltage power circuit.

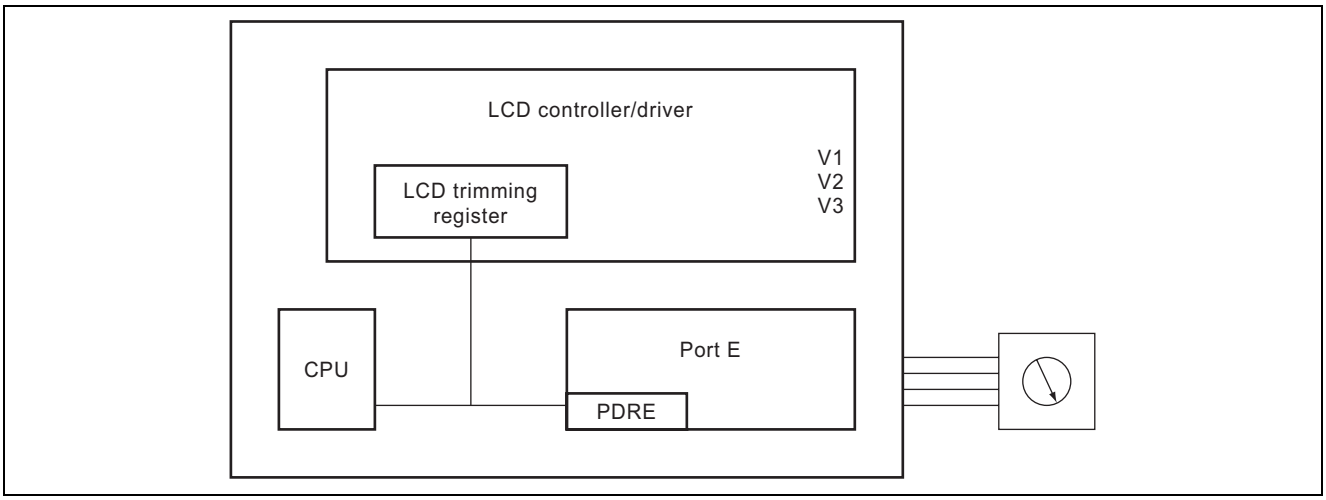


Figure 2 Method for Trimming by Visual Inspection

1.3 Switching between Trimming Methods

1. Trimming method is determined and switched by a program according to the input level on the PE3 pin of port E.
2. When the input level on the PE3 pin is high, the automatic trimming method using the A/D converter is used; when it is low, the method by visual inspection is used.

2. Description of Functions Used

2.1 Description of LCD Controller/Driver

Since the H8/38099 incorporates a segment-type LCD control circuit, LCD driver, and power supply circuit, it can drive an LCD panel directly. Figure 3 shows a block diagram of the LCD controller/driver.

- LCD port control register (LPCR)
  LPCR selects a duty cycle and configures the pins for the LCD driver pin function or port pin function.
- LCD control register (LCR)
  LCR controls the LCD driving power supply and display data and selects a frame frequency.
- LCR2 port control register 2 (LCR2)
  LCR2 switches between waveforms A and B, selects a step-up clock for the 3-V constant-voltage circuit, controls the connection of the LCD power-supply split resistor, and controls turning on or off the 3-V constant-voltage circuit.
- LCD trimming register (LTRMR)
  LTRMR is used to adjust the 3-V constant-voltage for use as the LCD driving power and the output voltage of the 3-V constant-voltage power circuit.
- BGR control register (BGRMR)
  BGRMR runs or stops the band gap reference circuit (BGR) for generating the reference voltage for the 3-V constant-voltage power, and fine-adjusts the reference voltage.
- Segment output pins (SEG40 to SEG1)
  These pins are for driving the segments of the LCD. All of these pins can also serve as port pins; they are programmable as either.
- Common output pins (COM4 to COM1)
  These pins are for driving the common lines of the LCD. Parallel connection of these pins are allowed when a static or 1/2 duty cycle is selected.
- LCD power pins (V1, V2, and V3)
  These pins are used when an external bypass capacitor is connected or when an external power supply circuit is used.
- LCD step-up capacitance pins (C1 and C2)
  These are pins for connecting a capacitor for stepping up the LCD driving power.
- LCD RAM
  The relationships between LCD RAM and display segments differ depending on the selected duty cycle. First, configure the group of registers necessary for display, then write data to the portion corresponding to the selected duty cycle by using the same instructions used for writing to normal RAM, and turn display on, and the display will automatically start. To set values in LCD RAM, word/byte access instructions can be used.

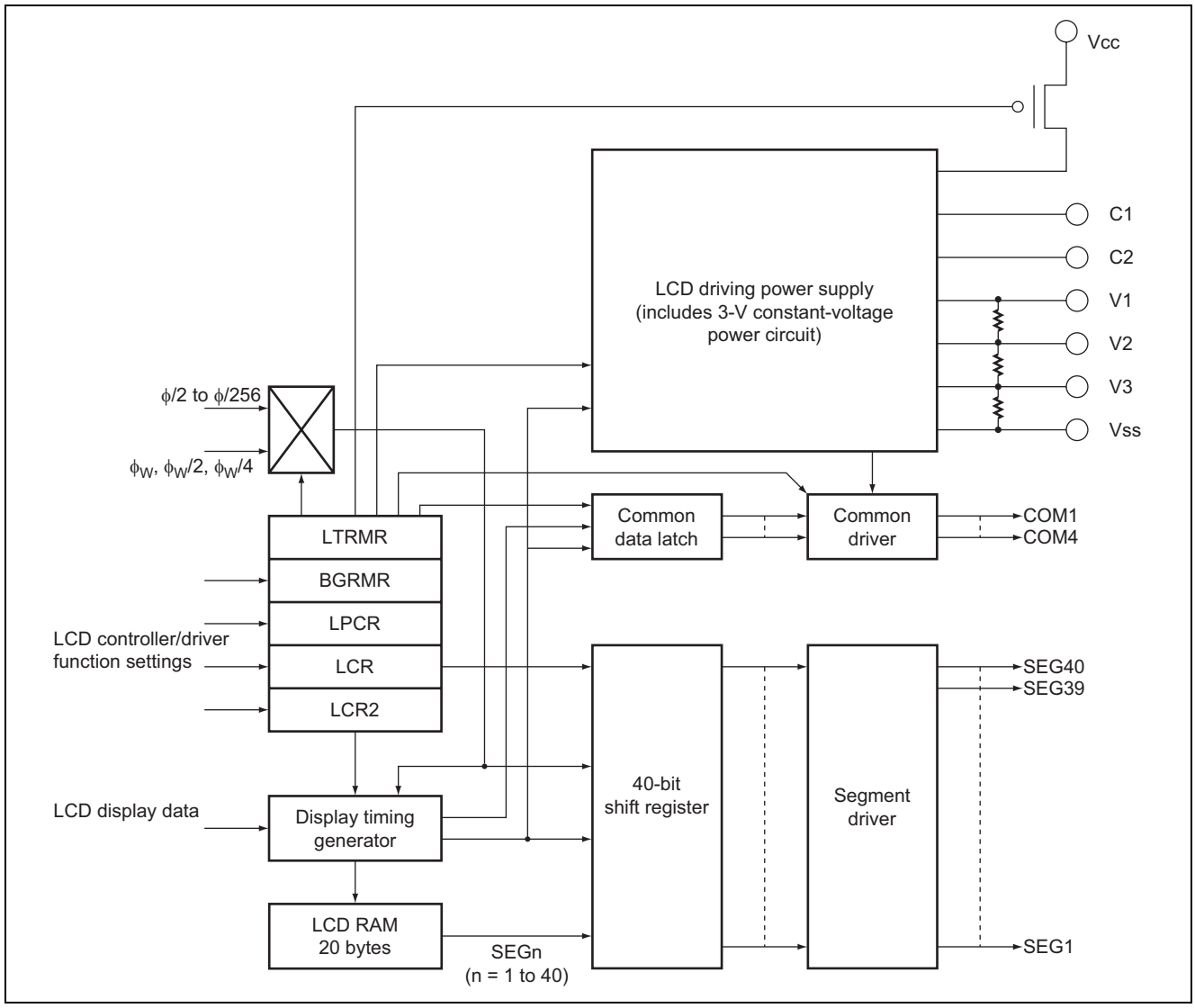


Figure 3 Block Diagram of the LCD Controller/Driver

2.2 3-V Constant-Voltage Power Circuit

The H8/38099 includes an internal 3-V constant-voltage power circuit consisting of a band gap reference circuit (BGR), a triple step-up circuit, and other components, so that a constant voltage of 3V can be used as the driving power for the LCD driver independently of the Vcc voltage. Before activating the step-up circuit, run the LCD controller/driver to select the duty cycle, select the LCD driver pin function or port pin function, set display data and a frame frequency, and make other settings; connect a 0.1-µF capacitor between the C1 and C2 pins and also connect a 0.1-µF capacitor to each of the V1 to V3 pins. After these settings have been made, set the BGRSTPN bit of the BGR control register (BGRMR) to 1 to activate the band gap reference circuit, which generates a constant voltage of 1 V (V_{LCD3}) on the V3 pin. Then, by selecting the clock for the step-up circuit with the LCD control register 2 (LCR2) and setting the SUPS bit of LCR2 to 1, the triple step-up circuit operates so that a constant voltage of 2 V, twice of V_{LCD3}, is generated on the V2 pin along with a constant voltage of 3 V, three times of V_{LCD3}, generated on the V1 pin. Figure 4 shows the connection to be made when using the 3-V constant-voltage power circuit.

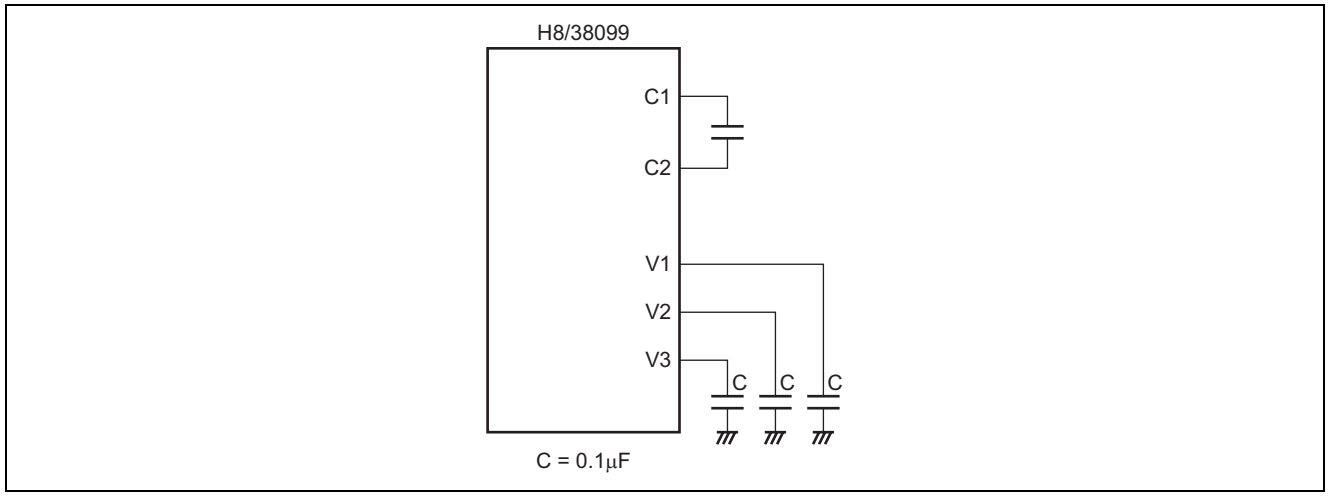


Figure 4 Method of Connecting When Using the 3-V Constant-Voltage Power Circuit

2.3 Characteristics of the Step-up Circuit

Figure 5 shows the normal distribution of the output voltage of the step-up circuit in the initial state. The number of devices measured is 643. The horizontal axis represents the V1 pin voltage, while the vertical axis represents the number of devices. The output voltage of the step-up circuit in its initial state differs from device to device due to manufacturing variations. Thus, be sure to adjust the voltage by setting the LCD trimming register (LTRMR) appropriately, on a device-by-device basis.

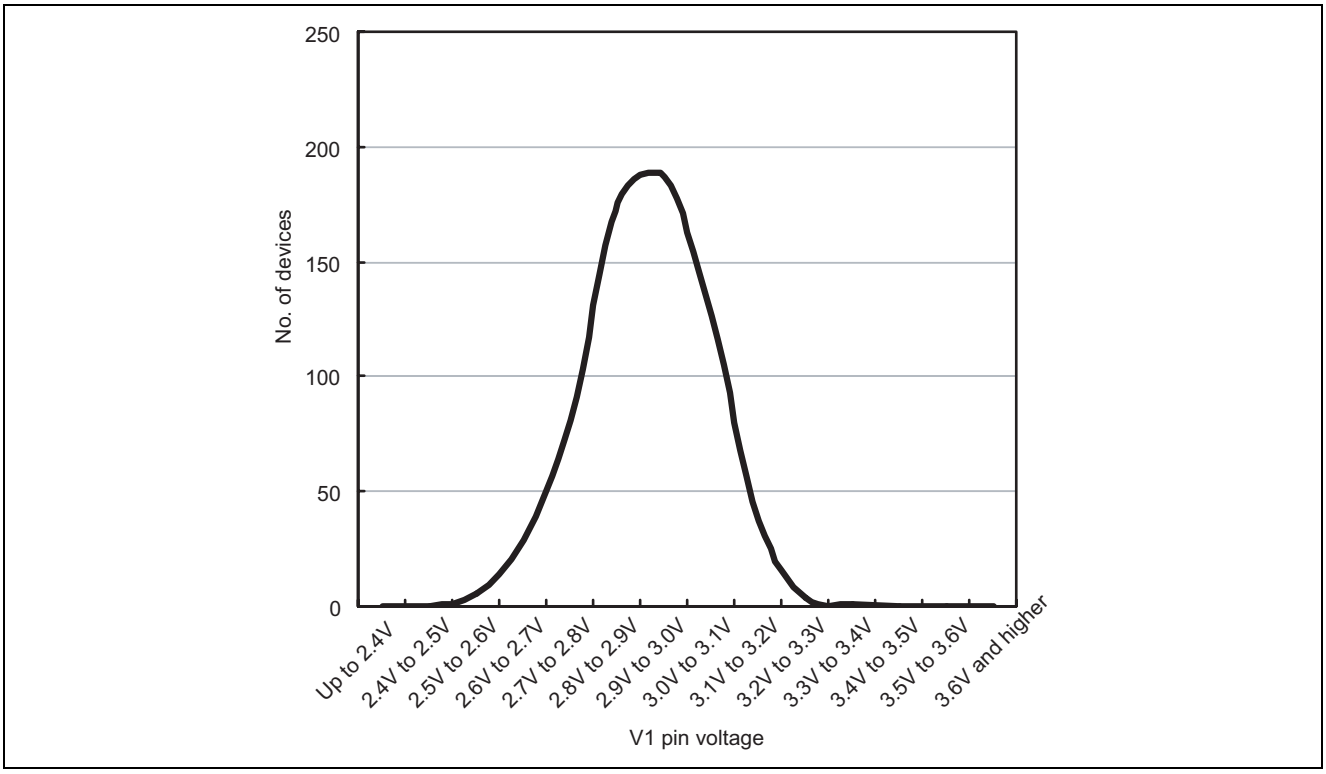


Figure 5 Normal Distribution of the Output Voltage of the Step-up Circuit in Its Initial State

2.4 Description of the LCD

The LCD panel used in this application note is driven with a duty cycle of 1/4 and at a frame frequency of 64 Hz. The outline of the LCD panel is shown in figure 6, the relationships between the segment signals of the LCD panel and LCD RAM are given in table 1, and the pins of the LCD panel and the H8/38099 that are to be connected together are given in table 2.

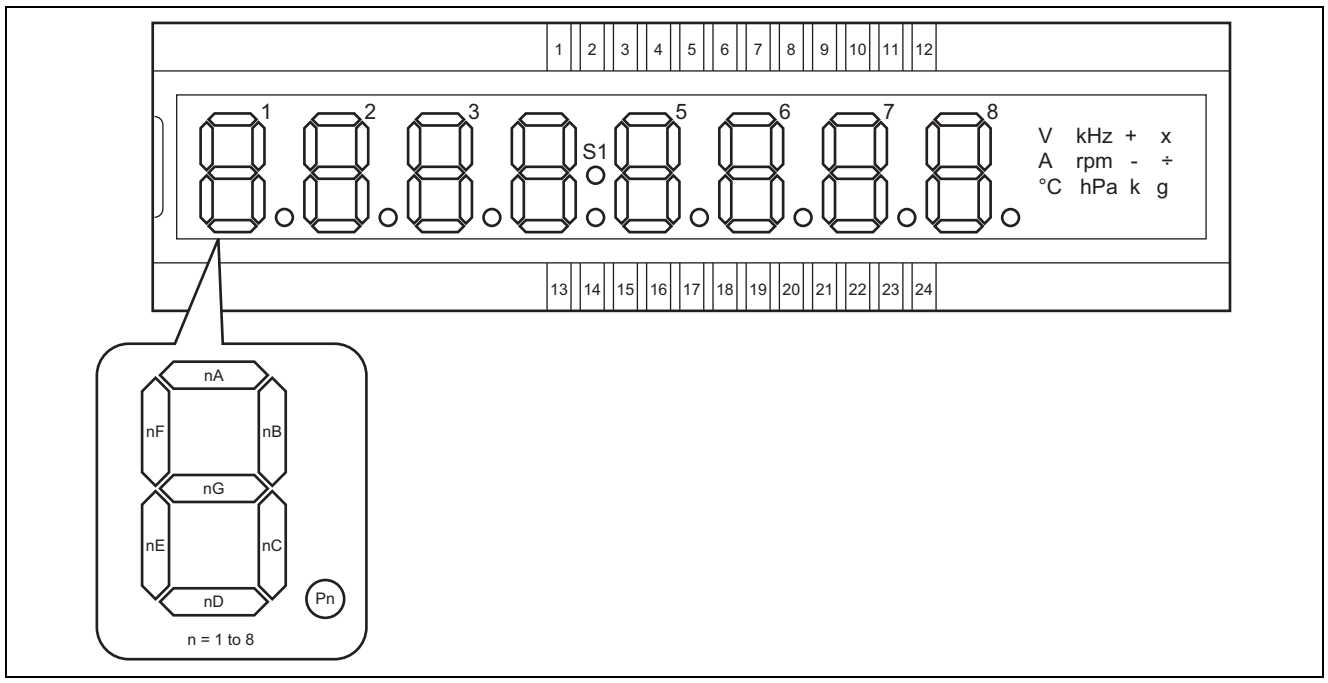


Figure 6 Outline of the LCD Panel

Table 1 Relationship between the Segment Signals of the LCD Panel (When Driven with 1/4-Duty Cycle) and LCD RAM

LCD RAM address	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
	COM4	COM3	COM2	COM1	COM4	COM3	COM2	COM1
H'FFF360	SEG2	SEG2	SEG2	SEG2	SEG1	SEG1	SEG1	SEG1
	1D	1E	1G	1F	P1	1C	1B	1A
H'FFF361	SEG4	SEG4	SEG4	SEG4	SEG3	SEG3	SEG3	SEG3
	2D	2E	2G	2F	P2	2C	2B	2A
H'FFF362	SEG6	SEG6	SEG6	SEG6	SEG5	SEG5	SEG5	SEG5
	3D	3E	3G	3F	P3	3C	3B	3A
H'FFF363	SEG8	SEG8	SEG8	SEG8	SEG7	SEG7	SEG7	SEG7
	4D	4E	4G	4F	P4	4C	4B	4A
H'FFF364	SEG10	SEG10	SEG10	SEG10	SEG9	SEG9	SEG9	SEG9
	5D	5E	5G	5F	P5	5C	5B	5A
H'FFF365	SEG12	SEG12	SEG12	SEG12	SEG11	SEG11	SEG11	SEG11
	6D	6E	6G	6F	P6	6C	6B	6A
H'FFF366	SEG14	SEG14	SEG14	SEG14	SEG13	SEG13	SEG13	SEG13
	7D	7E	7G	7F	P7	7C	7B	7A
H'FFF367	SEG16	SEG16	SEG16	SEG16	SEG15	SEG15	SEG15	SEG15
	P8	8C	8B	8A	8D	8E	8F	8G
H'FFF368	SEG18	SEG18	SEG18	SEG18	SEG17	SEG17	SEG17	SEG17
	kg	hPa	rpm	kHz	÷	–	×	+
H'FFF369	SEG20	SEG20	SEG20	SEG20	SEG19	SEG19	SEG19	SEG19
					S1	°C	A	V

Table 2 Pins of the LCD Panel and the H8/38099 That Are to Be Connected Together

LCD Panel Pin Number	H8/38099 Pin Number	H8/38099 Pin Function
pin1	7	SEG7
pin2	10	SEG10
pin3	9	SEG9
pin4	12	SEG12
pin5	11	SEG11
pin6	14	SEG14
pin7	13	SEG13
pin8 (NC)	—	—
pin9	41	COM1
pin10	42	COM2
pin11	43	COM3
pin12	44	COM4
pin13	2	SEG2
pin14	1	SEG1
pin15	4	SEG4
pin16	3	SEG3
pin17	6	SEG6
pin18	5	SEG5
pin19	8	SEG8
pin20	15	SEG15
pin21	16	SEG16
pin22	19	SEG19
pin23	18	SEG18
pin24	17	SEG17

2.5 Description of Functions Used

In this application note, the output voltage of the 3-V constant-voltage power circuit is trimmed with two methods, one using the A/D converter and another by visual inspection. The following describes the functions used. The details of the bits of each register are given in section 4.3, "Internal Registers Used".

2.5.1 A/D Converter Function

This is a 10-bit A/D converter with a successive approximation method, and can convert analog inputs on up to eight channels.

- A/D result register (ADRR)
  ADRR is a 16-bit read-only register for storing A/D conversion results. Data is stored in the ten higher-order bits of ADRR. ADRR is always readable by the CPU. The ADRR value during A/D conversion is undefined, and after A/D conversion, ten bits of A/D-converted data are stored and held until the next conversion is started. The initial value of ADRR is undefined. This register should be read in a word unit.

- A/D mode register (AMR)
  AMR sets the conversion time for the A/D converter, selects an external trigger, and specifies an analog input pin.

- A/D start register (ADSR)
  ADSR starts or stops A/D conversion.

2.5.2 Timer C Function

Timer C is an 8-bit timer that increments or decrements at each input clock. Timer C has the interval function and auto-reload function.

- Timer mode register C (TMC)
  TMC is an 8-bit readable/writable register that selects the auto-reload function, controls count-up/count-down of timer counter C (TCC), and selects an input clock. For the TCC count-up/count-down control, either hardware control driven by the UD pin input or usage as a software-controlled up-counter or down-counter is selectable. The TMC is initialized to H'10 by a reset.

- Timer counter C (TCC)
  TCC is an 8-bit readable up/down-counter that is incremented or decremented by an input internal clock or an external event. An input clock can be selected from among ten types of clock: the system clock divided by 8192, 2048, 512, 64, 16, and 4, the subclock divided by 1024, 256, and 4, and an external clock. In this sample application, the TCC is configured as a down-counter, and the system clock divided by 64 is selected for the TCC input clock.

- Timer load register C (TLC)
  TLC is an 8-bit write-only register used to set a value to be reloaded to TCC. When a value written to TLC, the value is also loaded to TCC at the same time, and TCC starts counting up or down from that value. When TCC overflows or underflows during auto-reloading operation, the TLC value is loaded to TCC. This allows TCC to overflow/underflow periodically within a range from 1 to 256 cycles of the input clock. TLC is allocated to the same address as TCC and initialized to H'00 by a reset.
  In this sample task, the H'A0 is set to TLC to allow the TCC to underflow in 1.024 ms.

2.5.3 Port E Function

Port E is an input/output port which can also serve as external interrupt input pins, SCI3_2/SCI3_3 input/output pins, or timer C input pins. In this application note, all the pins are configured as input pins.

- Port data register E (PDRE)
  PDRE is a register for storing data for port E. When port E is read while PCRE bits are set to 1, the values stored in PDRE are read regardless of the actual pin states. When port E is read while PCRE bits are cleared to 0, the pin states are read.

- Port control E (PCRE)
  PCRE controls the input/output of port E on a bit-by-bit basis. Setting a PCRE bit to 1 makes the corresponding pin of PE7 to PE0 an output pin, while clearing the bit to 0 makes the pin an input pin. The settings in PCRE and PDRE registers are valid when the corresponding pin is set as a general I/O pin.
  This register is write-only. When it is read, each of its bits is always read as 1.

2.5.4 Watchdog Timer Function

The H8/38099 has an internal watchdog timer (WDT). After a reset, the WDT is turned on. The WDT is an 8-bit timer, and the inside of the H8/38099 is reset when the WDT counter overflows because of the CPU being unable to rewrite the counter value due to a system runaway or other reasons. In this sample task, the watchdog timer function is deactivated because it is not used.

- Timer control/status register WD1 (TCSRWD1)
  TCSRWD1 controls writing to TCSRWD1 itself and to TCWD. TCSRWD1 also controls the operation of the watchdog timer and indicates its operating status. To rewrite this register, use the MOV instruction.
  Bit manipulation instructions cannot be used to change its setting.

2.5.5 Interrupt Controller

This LSI uses the interrupt controller to control interrupts.

- Interrupt enable register 2 (IENR2)
  IENR2 enables interrupt requests related to direct transitions, A/D converter, timer G, timer F, timer C, and asynchronous event counter.

- Interrupt request register 2 (IRR2)
  IRR2 indicates the status of the interrupt requests related to direct transitions, A/D converter, timer G, timer F, timer C, and asynchronous event counter.

2.6 Assignment of Functions

Table 3 lists the function assignment of this sample application. With the functions assigned as shown in table 3, trimming of the output voltage of the 3-V constant-voltage power circuit is performed.

Table 3 Assignment of Functions

Elements	Assignment of functions
LPCR	Selects a duty cycle, and selects between LCD driver pin function and port pin function.
LCR	Controls turning on/off the LCD driving power supply, starting of the display function, and display data, and selects a frame frequency.
LCR2	Controls the switching between waveforms A and B, selects a step-up clock for the 3-V constant-voltage power circuit, selects whether to connect or disconnect the LCD power-supply split resistor to/from the LCD driving power supply, and turns on or off the 3-V constant-voltage power circuit.
LTRMR	Adjusts the 3-V constant-voltage for use as the LCD driving power supply.
BGRMR	Controls running and stopping of the BGR.
SEG1 to SEG20	Used as segment drivers.
COM1 to COM4	Used as common drivers.
LCD RAM	Used to set display data for the LCD.
ADRR	Stores A/D conversion results.
AMR	Sets the conversion time for the A/D converter to 124 states and specify analog input channel AN0.
ADSR	Starts or stops the A/D converter.
TMC	Selects the auto reload function, controls the counting up and down of the counter, and selects ϕ/64 as the input clock.
TLC	Sets the value to be reloaded to TCC.
TCC	8-bit counter that takes the system clock divide by 64 as input.
PDRE	Register for storing port E data.
PCRE	Sets port E as an input pin.
IENTC	Enables timer C interrupt requests.
IRRTC	Indicates whether a timer C interrupt has been requested.
TCSRWD1	Stops the watchdog timer.

3. Principles of Operation

3.1 Automatic Trimming Method Using the A/D Converter

The automatic trimming method using the A/D converter is described below.

1. After the timer C interrupt handling is started, A/D conversion is executed.
2. The value of ADDR is shifted by 6 bits to the right, and is compared with 1.25 V (H'0183), which is the lower limit that can be adjusted with the LCD trimming register. When it is 1.25 V or less, the maximum adjustable register value H'8B is written to the LCD trimming register and timer C interrupts are disabled. When it is greater than 1.25 V, the method proceeds to the next step.
3. The value of ADDR is shifted by 6 bits to the right, and is compared with 2.69 V (H'0342), which is the upper limit that can be adjusted with the LCD trimming register. When it is 2.69 V or greater, the minimum adjustable register value H'7C is written to the LCD trimming register, and timer C interrupts are disabled. When it is less than 2.69 V, the method proceeds to the next step.
4. The value of ADDR is shifted by 6 bits to the right, and is checked whether it is in the range of 1.25 V to 1.90 V (H'024D). When it is in the range, the currently set register value plus 0.03 V is written to the LCD trimming register. When it is not in the range, the method proceeds to the next step.
5. The value of ADDR is shifted by 6 bits to the right, and is checked whether it is in the range of 2.10 V (H'028B) to 2.69 V. When it is in the range, the currently set register value minus 0.03 V is written to the LCD trimming register. When it is not in the range, the method proceeds to the next step.
6. The value of ADRR is shifted by 6 bits to the right; when it is 1.90 V to 2.10 V, trimming is considered unnecessary and timer C interrupts are disabled.
7. Perform trimming by repeating steps 1 to 6 above at intervals of 1.024 ms, which is the period of the timer C interrupt.

3.2 Trimming Method for Visual Inspection

The trimming method for visual inspection is described below.

1. After the timer C interrupt handling is started, the value of port data register E is compared with DATA stored in the RAM area.
2. When DATA does not match the value of port data register E, the value of port data register E is stored in DATA and also written to the LCD trimming register. Then, CNT, which is an up-counter in memory that is incremented when DATA matches the value of port data register E, is cleared to H'0000.
3. When DATA matches the value of port data register E, CNT is incremented. When the value of CNT matches H'E4E2 at this time, it is assumed that the rotary DIP switch has not been operated for one minute and trimming is decided to have ended, then timer C interrupts are disabled.
4. Port data register E is read at intervals of 1.024 ms.

3.3 Description of Program Operation

A description of program operation is given in figure 7. Trimming is performed through the hardware and software processing shown in figure 7.

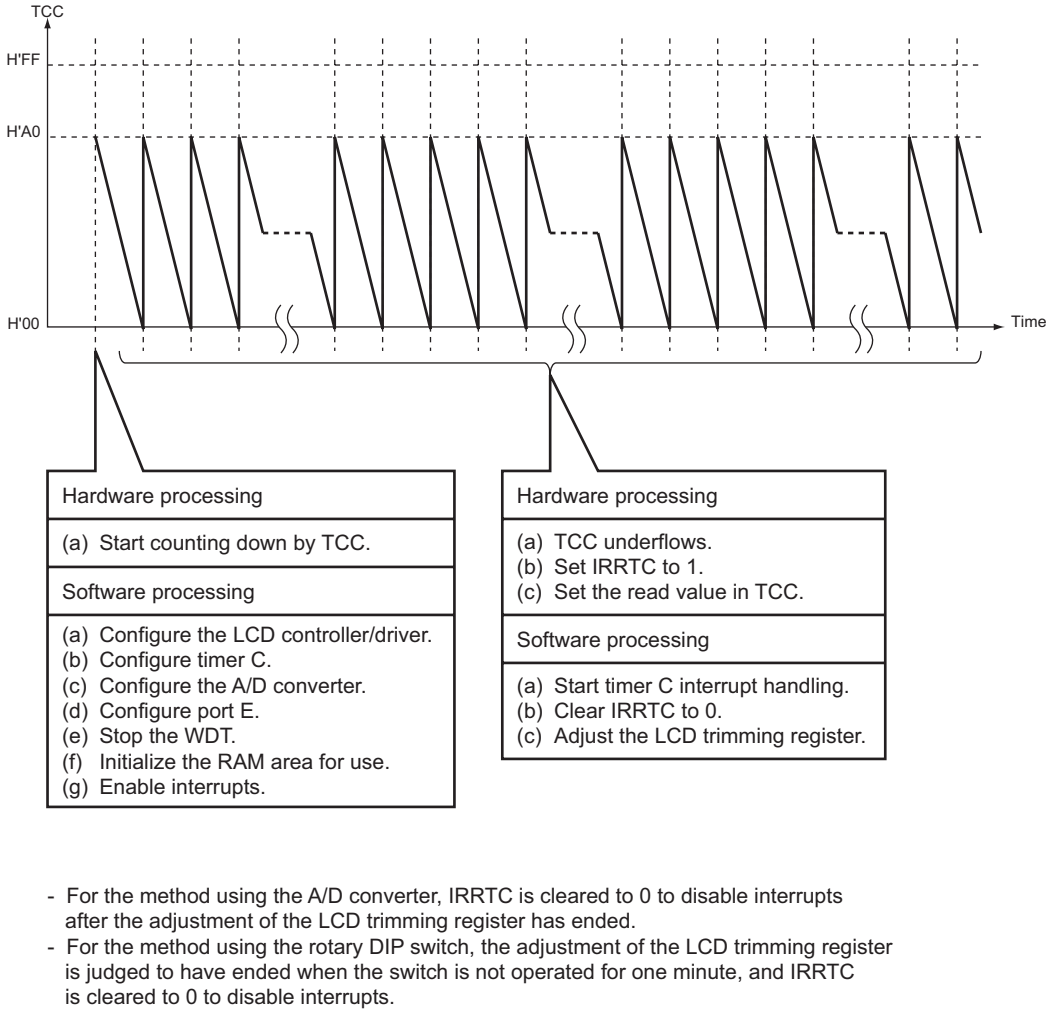


Figure 7 Trimming the Output Voltage of the 3-V Constant-Voltage Power Circuit Using the A/D Converter

4. Description of Software

4.1 Modules

Table 4 lists the modules of this application note.

Table 4 Description of Modules

Module Name	Label Name	Description
Main routine	main	Initializes the LCD controller/driver, LCD RAM, A/D converter, timer C, and port E, configures the 3-V constant-voltage power circuit, sets LCD display data, sets timer C interrupts, and stops the watchdog timer.
Timer C interrupt	tcint	Handles timer C interrupts. For the method using A/D conversion: Starts the A/D conversion of the V2 pin voltage, compares the A/D conversion results, and reflects them in the LCD trimming register. For the method using the rotary DIP switch: Reflects the value of port data register E in the LCD trimming register.

4.2 Arguments

No arguments are used in this application note.

4.3 Internal Registers Used

The following tables describe the internal registers used in this application note.

- LCD Port Control Register (LPCR) Address: H'FFFFA0

Bit	Bit Name	Initial Value	Setting Value	R/W	Description
7	DTS1	0	1	R/W	Duty Cycle Select 1 and 0
6	DTS0	0	1	R/W	Common Function Select
5	CMX	0	0	R/W	With a DTS1 and DTS0 combination, select a duty cycle from among static and 1/2 to 1/4. CMX selects whether the common output pins not in use are made to output the same waveform as that output from the common output pins in use to increase the common drive capability. DTS1 = 1, DTS2 = 1, CMX = X: The duty cycle is set to 1/4, and COM1 to COM4 are set as common driver pins.
3	SGS3	0	0	R/W	Segment Driver Pin Select 3 to 0
2	SGS2	0	1	R/W	Selects the segment driver pins for use.
1	SGS1	0	0	R/W	SGS3 = 0, SGS2 = 1, SGS1 = 0, SGS0 = 1: SEG1 to SEG20 are set as segment driver pins.
0	SGS0	0	1	R/W	

Legend:
X: Don't care

- LCD Control Register (LCR) Address: H'FFFFA1

Bit	Bit Name	Initial Value	Setting Value	R/W	Description
6	PSW	0	1	R/W	LCD Driving Power Supply Control In power-down modes, in which LCD display is not required, or when an external power is used, the LCD driving power supply can be turned off. When the ACT bit is set to 0 or the chip is put in standby mode, the LCD driving power supply is turned off regardless of the setting of this bit. 0: LCD driving power supply is off. 1: LCD driving power supply is on.
5	ACT	0	1	R/W	Display Function Start Selects whether to use the LCD controller/driver. Clearing this bit to 0 causes the LCD controller/driver to stop operation. The LCD driving power is also turned off regardless of the value of PSW. Note, however, that the contents of the register are retained. 0: LCD controller/driver is stopped. 1: LCD controller/driver runs.
4	DISP	0	1	R/W	Display Data Control Selects whether to display the contents of LCD RAM or display blank data regardless of the contents of LCD RAM. 0: Blank data is displayed. 1: LCD RAM data is displayed.
3	CKS3	0	0	R/W	Frame Frequency Select 3 to 0 These bits select the clock to be used and a frame frequency. Note that in sub-active mode, watch mode, and sub-sleep mode, the system clock (ϕ) is stopped and thus when one of $\phi/2$ to $\phi/256$ is selected, display operation is not performed. To perform LCD display in these modes, be sure to select one of ϕ_W, $\phi_W/2$, and $\phi_W/4$ as the clock to be used. CKS3 = 0, CKS2 = X, CKS1 = 0, CKS0 = 1: Clock to be used = $\phi_W/2$, frame frequency = 64 Hz (frame frequency when ϕ_W = 32.768 kHz)
2	CKS2	0	0	R/W	
1	CKS1	0	0	R/W	
0	CKS0	0	1	R/W	

Legend:
X: Don't care

- LCD Control Register 2 (LCR2) Address: H'FFFFA2

Bit	Bit Name	Initial Value	Setting Value	R/W	Description
7	LCDAB	0	0	R/W	Waveform A/B Switching Control Selects waveform A or waveform B for LCD driving. 0: Drive with waveform A. 1: Drive with waveform B.
6	HCKS	0	0	R/W	Clock Select for Stepping Up by 3-V Constant-Voltage Circuit Selects the step-up clock for use by the 3-V constant-voltage power supply circuit. The step-up clock is the clock selected by the CKS3 to CKS0 bits of LCR divided by four or eight. 0: Step-up clock is the clock used for the LCD divided by four. 1: Step-up clock is the clock used for the LCD divided by eight.
5	CHG	0	1	R/W	LCD Power-Supply Split Resistor Connection Control Selects whether to connect the LCD power-supply split resistor to the LCD driving power supply. 0: Disconnected. 1: Connected.
4	SUPS	0	1	R/W	3-V Constant-Voltage Power Control In power-down modes, in which LCD display is not required, or when an external power is used, the 3-V constant-voltage power supply circuit can be turned off. In standby mode or when the BGRSTPN bit of BGRMR is cleared to 0, the 3-V constant-voltage power supply circuit is turned off regardless of the setting of this bit. 0: 3-V constant-voltage power circuit is turned off. 1: 3-V constant-voltage power circuit is turned on.

- LCD Trimming Register (LTRMR) Address: H'FFFFA3

Bit	Bit Name	Initial Value	Setting Value	R/W	Description
7	TRM3	0	*3	R/W	Output Voltage Adjustment of 3-V Constant-Voltage
6	TRM2	0	*3	R/W	Power Supply Circuit *1*2
5	TRM1	0	*3	R/W	By adjusting the reference voltage to generate the
4	TRM0	0	*3	R/W	3-V constant-voltage, the LCD driving power supply can be adjusted to 3 V. Set this register so that the voltage on the V1 pin is 3 V. 0000: ±0V 1000: +0.48V 0001: –0.06V 1001: +0.42V 0010: –0.12V 1010: +0.36V 0011: –0.15V 1011: +0.30V 0100: –0.21V 1100: +0.24V 0101: –0.24V 1101: +0.18V 0110: –0.30V 1110: +0.12V 0111: –0.33V 1111: +0.06V
2	CTRM2	0	*3	R/W	Variable Voltage Adjustment of 3-V Constant-Voltage
1	CTRM1	0	*3	R/W	Power Supply *1*2
0	CTRM0	0	*3	R/W	The LCD driving power adjusted by the TMR bits can be further adjusted. When the LCD panel does not display normally due to the temperature conditions when the LCD is used or for other reasons, set these bits for adjustment. 000: ±0V 001: +0.09V 010: +0.18V 011: +0.27V 100: –0.36V 101: –0.27V 110: –0.18V 111: –0.09V

Notes: *1. This is an approximate value, and does not guarantee the voltage value. Use it as a rough guide.

*2. The LCD trimming register should be set in the following way.

V1 voltage when the initial value is set: A
TRM3 to TRM0 of the LTRMR register: B
CTRM2 to CTRM0 of the LTRMR register: C

When defined as above, the voltages after trimming are roughly determined by the formulas below.

V1 voltage = A + B + C
V2 voltage = (A + B + C) × 2/3
V3 voltage = (A + B + C) ÷ 3

After monitoring voltage A, set B and C so that the V1 voltage becomes 3 V.

*3. These bits are set accordingly by the program.

- BGR Control Register (BGRMR) Address: H'FFFFA4

Bit	Bit Name	Initial Value	Setting Value	R/W	Description
7	BGRSTPN	0	1	R/W	Band Gap Reference Circuit Control Controls running and stopping of the band gap reference circuit. 0: Band gap reference circuit is stopped. 1: Band gap reference circuit runs.
2	BTRM2	0	0	R/W	BGR Output Voltage Trimming
1	BTRM1	0	0	R/W	Adjust the BGR output voltage of about 1.2 V.
0	BTRM0	0	0	R/W	000: ±0V 001: +0.14V 010: +0.09V 011: +0.04V 100: –0.04V 101: –0.09V 110: –0.14V 111: –0.18V

- A/D Result Register (ADRR) Address: H'FFFFBC

Bit	Bit Name	Initial Value	Setting Value	R/W	Description
15	ADR9	Undefined	Undefined	R	ADRR is a 16-bit read-only register for storing A/D conversion results. Data is stored in the ten higher-order bits of ADRR. ADRR is always readable by the CPU. The ADRR value during A/D conversion is undefined, and after A/D conversion, ten bits of A/D-converted data are stored and held until the next conversion is started. The initial value of ADRR is undefined. This register should be read in a word unit.
14	ADR8	Undefined	Undefined	R	
13	ADR7	Undefined	Undefined	R	
12	ADR6	Undefined	Undefined	R	
11	ADR5	Undefined	Undefined	R	
10	ADR4	Undefined	Undefined	R	
9	ADR3	Undefined	Undefined	R	
8	ADR2	Undefined	Undefined	R	
7	ADR1	Undefined	Undefined	R	
6	ADR0	Undefined	Undefined	R	
5	—	—	—	—	
4	—	—	—	—	
3	—	—	—	—	
2	—	—	—	—	
1	—	—	—	—	
0	—	—	—	—	

- A/D Mode Register (AMR) Address: H'FFFFBE

Bit	Bit Name	Initial Value	Setting Value	R/W	Description
5	CKS1	0	0	R/W	Clock Select
4	CKS0	0	0	R/W	Selects the clock source for A/D conversion. 00: φ/8 (Conversion time = 124 states (max.)* 01: φ/4 (Conversion time = 62 states (max.)* 10: φ/2 (Conversion time = 31 states (max.)* 11: None selected (setting prohibited)
3	CH3	0	0	R/W	Channel Select 3 to 0
2	CH2	0	1	R/W	Selects an analog input channel.
1	CH1	0	0	R/W	00XX: None selected
0	CH0	0	0	R/W	0100: AN0 0101: AN1 0110: AN2 0111: AN3 1000: AN4 1001: AN5 1010: AN6 1011: AN7 11XX: Setting prohibited When changing the channel selection, ADSF must be cleared to 0.

Legend:
X: Don't care
Note: * When the reference clock is φ

- A/D Start Register (ADSR) Address: H'FFFFBF

Bit	Bit Name	Initial Value	Setting Value	R/W	Description
7	ADSF	0	0/1	R/W	Setting this bit to 1 causes A/D conversion to start. After the conversion has ended, the converted data is set in ADRR and this bit is cleared to 0 at the same time. A/D conversion can be forcibly terminated by writing 0 to this bit.

- Timer Mode Register C (TMC) Address: H'FFFFB4

Bit	Bit Name	Initial Value	Setting Value	R/W	Description
7	TMC7	0	1	R/W	Auto Reload Function Select Selects the timer C auto reload function. 0: Interval function is selected. 1: Auto reload function is selected.
6	TMC6	0	0	R/W	Counter Up/Down Control
5	TMC5	0	1	R/W	Selects whether TCC is to count up/down by hardware control with UD pin input and whether it is to be an up or down counter. 00: TCC is an up counter. 01: TCC is a down counter. 1X: Hardware control with UD pin input. UD pin input at high level: Down counter. UD pin input at low level: Up counter.
3	TMC3	0	0	R/W	Clock Select
2	TMC2	0	0	R/W	TMC3 to TMC0 select the clock to be input to TCC. For an external event input, it is possible to select between rising and falling edges. X000: Count with the internal clock ϕ/8192. X001: Count with the internal clock ϕ/2048. X010: Count with the internal clock ϕ/512. X011: Count with the internal clock ϕ/64. X100: Count with the internal clock ϕ/16. 0101: Count with the internal clock ϕ/4. 0110: Count with the internal clock ϕ_W/1024. 1101: Count with the internal clock ϕ_W/256. 1110: Count with the internal clock ϕ_W/4. 0111: Count at a falling edge of an external event (TMIC)* 1111: Count at a rising edge of an external event (TMIC)*
1	TMC1	0	1	R/W	
0	TMC0	0	1	R/W	

Legend:
X: Don't care
Note: * Before setting TMC3 to TMC0 to B'X111, be sure to set TMIC of port mode register E (PMRE) to 1.

- Timer Counter C (TCC) Address: H'FFFFB5

Bit	Bit Name	Initial Value	Setting Value	R/W	Description
7	TCC7	0	—	R	TCC is an 8-bit readable up-/down-counter that is incremented or decremented by an input internal clock or an external event. The clock to be input to TCC is selected by the TMC3 to TMC0 bits in TMC. The value of TCC can always be read from the CPU. When TCC overflows (H'FF → H'00 or H'FF → TLC value) or underflows (H'00 → H'FF or H'00 → TLC value), IRRTC in IRR2 is set to 1. TCC is allocated to the same address as TLC and is initialized to H'00 by a reset.
6	TCC6	0	—	R	
5	TCC5	0	—	R	
4	TCC4	0	—	R	
3	TCC3	0	—	R	
2	TCC2	0	—	R	
1	TCC1	0	—	R	
0	TCC0	0	—	R	

- Timer Load Register (TLC) Address: H'FFFFB5

Bit	Bit Name	Initial Value	Setting Value	R/W	Description
7	TLC7	0	0	W	TLC is an 8-bit write-only register used to set a value to be reloaded to TCC. When a value written to TLC, the value is also loaded to TCC at the same time, and TCC starts counting up or down from that value. When TCC overflows or underflows during auto-reloading operation, the TLC value is loaded to TCC. This allows TCC to overflow/underflow periodically within a range from 1 to 256 cycles of the input clock. TLC is allocated to the same address as TCC and initialized to H'00 by a reset.
6	TLC6	0	0	W	
5	TLC5	0	0	W	
4	TLC4	0	0	W	
3	TLC3	0	0	W	
2	TLC2	0	0	W	
1	TLC1	0	0	W	
0	TLC0	0	0	W	

- Port Data Register E (PDRE) Address: H'FFF033

Bit	Bit Name	Initial Value	Setting Value	R/W	Description
7	PE7	0	*	R/W	When port E (this register) is read when the corresponding bit of the PCRE register is 1 (output pin), the value of PDRE is directly read. The pin state therefore has no effect on reading. When port E is read when PCRE is 0 (input pin), the pin state is read.
6	PE6	0	*	R/W	
5	PE5	0	*	R/W	
4	PE4	0	*	R/W	
3	PE3	0	*	R/W	
2	PE2	0	*	R/W	
1	PE1	0	*	R/W	
0	PE0	0	*	R/W	

Note *: In this application, all port E pins are specified as input pins, so the pin states are reflected in these bits.

- Port Control Register E (PCRE) Address: H'FFF037

Bit	Bit Name	Initial Value	Setting Value	R/W	Description
7	PCRE7	0	0	R	Setting a PCRE bit to 1 makes the corresponding pin (PE7 to PE0) an output pin, while clearing the bit to 0 makes the pin an input pin. The settings in PCRE and PDRE registers are valid when the corresponding pin is set as a general I/O pin. This register is write-only. When it is read, each of its bits is always read as 1.
6	PCRE6	0	0	R	
5	PCRE5	0	0	R	
4	PCRE4	0	0	R	
3	PCRE3	0	0	R	
2	PCRE2	0	0	R	
1	PCRE1	0	0	R	
0	PCRE0	0	0	R	

- Interrupt Enable Register 2 (IENR2) Address: H'FFFFF4

Bit	Bit Name	Initial Value	Setting Value	R/W	Description
1	IENTC	0	1	R/W	Timer C Interrupt Enable Setting this bit to 1 enables timer C interrupt requests.

- Interrupt Request Flag Register 2 (IRR2) Address: H'FFFFF7

Bit	Bit Name	Initial Value	Setting Value	R/W	Description
1	IRRTC	0	0/1	R/W	Timer C Interrupt Request Flag [Setting condition] • Timer C overflows or underflows [Clearing condition] • Writing 0

- Timer Control/Status Register WD1 (TCSRWD1) Address: H'FFFFB1

Bit	Bit Name	Initial Value	Setting Value	R/W	Description
7	B6WI	1	1	R/W	Bit 6 Write Disable Writing to bit 6 of this register is enabled only when 0 is written to this bit. This bit is always read as 1.
6	TCWE	0	0	R/W	Timer Counter W Write Enable Writing to TCWD is enabled when this bit is set to 1. When writing to this bit, 0 must be written to bit 7.
5	B4WI	1	*	R/W	Bit 4 Write Disable Writing to bit 4 of this register is enabled only when 0 is written to this bit. This bit is always read as 1.
4	TCSRWE	0	*	R/W	Timer Control/Status Register W Write Enable Writing to bits 2 and 0 of this register is enabled when this bit is set to 1. When writing to this bit, 0 must be written to bit 5.
3	B2WI	1	*	R/W	Bit 2 Write Disable Writing to bit 2 of this register is enabled only when 0 is written to this bit. This bit is always read as 1.
2	WDON	1	*	R/W	Watchdog Timer On Setting this bit to 1 causes TCWD to start counting up. Clearing it to 0 causes TCWD to stop counting up. [Clearing condition] • 0 is written to B2WI and WDON while TCSRWE is 1. [Setting conditions] • A reset is made. • 0 is written to B2WI and 1 is written to WDON while TCSRWE is 1.
1	B0WI	1	1	R/W	Bit 0 Write Disable Writing to bit 0 of this register is enabled only when 0 is written to this bit. This bit is always read as 1.
0	WRST	0	0	R/W	Watchdog Timer Reset [Clearing conditions] • A reset is made with the $\overline{\text{RES}}$ pin. • 0 is written to B0WI and WRST while TCSRWE is 1. [Setting condition] • TCWD overflows and an internal reset signal is generated.

Note: * These bits are manipulated so as to stop the watchdog timer. See the flowchart for the main routine.

4.4 RAM Usage

The RAM usage in this application note is given in table 5.

Table 5 RAM Usage

Type	Label Name	Description	Used In
unsigned char	REVDAT	Indicates the array number of the voltage adjustment values for the LCD trimming register.	main, tcint
unsigned short	CNT	Incremented when the value of DATA matches the value in port data register E. When CNT is H'E4E2, the rotary DIP switch is judged not to have been operated for one minute.	main, tcint
unsigned char	DATA	Stores the value of port data register E.	main, tcint

4.5 Description of Constants

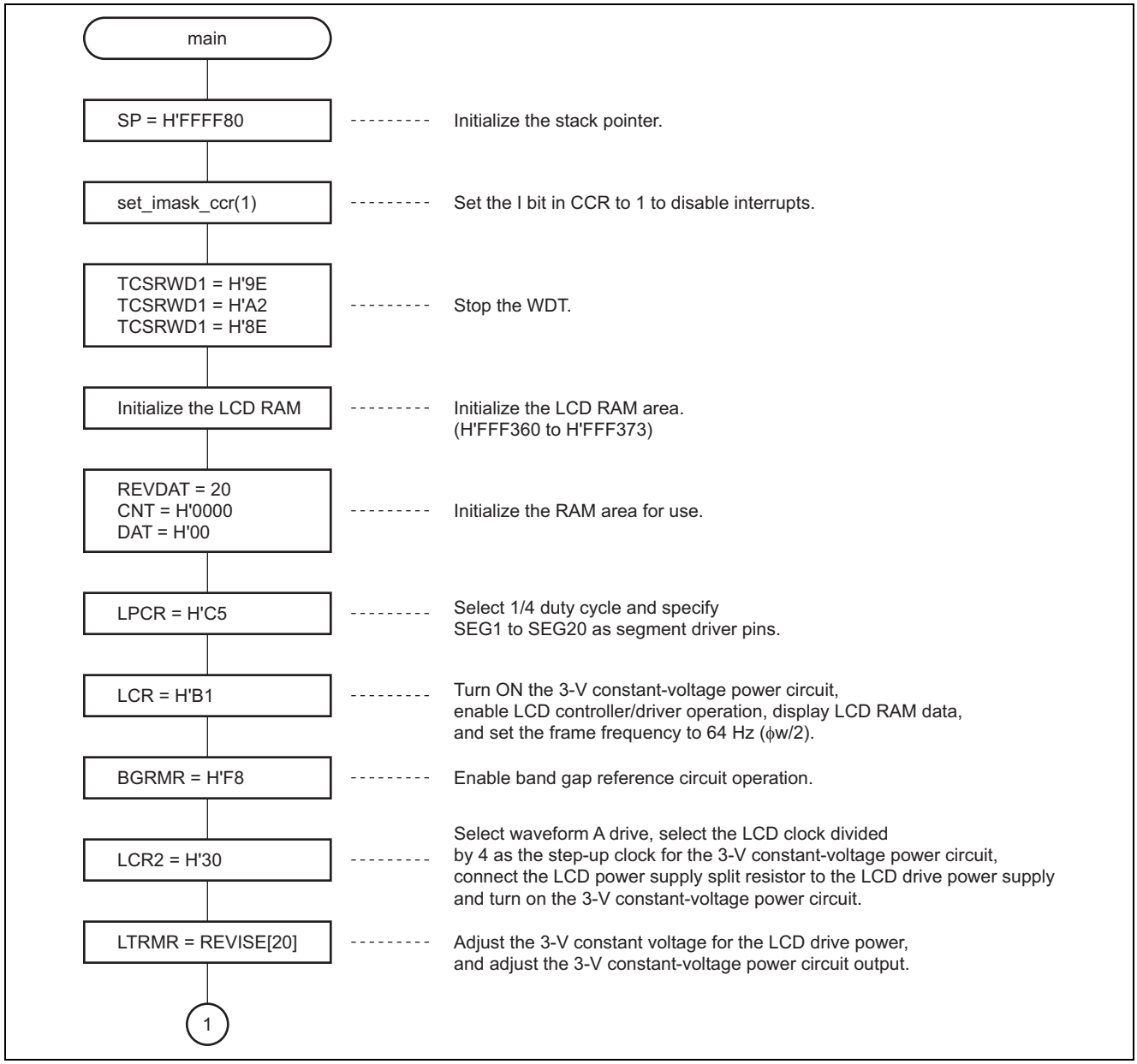
The constants used in this application note are given in table 6.

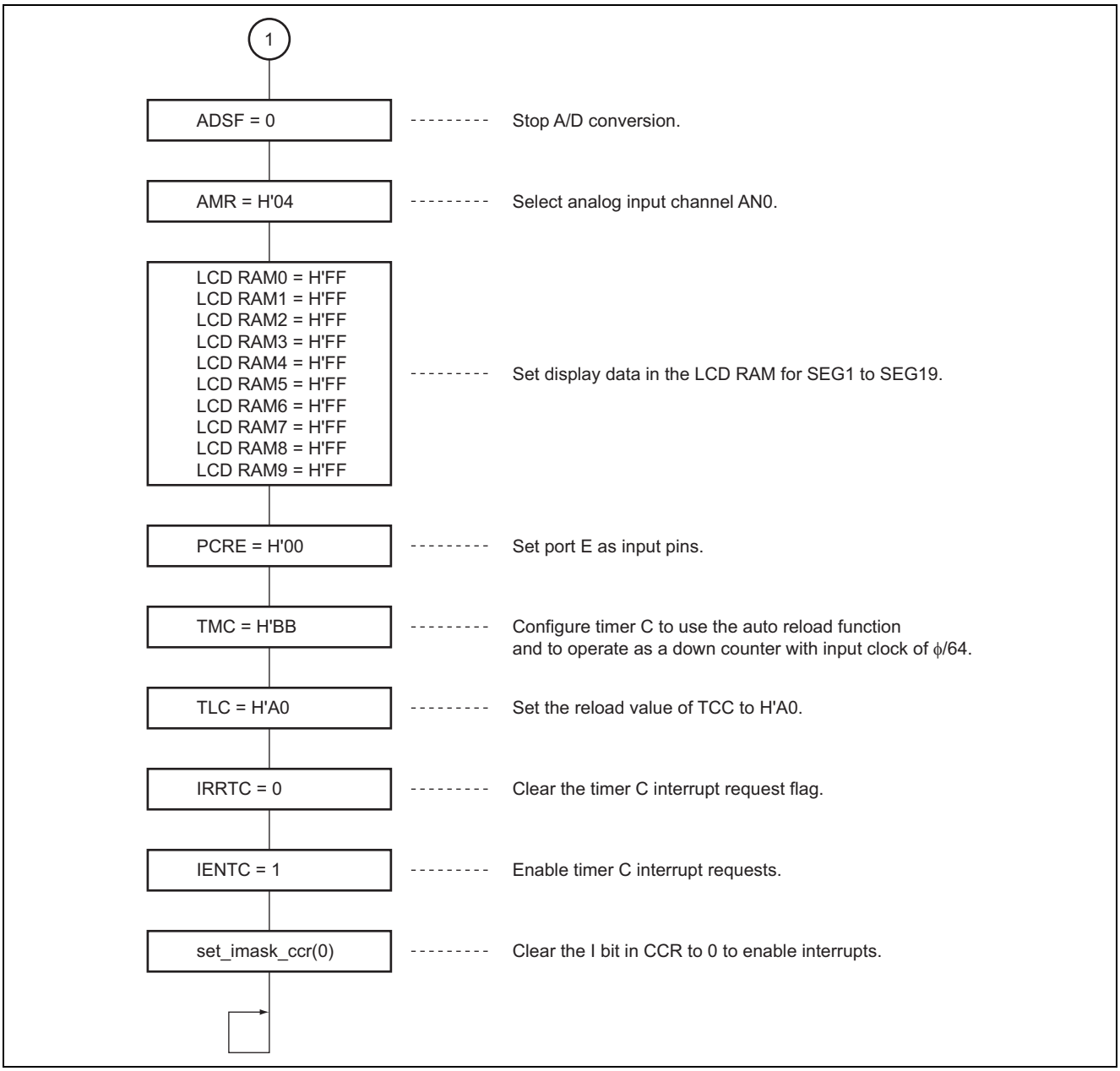
Table 6 Constants Used

Buffer Name	Constant Value	Description (voltage adjustment value for the LCD trimming register)	Used In
REVISE[0]	H'7C	–0.69V V3 voltage adjustment	main, tcint
REVISE[1]	H'6C	–0.66V V3 voltage adjustment	
REVISE[2]	H'7D	–0.60V V3 voltage adjustment	
REVISE[3]	H'6D	–0.57V V3 voltage adjustment	
REVISE[4]	H'3C	–0.51V V3 voltage adjustment	
REVISE[5]	H'6E	–0.48V V3 voltage adjustment	
REVISE[6]	H'1C	–0.42V V3 voltage adjustment	
REVISE[7]	H'6F	–0.39V V3 voltage adjustment	
REVISE[8]	H'0C	–0.36V V3 voltage adjustment	
REVISE[9]	H'78	–0.33V V3 voltage adjustment	
REVISE[10]	H'68	–0.30V V3 voltage adjustment	
REVISE[11]	H'0D	–0.27V V3 voltage adjustment	
REVISE[12]	H'58	–0.24V V3 voltage adjustment	
REVISE[13]	H'48	–0.21V V3 voltage adjustment	
REVISE[14]	H'0E	–0.18V V3 voltage adjustment	
REVISE[15]	H'38	–0.15V V3 voltage adjustment	
REVISE[16]	H'28	–0.12V V3 voltage adjustment	
REVISE[17]	H'0F	–0.09V V3 voltage adjustment	
REVISE[18]	H'18	–0.06V V3 voltage adjustment	
REVISE[19]	H'FF	–0.03V V3 voltage adjustment	
REVISE[20]	H'08	±0.00V V3 voltage adjustment	
REVISE[21]	H'19	+0.03V V3 voltage adjustment	
REVISE[22]	H'F8	+0.06V V3 voltage adjustment	
REVISE[23]	H'09	+0.09V V3 voltage adjustment	
REVISE[24]	H'E8	+0.12V V3 voltage adjustment	
REVISE[25]	H'F9	+0.15V V3 voltage adjustment	
REVISE[26]	H'D8	+0.18V V3 voltage adjustment	
REVISE[27]	H'E9	+0.21V V3 voltage adjustment	
REVISE[28]	H'C8	+0.24V V3 voltage adjustment	
REVISE[29]	H'D9	+0.27V V3 voltage adjustment	
REVISE[30]	H'B8	+0.30V V3 voltage adjustment	
REVISE[31]	H'C9	+0.33V V3 voltage adjustment	
REVISE[32]	H'A8	+0.36V V3 voltage adjustment	
REVISE[33]	H'B9	+0.39V V3 voltage adjustment	
REVISE[34]	H'98	+0.42V V3 voltage adjustment	
REVISE[35]	H'A9	+0.45V V3 voltage adjustment	
REVISE[36]	H'88	+0.48V V3 voltage adjustment	
REVISE[37]	H'99	+0.51V V3 voltage adjustment	
REVISE[38]	H'AA	+0.54V V3 voltage adjustment	
REVISE[39]	H'89	+0.57V V3 voltage adjustment	
REVISE[40]	H'9A	+0.60V V3 voltage adjustment	
REVISE[41]	H'AB	+0.63V V3 voltage adjustment	
REVISE[42]	H'8A	+0.66V V3 voltage adjustment	
REVISE[43]	H'9B	+0.69V V3 voltage adjustment	
REVISE[44]	H'8B	+0.75V V3 voltage adjustment	

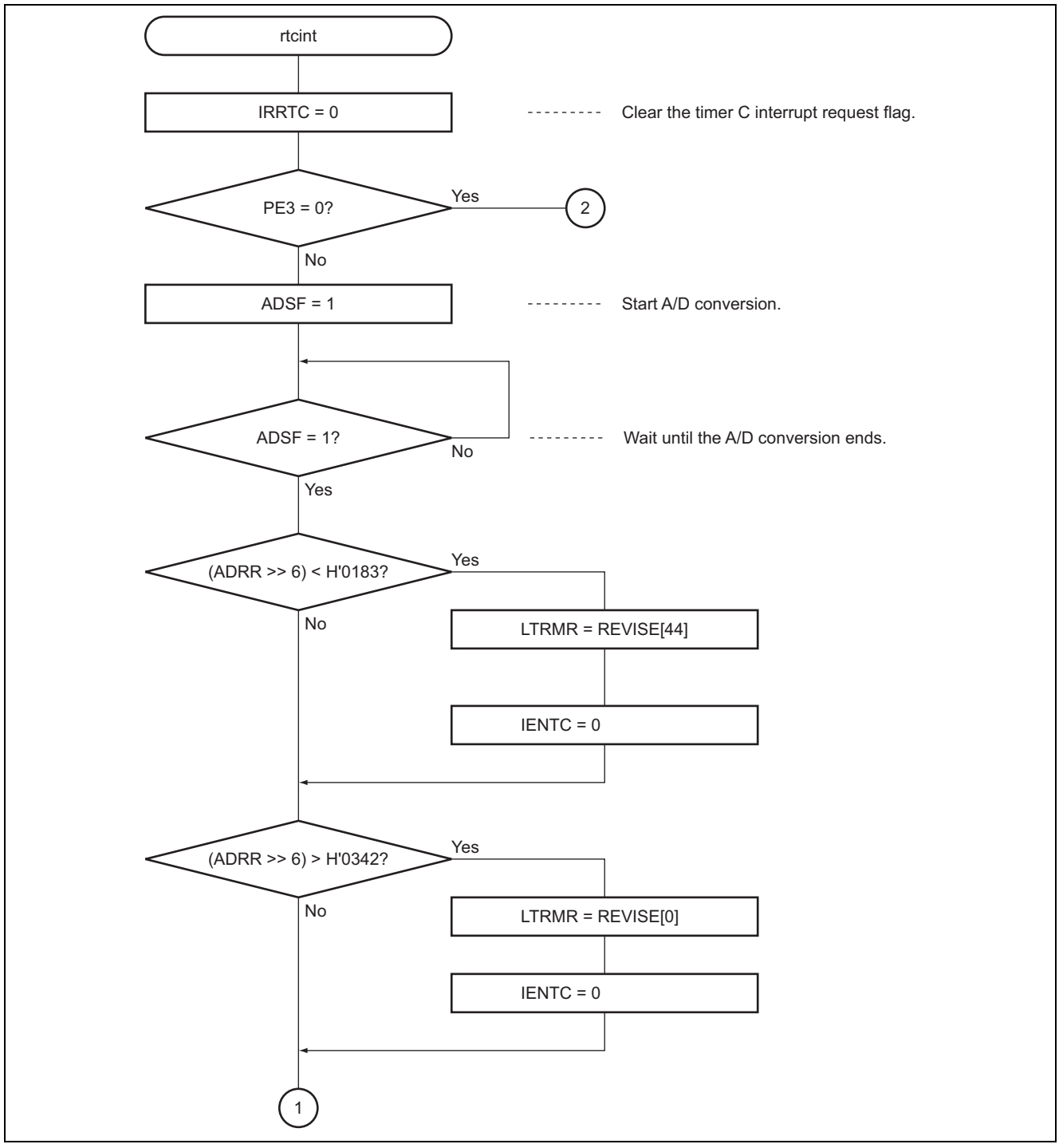
5. Flowcharts

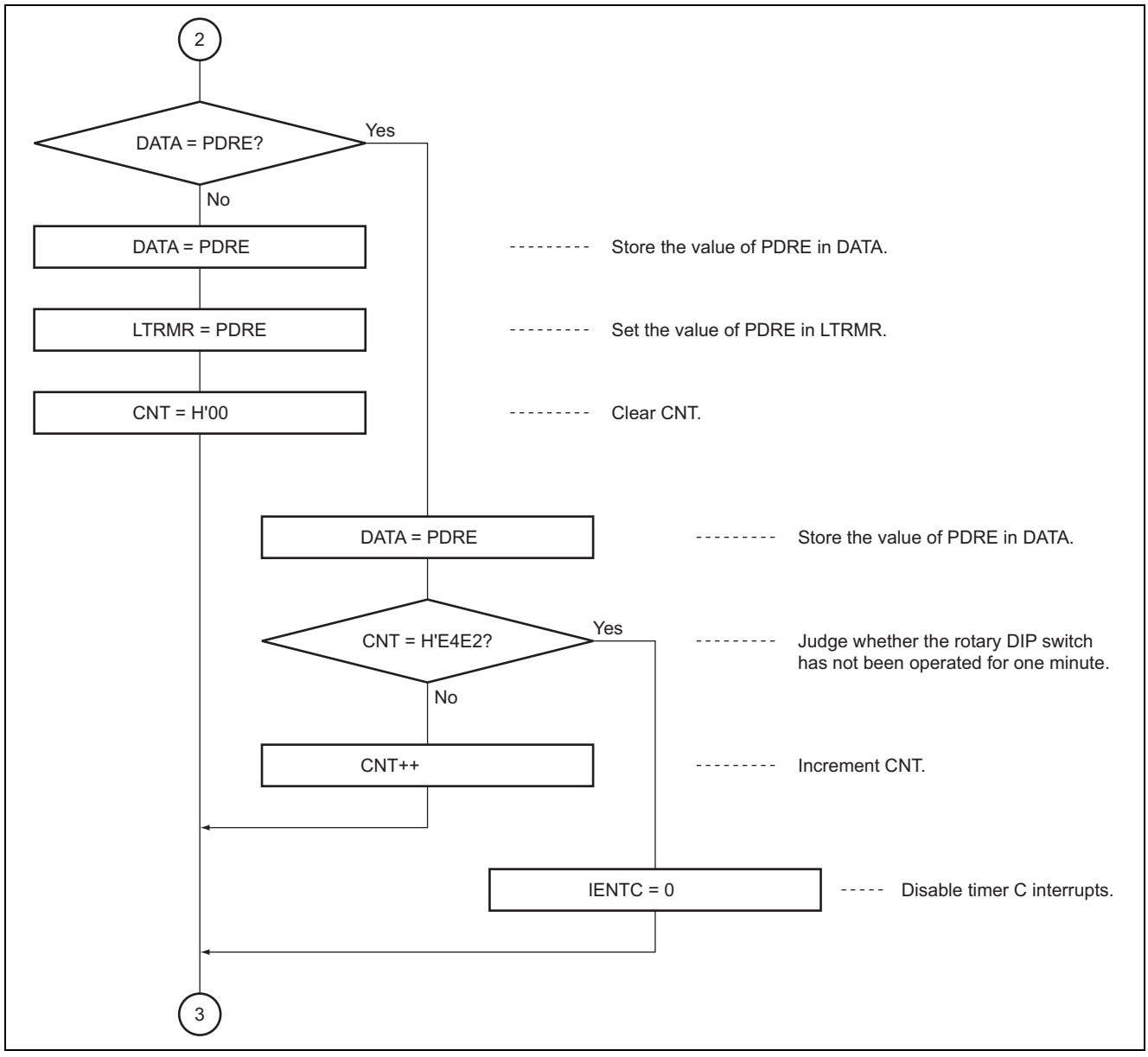
5.1 main Function

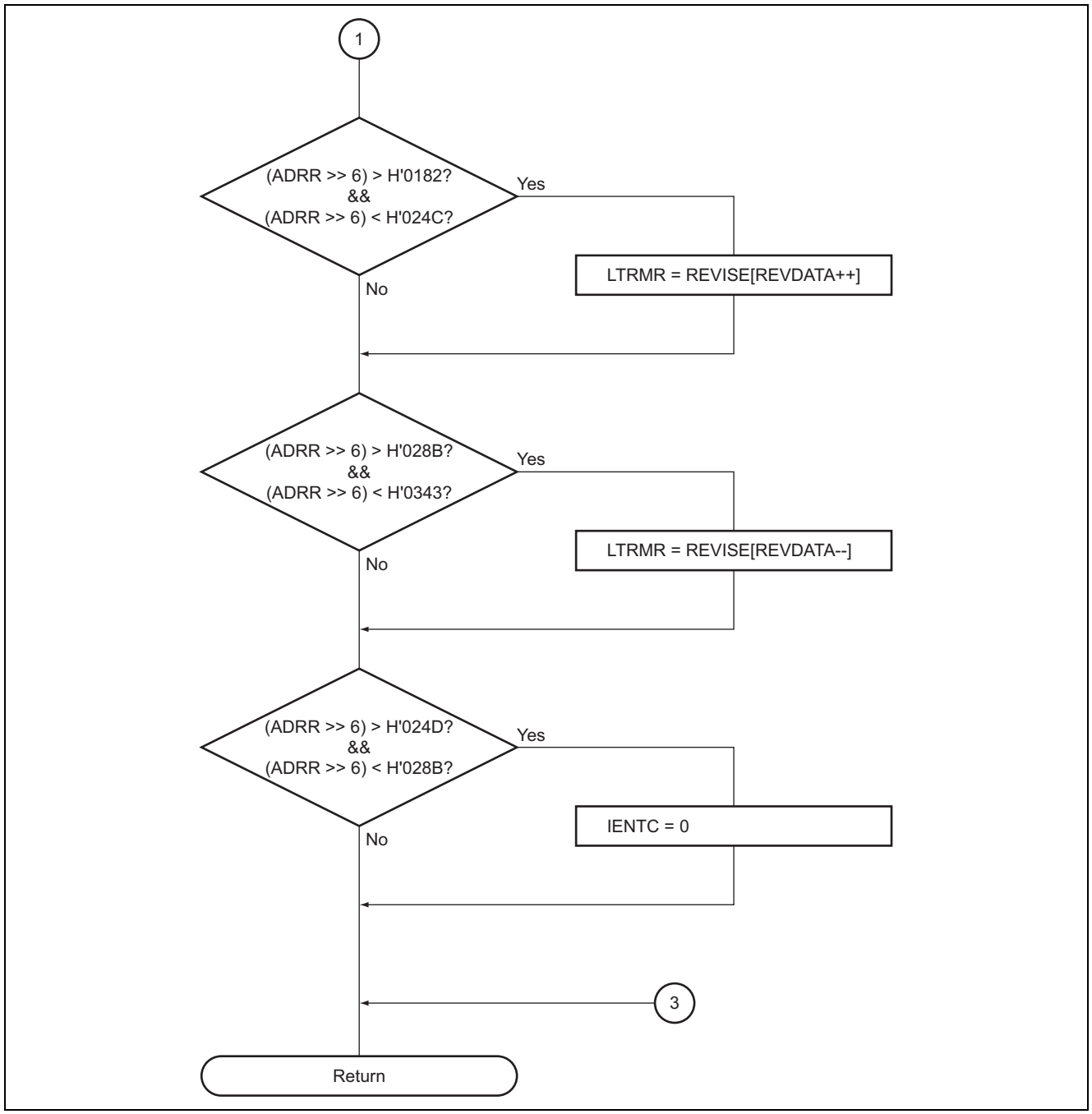



1
ADSF = 0
Stop A/D conversion.
AMR = H'04
Select analog input channel AN0.
LCD RAM0 = H'FF
LCD RAM1 = H'FF
LCD RAM2 = H'FF
LCD RAM3 = H'FF
LCD RAM4 = H'FF
LCD RAM5 = H'FF
LCD RAM6 = H'FF
LCD RAM7 = H'FF
LCD RAM8 = H'FF
LCD RAM9 = H'FF
Set display data in the LCD RAM for SEG1 to SEG19.
PCRE = H'00
Set port E as input pins.
TMC = H'BB
Configure timer C to use the auto reload function
and to operate as a down counter with input clock of ϕ/64.
TLC = H'A0
Set the reload value of TCC to H'A0.
IRRTC = 0
Clear the timer C interrupt request flag.
IENTC = 1
Enable timer C interrupt requests.
set_imask_ccr(0)
Clear the I bit in CCR to 0 to enable interrupts.

5.2 tcint Function




2
DATA = PDRE?
Yes
No
DATA = PDRE
Store the value of PDRE in DATA.
LTRMR = PDRE
Set the value of PDRE in LTRMR.
CNT = H'00
Clear CNT.
DATA = PDRE
Store the value of PDRE in DATA.
CNT = H'E4E2?
Yes
No
Judge whether the rotary DIP switch has not been operated for one minute.
CNT++
Increment CNT.
IENTC = 0
Disable timer C interrupts.
3


1
(ADRR >> 6) > H'0182?
&&
(ADRR >> 6) < H'024C?
Yes
LTRMR = REVISE[REVDATA++]
No
(ADRR >> 6) > H'028B?
&&
(ADRR >> 6) < H'0343?
Yes
LTRMR = REVISE[REVDATA--]
No
(ADRR >> 6) > H'024D?
&&
(ADRR >> 6) < H'028B?
Yes
IENTC = 0
No
3
Return

6. Link Address Specifications

Section Name	Address
CV1	H'000000
CV2	H'0000D4
P, CREVISE	H'000800
B	H'FFF380

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csc@renesas.com

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		Description	
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