ClockMatrix™

Mapping Clock Device Pins to Clock Numbers in the 8A34005

Abstract

This document explains the mapping between the device pins used for input clocks (CLK and GPIO) and the internal names (CLK) used by the firmware to configure these input clocks in the ClockMatrix 8A34005.

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Related Information

For more information, visit our website: ClockMatrix™ Timing Solutions

1. Pin Mapping to Clock Names

In addition to the CLK and nCLK pins on the 8A34005, the GPIO inputs on the device can also be used as frequency-only input clocks. Multiplexors in the device direct the clock signals from the clock and GPIO pins to different functional blocks in the 8A34005. The clock name corresponding to each clock or GPIO pin changes depending on the configuration. These names are used to determine the correct registers for input configuration.

For more information, see the *8A34005 Datasheet* and the *8A3xxxx Family Programming Guide v5.2.* In addition, the corresponding version of firmware can be downloaded from the 8A34005 product page.

Each pair of clock input pins can be used as a differential pair or two single-ended references. In addition, a GPIO can be used instead of the second single-ended reference clock. In the GUI, the clock is labeled with a differential, single-ended, or GPIO name, but all share common resources in the frequency input blocks. A GPIO alternate clock can be used with either a single-ended or differential clock on the CLK/nCLK pins. The clock names are listed in Table 1.

For example, when CLK1/nCLK1 is used as two single-ended clocks they will be configured as CLK1 and CLK9 (for the clock on pin nCLK1). For the 8A34005, the clock input numbers are not shared between CLK/nCLK and GPIO pins.

Table 1. Clock Naming on 8A34005

Pin Name, Differential Clock Number [m]	Primary Single-ended Clock Number [m]	Secondary Single-ended Clock Number [m+8]	GPIO Pin for Alternate Clock Input [j]
CLK0	CLK0		
nCLK0		CLK8	NA
CLK1	CLK1		
nCLK1		CLK9	NA
		CLK13	GPIO0
		CLK15	GPIO3

Note: This mapping is for the 8A34005. For the 8A34005, only two of the GPIO pins can act as references. Other ClockMatrix devices may have a slightly different mapping.

The clock routing within the 8A34005 is shown in Figure 1 for the CLK input pins, and Figure 2 for the GPIO pins. The internal structures in both figures are related and use some of the same registers for configuration. The details of the control of the multiplexors in the figure are shown in Table 2. Mux B must be set to match the available inputs in each figure (the multiplexor must use nCLK for clock inputs and GPIO for GPIO inputs).

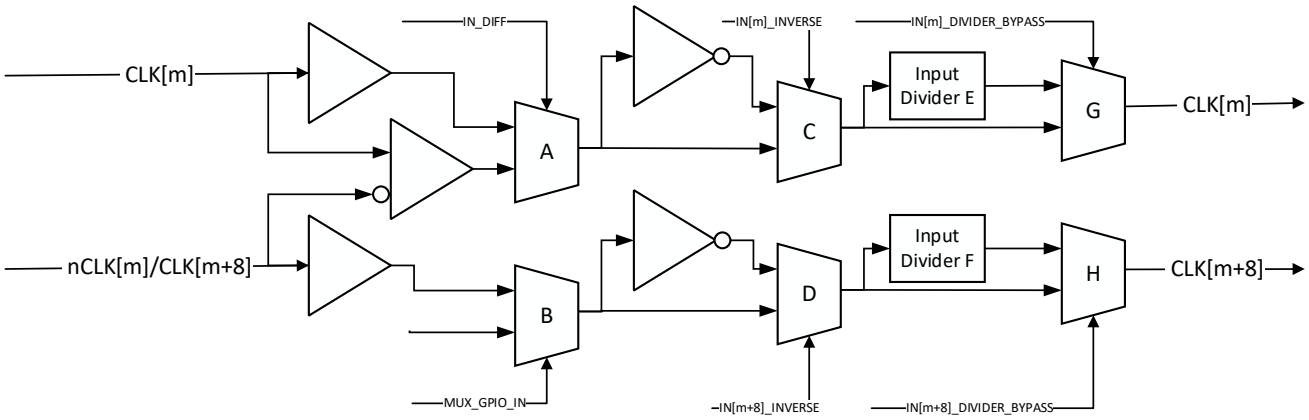

Figure 1. Input Signal Routing on ClockMatrix for Differential, Single-Ended via CLK[m] and nCLK[m]/CLK[m+8]

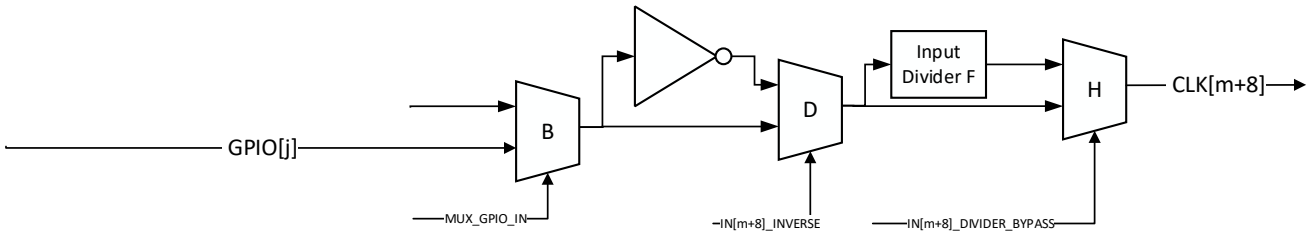

Figure 2. Input Signal Routing on ClockMatrix for Alternate Frequency Input via GPIO[j] Pin for CLK[m+8]

The multiplexors in the diagrams are explained in the following table using CLK0 and CLK8.

Table 2. Register Names for Input Clock Routing Control

Mux	Function	Register in Programmer's Guide	Register in GUI	Function when 0	Function when 1
A	Primary single-ended or differential	INPUT_0.IN_MODE. IN_DIFF[5]	IN0_DIFF (or set indirectly via "Input protocol")	Use CLK as first single-ended input	Use CLK/nCLK as first differential input
B	Secondary single-ended clock source (from nCLK or GPIO)	INPUT_0.IN_MODE. MUX_GPIO_IN[6]	IN0_MUX_GPIO_IN	Use nCLK as second single-ended input	Use GPIO as second single-ended input
C	Diff/primary single-ended invert	INPUT_0.IN_MODE. IN_INVERSE[3]	IN0_INVERSE	Use Primary single-ended or differential normally	Use Primary single-ended or differential inverted
D	Secondary clock invert	INPUT_8.IN_MODE. IN_INVERSE[3]	IN8_INVERSE	Use Secondary Single-ended or GPIO clock normally	Use Secondary Single-ended or GPIO clock inverted
G	Primary clock divider bypass	INPUT_0.IN_DIV	IN0_DIV	When Divider E is set to 0 or 1, bypass divider	
H	Secondary clock divider bypass	INPUT_8.IN_DIV	IN8_DIV	When Divider F is set to 0 or 1, bypass divider	

Note: E and F are dividers controlled in this example by Programmer's Guide registers INPUT_0.IN_DIV for multiplexor G and INPUT_8.IN_DIV for multiplexor H.

Note: An "[n]" in a register name refers to a bit within the register. For example, INPUT_0.IN_MODE.IN_DIFF[5] refers to module INPUT_0, register IN_MODE, bit 5.

2. Revision History

Revision	Date	Description
1.0	Feb.1.21	Initial release.

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