# ClockMatrix™

## Mapping Clock Device Pins to Clock Numbers in the 8A34001


### Abstract

This document explains the mapping between the device pins used for input clocks (CLK and GPIO) and the internal names (CLK) used by the firmware to configure these input clocks in the ClockMatrix 8A34001.


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## Related Documents

For more information, visit our website: ClockMatrix™ Timing Solutions

# 1. Pin Mapping to Clock Names

Besides the CLK and nCLK pins on the ClockMatrix 8A34001, the GPIO inputs on ClockMatrix can also be used as frequency-only input clocks. Multiplexors in the device direct the clock signals from the clock and GPIO pins to different functional blocks in the device. The clock name corresponding to each clock or GPIO pin change depending on the configuration. These names are used to determine the correct registers for input configuration.

Note: For more information, see the *8A34001 Datasheet* and the *8A3xxx Family Programming Guide* for the corresponding version of firmware that can be downloaded from ClockMatrix Timing Solutions.

Each pair of clock input pins can be used as a single differential pair or two single-ended references. In addition, a GPIO can be used instead of the second single-ended reference clock. In the GUI, the clock are labeled with differential, single-ended, or GPIO names, but all share common resources in the frequency input blocks. A GPIO alternate clock can be used with either a single-ended or differential clock on the CLK/nCLK pins. The clock names are listed in Table 1.

For example, when CLK1/nCLK1 is used as two single-ended clocks they will be configured as CLK1 and CLK9 (for the clock on pin nCLK1). If nCLK1 is not used as a single-ended clock, then GPIO15 can be configured as CLK9.

**Table 1. Clock Naming on 8A34001**

| Pin Name, Differential Clock Number [m] | Primary Single-ended Clock Number [m] | Secondary Single-ended Clock Number [m+8] | GPIO Pin for Alternate Clock Input [j] |
|---|---|---|---|
| CLK0 | CLK0 | | |
| nCLK0 | | CLK8 | GPIO0 |
| CLK1 | CLK1 | | |
| nCLK1 | | CLK9 | GPIO15 |
| CLK2 | CLK2 | | |
| nCLK2 | | CLK10 | GPIO14 |
| CLK3 | CLK3 | | |
| nCLK3 | | CLK11 | GPIO13 |
| CLK4 | CLK4 | | |
| nCLK4 | | CLK12 | GPIO12 |
| CLK5 | CLK5 | | |
| nCLK5 | | CLK13 | GPIO11 |
| CLK6 | CLK6 | | |
| nCLK6 | | CLK14 | GPIO10 |
| CLK7 | CLK7 | | |
| nCLK7 | | CLK15 | GPIO3 |

Note: This clock mapping is for the 8A34001. Other ClockMatrix devices may have a slightly different mapping.

The clock routing within the device is shown in Figure 1. The details of the control of the multiplexors in the figure are shown in Table 2.

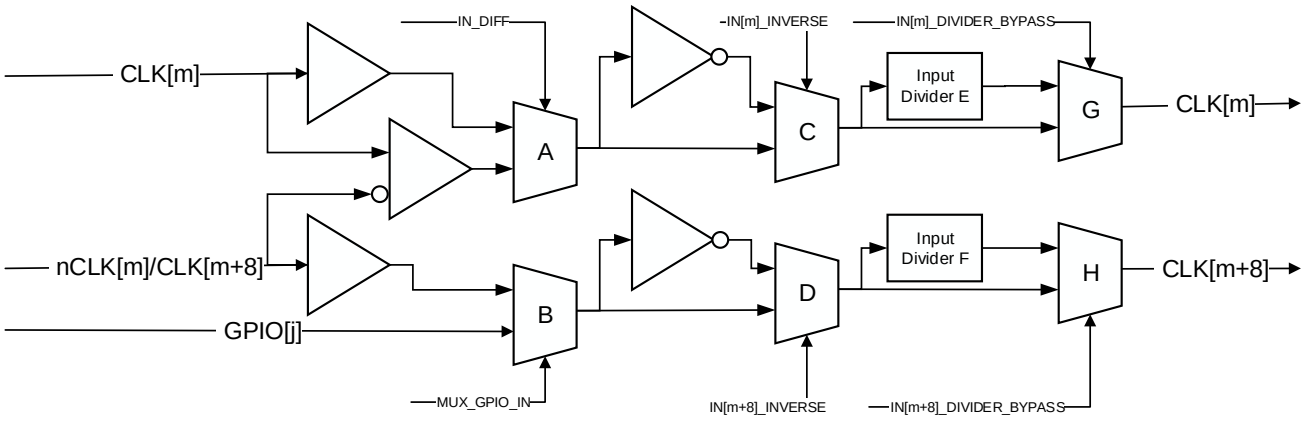


**Figure 1. Input Signal Routing on ClockMatrix**

Note: The figure shows differential, single-ended, and alternate frequency input via GPIO pin for CLK[m], nCLK[m]/CLK[m+8], and GPIO[j].

The multiplexors in the diagram are explained in the following table (using CLK0/CLK8/GPIO0 as an example).

**Table 2. Register Names for Input Clock Routing Control**

| Mux | Function | Register in Programmer's Guide | Register in GUI | Function when 0 | Function when 1 |
|---|---|---|---|---|---|
| A | Primary single-ended or differential | INPUT_0.IN_MODE. IN_DIFF[5] | IN0_DIFF (or set indirectly via "Input protocol") | Use CLK as first single-ended input | Use CLK/nCLK as first differential input |
| B | Secondary single-ended clock source (from nCLK or GPIO) | INPUT_0.IN_MODE. MUX_GPIO_IN[6] | IN0_MUX_GPIO_IN | Use nCLK as second single-ended input | Use GPIO as second single-ended input |
| C | Diff/primary single-ended invert | INPUT_0.IN_MODE. IN_INVERSE[3] | IN0_INVERSE | Use Primary single-ended or differential normally | Use Primary single-ended or differential inverted |
| D | Secondary clock invert | INPUT_8.IN_MODE. IN_INVERSE[3] | IN8_INVERSE | Use Secondary single---ended or GPIO clock normally | Use Secondary single-ended or GPIO clock inverted |
| G | Primary clock divider bypass | INPUT_0.IN_DIV | IN0_DIV | When Divider E is set to 0 or 1, bypass divider | |
| H | Secondary clock divider bypass | INPUT_8.IN_DIV | IN8_DIV | When Divider F is set to 0 or 1, bypass divider | |

Note: E and F are dividers controlled in this example by Programming Guide registers INPUT_0.IN_DIV for multiplexor G and INPUT_8.IN_DIV for multiplexor H.

Note: A "[n]" in a register name refers to a bit within the register. For example, INPUT_0.IN_MODE.IN_DIFF[5] refers to module INPUT_0, register IN_MODE, bit 5.

# 2. Revision History

| Revision | Date | Description |
|---|---|---|
| 1.0 | Jun.1.20 | Initial release. |

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