M16C/65C Group and RL78/G13, RL78/G14

Peripheral Function Comparison between M16C/65C Group and RL78/G13, RL78/G14

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Abstract

This document describes peripheral function comparison between the M16C/65C Group and RL78/G13, RL78/G14.

Products

M16C Family: M16C/65C Group (100-pin version)
RL78 Family: RL78/G13 (100-pin products) and RL78/G14 (100-pin products)

For more details and electrical characteristics, refer to the hardware user's manual and technical updates.

1. Peripheral Function Comparison

Table 1.1 to Table 1.9 list the peripheral function comparison between the M16C/65C Group (100-pin version) and RL78/G14, RL78/G13 (100-pin products).
In this application note, peripheral functions of the RL78/G14 and RL78/G13 are compared to the peripheral functions in the M16C/65 Group in order to show a guideline when the M16C Family is replaced with the RL78 Family. Tables comparing the peripheral functions show which peripheral functions of the RL78/G14 and RL78/G13 apply to the peripheral functions of the M16C/65C Group. A comparison of CPU cores is not included in the tables.
For more details on RL78/G14 and RL78/G13 peripheral functions, refer to the documents listed in 2.Reference Documents.

Table 1.1 Peripheral Function Comparison (1)

Item		M16C/65C Group (100-pin version)	RL78/G14 (100-pin products)	RL78/G13 (100-pin products)
Protection	Protect function for rewriting registers	Protect by protect register (protect rewriting registers associated with clocks, timer B2, serial interface (SI/O3, SI/O4), processor mode, port direction, and voltage detection, etc.)	Protect by invalid memory access detection control register (protect rewriting registers associated with part of RAM, ports, interrupts, clocks, and voltage detection, etc.)	
Resets		Hardware reset	External reset input via $\overline{\text{RESET}}$ pin	
		Power-on reset	Internal reset by comparison of supply voltage and detection voltage of power-on-reset (POR) circuit	
		• Voltage monitor 0 reset • Voltage monitor 1 reset • Voltage monitor 2 reset	Internal reset by comparison of supply voltage of the voltage detector (LVD) and detection voltage	
		Oscillator stop detect reset	—	
		Watchdog timer reset	Internal reset by watchdog timer program loop detection	
		Software reset	—	
Voltage Detectors	Voltage monitor 0	Voltage monitor 0 reset	• Function of voltage detector (LVD) (reset mode) • Function of voltage detector (LVD) (interrupt and reset mode)	
	Voltage monitor 1	• Voltage monitor 1 reset • Voltage monitor 1 interrupt	• Function of voltage detector (LVD) (reset mode) • Function of voltage detector (LVD) (interrupt mode)	
	Voltage monitor 2	• Voltage monitor 2 reset • Voltage monitor 2 interrupt	• Function of voltage detector (LVD) (reset mode) • Function of voltage detector (LVD) (interrupt mode)	
Clocks	External oscillator	XIN clock generator (2 to 20 MHz)	X1 oscillator (1 to 20 MHz)	
	External sub oscillator	XCIN clock generator (32.768 to 50 kHz)	XT1 oscillator (32.768 kHz)	
	Internal oscillator (high-speed)	40 MHz on-chip oscillator (CPU clock: Divide ratio selectable from 2, 4, 8, and 16 of fOCO-F) * fOCO-F = 40 MHz on-chip oscillator/2	Internal high-speed oscillator (Selectable from 64 MHz, 48 MHz, 32 MHz, 24 MHz, 16 MHz, 12 MHz, 8 MHz, or 1 MHz)	Internal high-speed oscillator (Selectable from 32 MHz, 24 MHz, 16 MHz, 12 MHz, 8 MHz, or 1 MHz)
	Internal oscillator (low-speed)	125 kHz on-chip oscillator	Internal low-speed oscillator (15 kHz)	
	PLL frequency synthesizer	PLL frequency synthesizer (10 to 32 MHz)	—	
	Power control	Wait mode	HALT mode	
		Stop mode	STOP mode	
		—	SNOOZE mode	
	Enable/disable peripheral clock provision	• Timer A • Timer B	• Timer array unit • Timer RJ • Timer RD • Timer RG • Real-time clock • Interval timer • A/D converter • D/A converter • Comparator • Serial array unit • Serial interface IICA • DTC	• Timer array unit • Real-time clock • Interval timer • A/D converter • Serial array unit • Serial interface IICA

Table 1.2 Peripheral Function Comparison (2)

Item		M16C/65C Group (100-pin version)	RL78/G14 (100-pin products)	RL78/G13 (100-pin products)
Bus	External bus	• Separate bus • Multiplexed bus	—	
Memories	Memory space expansion function	1-MB mode	—	
		4-MB mode	—	
Ports	I/O port control	Port Pi direction register (i = 0 to 10)	Port mode register (i = 0 to 8, 10 to 12, 14, or 15)	
	Input port	Pull-up control	Pull-up resistor option	
	Output port	—	N-ch open-drain can be selected by the port output mode registers	
Interrupts	Non-maskable interrupts	Undefined instruction interrupt	Internal reset by execution of illegal instruction	
		Overflow interrupt	—	
		BRK interrupt	Execution interrupt of BRK instruction	
		INT instruction interrupt	—	
		Watchdog timer interrupt	Internal reset by overflow of watchdog timer	
		$\overline{NMI}$ interrupt	—	
		Oscillation stop/restart detect interrupt	—	
		Voltage monitor 1 interrupt	—	
		Voltage monitor 2 interrupt	—	
		Address match interrupt	—	
	Maskable interrupts	Peripheral function interrupts	Internal interrupt	
	$\overline{INT}$ interrupt	$\overline{INT}$ interrupt input ($\overline{INT0}$ to $\overline{INT7}$) ($\overline{INT4}$ and $\overline{INT5}$ each share an interrupt vector and interrupt control register with SI/O3 and SI/O4, respectively.	External interrupt input (INTP0 to INTP11)	
	Key input interrupt	Key input interrupt (KI0 to KI3)	Key interrupt input (KRM0 to KRM7)	

Table 1.3 Peripheral Function Comparison (3)

Item		M16C/65C Group (100-pin version)	RL78/G14 (100-pin products)	RL78/G13 (100-pin products)
Option Function Select Areas		• Select watchdog timer start after reset • Select count source protection mode after reset • Select voltage detector 0 start • Select Vdet0 • Select ROM code protect function	• Select watchdog timer operation • Select watchdog timer operation in HALT/STOP mode • Set watchdog timer overflow time • Set window open period of watchdog timer • Select watchdog timer interval interrupt • Set LVD operation mode • Set LVD detection level (V_{LVIH}) • Set minimum operation voltage (V_{LVIL}) • Set frequency of the internal high-speed oscillator • Set flash operation mode • Handling of data of flash memory in case of failure in on-chip debug security ID authentication • Select control of on-chip debug operation	
Watchdog Timer		Count source protection mode can be selected: • Disabled: The count source for the watchdog timer is the CPU clock • Enabled: The count source for the watchdog timer is fOCO-S (125 kHz on-chip oscillator clock)	Always protect count source • The count source is the internal low-speed oscillation clock	
		Watchdog timer interrupt • Underflow	Interval interrupt when 75% of the overflow time is reached	
		Watchdog timer reset • Underflow	Internal reset by watchdog timer program loop detection • Overflow • Write during a window close period • Use a 1-bit manipulation instruction on the WDTE register • Write data other than "ACH" to the WDTE register	
Data Transfer Functions	Direct memory access controller (DMAC)	DMAC (single transfer, repeat transfer)	DTC (normal mode, repeat mode, and chain transfers)	DMA (single transfer)

Table 1.4 Peripheral Function Comparison (4)

Item		M16C/65C Group (100-pin version)	RL78/G14 (100-pin products)	RL78/G13 (100-pin products)
Timers	Timer A (16-bit timer)	Timer A (timer mode) • Gate function not available	• Timer RJ (timer mode) • Timer RD (timer mode) • Timer RG (timer mode) • TAU interval timer • Interval timer	• TAU interval timer • Interval timer
		Timer A (timer mode) • Gate function available	• Timer RJ (pulse width measurement mode)	—
		Timer A (timer mode) • Pulse output function	• Timer RJ (pulse output mode) • Timer RD (timer mode (output compare function)) • Timer RG (timer mode (output compare function)) • TAU square wave output • TAU divider function (channel 0 (unit 0 only))	• TAU square wave output • TAU divider function (channel 0 (unit 0 only))
		Timer A (event counter mode) • Two-phase pulse signal processing not included	• Timer RJ (event counter mode) • Timer RD (timer mode) • Timer RG (timer mode) • TAU external event counter	TAU external event counter
		Timer A (event counter mode) • Two-phase pulse signal processing included	• Timer RG (phase counting mode)	—
		Timer A (one-shot timer mode)	TAU delay counter	TAU delay counter
		Timer A (pulse width modulation mode)	• Timer RD (PWM function) • Timer RG (PWM mode) • TAU PWM output (channels 0-1 to 3, 2-3)	TAU PWM output (channels 0-1 to 7, 2-3 to 7, 4-5 to 7, 6-7)
		Timer A (programmable output mode)	—	

Table 1.5 Peripheral Function Comparison (5)

Item		M16C/65C Group (100-pin version)	RL78/G14 (100-pin products)	RL78/G13 (100-pin products)
Timers	Timer B (16-bit timer)	Timer B (timer mode)	• Timer RJ (timer mode) • Timer RD (timer mode) • Timer RG (timer mode) • TAU interval timer • Interval timer	• TAU interval timer • Interval timer
		Timer B (event counter mode)	• Timer RJ (event counter mode) • Timer RD (timer mode) • Timer RG (timer mode) • TAU external event counter	TAU external event counter
		Timer B (pulse width measurement mode)	• Timer RJ (pulse width measurement mode) • Timer RD (timer mode (input capture function)) • Timer RG (timer mode (input capture function)) • Measurement of high-/low-level width of TAU input signal	Measurement of high-/low-level width of TAU input signal
		Timer B (pulse period measurement mode)	• Timer RJ (pulse period measurement mode) • Timer RD (timer mode (input capture function)) • Timer RG (timer mode (input capture function)) • Measurement of TAU input pulse interval	Measurement of TAU input pulse interval

Table 1.6 Peripheral Function Comparison (6)

Item		M16C/65C Group (100-pin version)	RL78/G14 (100-pin products)	RL78/G13 (100-pin products)
Timers	Three-phase motor control timer function	Triangular wave modulation three-phase mode 0	Timer RD (complementary PWM mode)	—
		Triangular wave modulation three-phase mode 1		—
		Sawtooth wave modulation mode	Timer RD (PWM3 mode)	—
	Real-time clock	Compare mode 1 (seconds, minutes, hours, a.m./p.m., a day, and a week can be counted)	Real-time clock (seconds, minutes, hours, a.m./p.m., a day, a week, month, and year can be counted)	
		Compare mode 2 (seconds, minutes, hours, a.m./p.m., a day, and a week can be counted)		
		Compare mode 3 (seconds, minutes, hours, a.m./p.m., a day, and a week can be counted)		
	PWM function	PWM function	• Timer RJ (pulse output mode) • Timer RD (timer mode (output compare function) and PWM function) • Timer RG (timer mode (output compare function) and PWM function) • TAU square wave output • TAU divider function (channel 0 (unit 0 only)) • TAU PWM output (channels 0-1 to 3, 2-3)	• TAU square wave output • TAU divider function (channel 0 (unit 0 only)) • TAU PWM output (channels 0-1 to 7, 2-3 to 7, 4-5, to 7, 6-7)
	Remote Control Signal Receiver	Pattern match mode	—	
		Input capture mode • Pulse period measurement • Pulse width measurement	Pulse period measurement: • Timer RJ (pulse period measurement mode) • Timer RD (timer mode (input capture function)) • Timer RG (timer mode (input capture function)) • Measurement of TAU input pulse interval Pulse width measurement: • Timer RJ (pulse width measurement mode) • Timer RD (timer mode (input capture function)) • Timer RG (timer mode (input capture function)) • Measurement of high-/low-level width of TAU input signal	Pulse period measurement: • Measurement of TAU input pulse interval Pulse width measurement: • Measurement of high-/low-level width of TAU input signal

Table 1.7 Peripheral Function Comparison (7)

Item		M16C/65C Group (100-pin version)	RL78/G14 (100-pin products)	RL78/G13 (100-pin products)
Communications	Serial interface UART0, 1, 5, 6, and 7	Clock synchronous serial I/O mode	Serial array unit: 3-wire serial I/O CSI00 (unit 0 channel 0) CSI01 (unit 0 channel 1) CSI10 (unit 0 channel 2) CSI11 (unit 0 channel 3) CSI20 (unit 1 channel 0) CSI21 (unit 1 channel 1) CSI30 (unit 1 channel 2) CSI31 (unit 1 channel 3)	
		Clock asynchronous serial I/O (UART) mode	Serial array unit UART UART0 [CSI00 (unit 0 channel 0) and CSI01 (unit 0 channel 1)] UART1 [CSI10 (unit 0 channel 2) and CSI11 (unit 0 channel 3)] UART2 [CSI20 (unit 1 channel 0) and CSI21 (unit 1 channel 1)] UART3 [CSI30 (unit 1 channel 2) and CSI31 (unit 1 channel 3)]	
		Special mode 1 (I^2C mode) (master/slave function in single-master system)	Serial array unit : Simplified I^2C Communication (only master function in single master system) IIC00 (unit 0 channel 0) IIC01 (unit 0 channel 1) IIC10 (unit 0 channel 2) IIC11 (unit 0 channel 3) IIC20 (unit 1 channel 0) IIC21 (unit 1 channel 1) IIC30 (unit 1 channel 2) IIC31 (unit 1 channel 3)	
		Special mode 2	Serial array unit : SPI function communication CSI00 (unit 0 channel 0) (Arbitration not checked and chip select controlled by ports)	—
		Special mode 3 (IE mode)	—	

Table 1.8 Peripheral Function Comparison (8)

Item		M16C/65C Group (100-pin version)	RL78/G14 (100-pin products)	RL78/G13 (100-pin products)
Communications	Serial interface UART2	Clock synchronous serial I/O mode	Serial array unit 3-wire serial I/O CSI00 (unit 0 channel 0) CSI01 (unit 0 channel 1) CSI10 (unit 0 channel 2) CSI11 (unit 0 channel 3) CSI20 (unit 1 channel 0) CSI21 (unit 1 channel 1) CSI30 (unit 1 channel 2) CSI31 (unit 1 channel 3)	
		Clock Asynchronous Serial I/O Mode (UART mode)	Serial array unit UART UART0 [CSI00 (unit 0 channel 0) and CSI01 (unit 0 channel 1)] UART1 [CSI10 (unit 0 channel 2) and CSI11 (unit 0 channel 3)] UART2 [CSI20 (unit 1 channel 0) and CSI21 (unit 1 channel 1)] UART3 [CSI30 (unit 1 channel 2) and CSI31 (unit 1 channel 3)]	
		Special mode 1 (I^2C mode) (Master/slave function in single-master system)	Serial array unit : Simplified I^2C communication (only master function in single master system) IIC00 (unit 0 channel 0) IIC01 (unit 0 channel 1) IIC10 (unit 0 channel 2) IIC11 (unit 0 channel 3) IIC20 (unit 1 channel 0) IIC21 (unit 1 channel 1) IIC30 (unit 1 channel 2) IIC31 (unit 1 channel 3)	
		Special mode 2	Serial array unit : SPI function communication CSI00 (unit 0 channel 0) (Arbitration not checked and chip select controlled by ports)	—
		Special mode 3 (IE mode)	—	
		Special mode 4 (SIM mode)	—	

Table 1.9 Peripheral Function Comparison (9)

Item		M16C/65C Group (100-pin version)	RL78/G14 (100-pin products)	RL78/G13 (100-pin products)
Communications	Serial interface I/O	Serial interface SI/O3 and SI/O4	Serial array unit 3-wire serial I/O CSI00 (unit 0 channel 0) CSI01 (unit 0 channel 1) CSI10 (unit 0 channel 2) CSI11 (unit 0 channel 3) CSI20 (unit 1 channel 0) CSI21 (unit 1 channel 1) CSI30 (unit 1 channel 2) CSI31 (unit 1 channel 3)	
	I^2C-bus interface	Mult-master I^2C-bus interface	Serial interface IICA	
	CEC function	CEC function	—	
Analog Conversion Function	A/D converter	One-shot mode	Select mode, one-shot conversion mode	
		Repeat mode	Select mode, sequential conversion mode	
		Single sweep mode	Scan mode, One-shot conversion mode	
		Repeat sweep mode 0	Scan mode, Sequential conversion mode	
		Repeat sweep mode 1	—	
	D/A converter	D/A converter	D/A converter	—
Flash Memories	UART programming	Standard serial I/O mode 1	Flash memory programming mode single-line UART	
		Standard serial I/O mode 2	Flash memory programming mode UART0	
	Parallel I/F programming	Parallel I/O mode	—	
	Software programming	CPU rewrite mode	Flash memory programming by self-programming	
	Boot mode	User boot mode	—	
		Standard serial I/O mode	—	
	Security function	• ID code check function (standard serial I/O mode) • Forced erase function (standard serial I/O mode) • Standard serial I/O mode disable function (standard serial I/O mode) • ROM code protect function (parallel I/O mode) • Data protect function (CPU rewrite mode)	• Disabling block erase • Disabling write • Disabling rewriting boot cluster 0 • Flash shield window function (self-programming only) • On-chip debug security ID	
CRC	CRC calculation	CRC calculator	Flash memory CRC operation function	

2. Reference Documents

User's Manual: Hardware

M16C/65C Group User's Manual: Hardware Rev. 1.00
RL78/G13 User's Manual: Hardware Rev. 1.00
RL78/G14 User's Manual: Hardware: Rev. 0.02
The latest versions can be downloaded from the Renesas Electronics website.

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General Precautions in the Handling of MPU/MCU Products

The following usage notes are applicable to all MPU/MCU products from Renesas. For detailed usage notes on the products covered by this manual, refer to the relevant sections of the manual. If the descriptions under General Precautions in the Handling of MPU/MCU Products and in the body of the manual differ from each other, the description in the body of the manual takes precedence.

1. Handling of Unused Pins
   Handle unused pins in accord with the directions given under Handling of Unused Pins in the manual.
   — The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible. Unused pins should be handled as described under Handling of Unused Pins in the manual.
2. Processing at Power-on
   The state of the product is undefined at the moment when power is supplied.
   — The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the moment when power is supplied.
   In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the moment when power is supplied until the reset process is completed.
   In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the moment when power is supplied until the power reaches the level at which resetting has been specified.
3. Prohibition of Access to Reserved Addresses
   Access to reserved addresses is prohibited.
   — The reserved addresses are provided for the possible future expansion of functions. Do not access these addresses; the correct operation of LSI is not guaranteed if they are accessed.
4. Clock Signals
   After applying a reset, only release the reset line after the operating clock signal has become stable. When switching the clock signal during program execution, wait until the target clock signal has stabilized.
   — When the clock signal is generated with an external resonator (or from an external oscillator) during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Moreover, when switching to a clock signal produced with an external resonator (or by an external oscillator) while program execution is in progress, wait until the target clock signal is stable.
5. Differences between Products
   Before changing from one product to another, i.e. to one with a different type number, confirm that the change will not lead to problems.
   — The characteristics of MPU/MCU in the same group but having different type numbers may differ because of the differences in internal memory capacity and layout pattern. When changing to products of different type numbers, implement a system-evaluation test for each of the products.

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