

Industrial Ethernet PHY

Programming Guide

Ethernet PHY ASSP

uPD60610,
uPD60611,
uPD60620,
uPD60620A,
uPD60621A,

All information contained in these materials, including products and product specifications, represents information on the product at the time of publication and is subject to change by Renesas Electronics Corp. without notice. Please review the latest information published by Renesas Electronics Corp. through various means, including the Renesas Technology Corp. website (<http://www.renesas.com>).

(1) List of Abbreviations and Acronyms

Abbreviation	Full Form
AN	Application Note
ASSP	Application Specific Standard Product
Autoneg	Auto-Negotiation
BER	Bit Error
DSP	Digital Signaling Processor
FEQ	Forward Equalizer
FLP	Fast Link Pulses
GPIO	General Programmable Input - Output
LED-MUX	LED Multiplexing
MII	Media Independent Interface
NLP	Normal Link Pulses
PD	Partner Device
PTP	Precision Time Protocol
RMII	Reduced Media Independent Interface
TDR	Time Domain Reflectometer
UM	User's Manual

Table of Contents

Chapter 1	General Information	4
Chapter 2	GPIOs	5
2.1	GPIO overview	5
2.2	LED multiplexing (Single-channel ASSP).....	7
Chapter 3	Interrupts	8
Chapter 4	Bit Error Counter	10
Chapter 5	FEQ Monitor.....	12
Chapter 6	Time Domain Reflectometer	15
Chapter 7	Quick Auto-Negotiation.....	18

Chapter 1 General Information

The Renesas Ethernet PHY ASSPs uPD60610/11 and uPD60620/20A/21A are Ethernet physical layer devices for 10Base-T, 100Base-TX and 100Base-FX operation. In addition to the specified Ethernet PHY functions these PHY ASSPs support various special functions which are explained in this application note.

This document does not contain descriptions of PTP 1588 and its related functionalities such as Input Capture and Pulse Generator.

This application note is complementary material to the following documents. Please read these documents for further information.

- Single PHY ASSP User Manual
R19UH0082EDxxxx
- Dual PHY ASSP User Manual
R19UH0083EDxxxx
- Single PHY ASSP Application Note - Layout recommendations and design rules
R19AN0014EDxxxx
- Dual PHY ASSP Application Note - Layout recommendations and design rules
R19AN0015EDxxxx

Note:

xxxx – version number

Chapter 2 GPIOs

2.1 GPIO overview

The Renesas Ethernet PHY ASSPs offer various options for configuring GPIO pins to achieve application-specific signalling in a system. The number of accessible GPIO ports depends on the MII mode. In RMII mode many more GPIOs are available due to the unused ports compared to MII mode.

To give an optimized overview of all GPIOs the tables 2-1, 2-2, 2-3 and 2-4 show the GPIO options depending on the PHY device and the used MII mode.

Detailed descriptions of the related functionalities are given in the UMs. Some functions of the GPIO configurations are only available in PTP devices (marked blue in the tables).

The GPIO programming registers are shown in table 2-5.

Table 2-1 ASSP1 GPIO configurations in MII mode

GPIO	Pin Name	GPIO configurations															
		1111	1110	1101	1100	1011	1010	1001	1000	0111	0110	0101	0100	0011	0010	0001	0000
		15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	POLINKLED	Input	chip_sync	INT	SOF_RX0	SOF_TX0	LED3	LED2	LED1	LED0	P0PackRX	Pulse0	Pulse2	Pulse1	0	PPS	No change
4	INT	Input	chip_sync	INT	SOF_RX0	SOF_TX0	LED3	LED2	LED1	LED0	P0PackRX	Pulse0	Pulse2	Pulse1	0	PPS	No change
6	P0CRS	Input	chip_sync	INT	SOF_RX0	SOF_TX0	reserved	reserved	CLK_1us	CLK_1ms	P0CRS	Pulse0	Pulse2	Pulse1	0	PPS	No change
9	P0TXERR	Input	chip_sync	INT	SOF_RX0	SOF_TX0	LED3	LED2	LED1	LED0	P0TXERR	Pulse0	Pulse2	Pulse1	0	PPS	No change
14	GPIO14	Input	chip_sync	INT	SOF_RX0	SOF_TX0	LED3	LED2	LED1	LED0	PLLReady	Pulse0	Pulse2	Pulse1	0	PPS	No change
19	P0COLSD*	Input	chip_sync	INT	SOF_RX0	SOF_TX0	LED3	LED2	LED1	LED0	P0COL	Pulse0	Pulse2	Pulse1	0	PPS	No change

default output pin
 default MII pin

RESET VALUE
 related function available
 for μPD60611 only

LED signals are configurable

*P0COLSD is used as SD in FX-Mode

Table 2-2 ASSP1 GPIO configurations in RMII mode

GPIO	Pin Name	GPIO configuration															
		1111	1110	1101	1100	1011	1010	1001	1000	0111	0110	0101	0100	0011	0010	0001	0000
		15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	POLINKLED	Input	chip_sync	INT	SOF_RX0	SOF_TX0	LED3	LED2	LED1	LED0	P0PackRX	Pulse0	Pulse2	Pulse1	0	PPS	No change
3	P0RXCLK	Input	chip_sync	INT	SOF_RX0	SOF_TX0	RXCLK	0	CLK_1us	CLK_1ms	P0PackRX	Pulse0	Pulse2	Pulse1	0	PPS	No change
4	INT	Input	chip_sync	INT	SOF_RX0	SOF_TX0	LED3	LED2	LED1	LED0	P0PackRX	Pulse0	Pulse2	Pulse1	0	PPS	No change
5	P0TXCLK	Input	chip_sync	INT	SOF_RX0	SOF_TX0	TXCLK	0	CLK_1us	CLK_1ms	P0PackRX	Pulse0	Pulse2	Pulse1	0	PPS	No change
6	P0CRS	Input	chip_sync	INT	SOF_RX0	SOF_TX0	reserved	reserved	CLK_1us	CLK_1ms	PLLReady	Pulse0	Pulse2	Pulse1	0	PPS	No change
7	P0RXD3	Input	chip_sync	INT	SOF_RX0	SOF_TX0	reserved	reserved	1	0	P0PackRX	Pulse0	Pulse2	Pulse1	0	PPS	No change
8	P0RXD2	Input	chip_sync	INT	SOF_RX0	SOF_TX0	reserved	reserved	1	0	P0PackRX	Pulse0	Pulse2	Pulse1	0	PPS	No change
9	P0TXERR	Input	chip_sync	INT	SOF_RX0	SOF_TX0	LED3	LED2	LED1	LED0	LED1	Pulse0	Pulse2	Pulse1	0	PPS	No change
10	P0TXD3	Input	chip_sync	INT	SOF_RX0	SOF_TX0	LED3	LED2	LED1	LED0	P0PackRX	Pulse0	Pulse2	Pulse1	0	PPS	No change
11	P0TXD2	Input	chip_sync	INT	SOF_RX0	SOF_TX0	LED3	LED2	LED1	LED0	P0PackRX	Pulse0	Pulse2	Pulse1	0	PPS	No change
14	GPIO14	Input	chip_sync	INT	SOF_RX0	SOF_TX0	LED3	LED2	LED1	LED0	PLLReady	Pulse0	Pulse2	Pulse1	0	PPS	No change
19	P0COLSD*	Input	chip_sync	INT	SOF_RX0	SOF_TX0	LED3	LED2	LED1	LED0	Input	Pulse0	Pulse2	Pulse1	0	PPS	No change

default output pin
 default MII pin

RESET VALUE
 related function available
 for μPD60611 only

LED signals are configurable

*P0COLSD is used as SD in FX-Mode

Table 2-3 ASSP2 GPIO configurations in MII mode

GPIO	Pin Name	GPIO configurations															
		1111 15	1110 14	1101 13	1100 12	1011 11	1010 10	1001 9	1000 8	0111 7	0110 6	0101 5	0100 4	0011 3	0010 2	0001 1	0000 0
0	P0LNKLED	Input	chip_sync	INT	LED6	LED5	LED4	LED3	LED2	LED1	P0PackRX	P0PackTX	Pulse2	Pulse1	Pulse0	PPS	No change
1	P0ACTLED	Input	chip_sync	INT	LED6	LED5	LED4	LED3	LED2	LED1	P0PackRX	P0PackTX	Pulse2	Pulse1	Pulse0	PPS	No change
2	P1LNKLED	Input	chip_sync	INT	LED6	LED5	LED4	LED3	LED2	LED1	P1PackRX	P1PackTX	Pulse2	Pulse1	Pulse0	PPS	No change
3	P1ACTLED	Input	chip_sync	INT	LED6	LED5	LED4	LED3	LED2	LED1	P1PackRX	P1PackTX	Pulse2	Pulse1	Pulse0	PPS	No change
4	P0100BT	Input	P0COL	INT	LED6	LED5	LED4	LED3	LED2	LED1	P0PackRX	P0PackTX	Pulse2	Pulse1	Pulse0	PPS	No change
5	P1100BT	Input	P1COL	INT	LED6	LED5	LED4	LED3	LED2	LED1	P0PackRX	P0PackTX	Pulse2	Pulse1	Pulse0	PPS	No change
6	P0CRS	Input	P0CRS	INT	LED6	LED5	LED4	LED3	LED2	LED1	P0PackRX	P0PackTX	Pulse2	Pulse1	Pulse0	PPS	No change
9	P0TXERR	Input	chip_sync	INT	LED6	LED5	LED4	LED3	LED2	LED1	P0PackRX	P0TXERR	Pulse2	Pulse1	Pulse0	PPS	No change
12	P1CRS	Input	P1CRS	INT	LED6	LED5	LED4	LED3	LED2	LED1	P1PackRX	P1PackTX	Pulse2	Pulse1	Pulse0	PPS	No change
15	P1TXERR	Input	Chip_sync	INT	LED6	LED5	LED4	LED3	LED2	LED1	P0PackRX	P1TXERR	Pulse2	Pulse1	Pulse0	PPS	No change
18	PECL_SD0/P1COL*	Input	P1COL	INT	LED6	LED5	LED4	LED3	LED2	LED1	P0PackRX	P0PackTX	Pulse2	Pulse1	Pulse0	PPS	No change
19	PECL_SD0/P0COL*	Input	P0COL	INT	LED6	LED5	LED4	LED3	LED2	LED1	P0PackRX	P0PackTX	Pulse2	Pulse1	Pulse0	PPS	No change

default LED pin

default MII pin

RESET VALUE

related function available
for μ PD60621 only

*PxCOLSD is used as SD in FX-Mode

LEDs: LED1: Link PHY 0
 LED2: Link PHY 1
 LED3: 100 MBit PHY0
 LED4: 100 MBit PHY1
 LED5: Activity P0
 LED6: Activity P1

Table 2-4 ASSP2 GPIO configurations in RMII mode

GPIO	Pin Name	GPIO configurations															
		1111 15	1110 14	1101 13	1100 12	1011 11	1010 10	1001 9	1000 8	0111 7	0110 6	0101 5	0100 4	0011 3	0010 2	0001 1	0000 0
0	P0LNKLED	Input	chip_sync	INT	LED6	LED5	LED4	LED3	LED2	LED1	P0PackRX	P0PackTX	Pulse2	Pulse1	Pulse0	PPS	No change
1	P0ACTLED	Input	chip_sync	INT	LED6	LED5	LED4	LED3	LED2	LED1	P0PackRX	P0PackTX	Pulse2	Pulse1	Pulse0	PPS	No change
2	P1LNKLED	Input	chip_sync	INT	LED6	LED5	LED4	LED3	LED2	LED1	P1PackRX	P1PackTX	Pulse2	Pulse1	Pulse0	PPS	No change
3	P1ACTLED	Input	chip_sync	INT	LED6	LED5	LED4	LED3	LED2	LED1	P1PackRX	P1PackTX	Pulse2	Pulse1	Pulse0	PPS	No change
4	P0100BT	Input	P0COL	INT	LED6	LED5	LED4	LED3	LED2	LED1	P0PackRX	P0PackTX	Pulse2	Pulse1	Pulse0	PPS	No change
5	P1100BT	Input	P1COL	INT	LED6	LED5	LED4	LED3	LED2	LED1	P0PackRX	P0PackTX	Pulse2	Pulse1	Pulse0	PPS	No change
6	P0CRS	Input	P0CRS	INT	LED6	LED5	LED4	LED3	LED2	LED1	P0PackRX	P0PackTX	Pulse2	Pulse1	Pulse0	PPS	No change
7	P0RXD3	Input	Chip_sync	INT	LED6	LED5	LED4	LED3	LED2	LED1	P0PackRX	P0PackTX	Pulse2	Pulse1	Pulse0	PPS	No change
8	P0RXD2	Input	SOF_RX0	INT	LED6	LED5	LED4	LED3	LED2	LED1	P0PackRX	P0PackTX	Pulse2	Pulse1	Pulse0	PPS	No change
9	P0TXERR	Input	chip_sync	INT	LED6	LED5	LED4	LED3	LED2	LED1	P0PackRX	Input	Pulse2	Pulse1	Pulse0	PPS	No change
10	P0TXD3	Input	SOF_TX0	INT	LED6	LED5	LED4	LED3	LED2	LED1	P0PackRX	P0PackTX	Pulse2	Pulse1	Pulse0	PPS	No change
11	P0TXD2	Input	SOF_TX0	INT	LED6	LED5	LED4	LED3	LED2	LED1	P0PackRX	P0PackTX	Pulse2	Pulse1	Pulse0	PPS	No change
12	P1CRS	Input	P1CRS	INT	LED6	LED5	LED4	LED3	LED2	LED1	P1PackRX	P1PackTX	Pulse2	Pulse1	Pulse0	PPS	No change
13	P1RXD3	Input	SOF_RX1	INT	LED6	LED5	LED4	LED3	LED2	LED1	P0PackRX	P0PackTX	Pulse2	Pulse1	Pulse0	PPS	No change
14	P1RXD2	Input	SOF_RX1	INT	LED6	LED5	LED4	LED3	LED2	LED1	P0PackRX	P0PackTX	Pulse2	Pulse1	Pulse0	PPS	No change
15	P1TXERR	Input	Chip_sync	INT	LED6	LED5	LED4	LED3	LED2	LED1	P0PackRX	Input	Pulse2	Pulse1	Pulse0	PPS	No change
16	P1TXD3	Input	SOF_TX1	INT	LED6	LED5	LED4	LED3	LED2	LED1	P0PackRX	P0PackTX	Pulse2	Pulse1	Pulse0	PPS	No change
17	P1TXD2	Input	SOF_TX1	INT	LED6	LED5	LED4	LED3	LED2	LED1	P1PackRX	P1PackTX	Pulse2	Pulse1	Pulse0	PPS	No change
18	PECL_SD1/P1COL*	Input	P1COL	INT	LED6	LED5	LED4	LED3	LED2	LED1	P0PackRX	P0PackTX	Pulse2	Pulse1	Pulse0	PPS	No change
19	PECL_SD0/P0COL*	Input	P0COL	INT	LED6	LED5	LED4	LED3	LED2	LED1	P0PackRX	P0PackTX	Pulse2	Pulse1	Pulse0	PPS	No change

default LED pin

default MII pin

RESET VALUE

related function available
for μ PD60621 only

*PxCOLSD is used as SD in FX-Mode

LEDs: LED1: Link PHY 0
 LED2: Link PHY 1
 LED3: 100 MBit PHY0
 LED4: 100 MBit PHY1
 LED5: Activity P0
 LED6: Activity P1

Table 2-5 GPIO registers

<i>PHY address 7</i>	Bits			
Register	15 - 12	11 - 8	7 - 4	3 - 0
0	GPIO 3	GPIO 2	GPIO 1	GPIO 0
1	GPIO 7	GPIO 6	GPIO 5	GPIO 4
2	GPIO 11	GPIO 10	GPIO 9	GPIO 8
3	GPIO 15	GPIO 14	GPIO 13	GPIO 12
4	GPIO 19	GPIO 18	GPIO 17	GPIO 16

2.2 LED multiplexing (Single-channel ASSP)

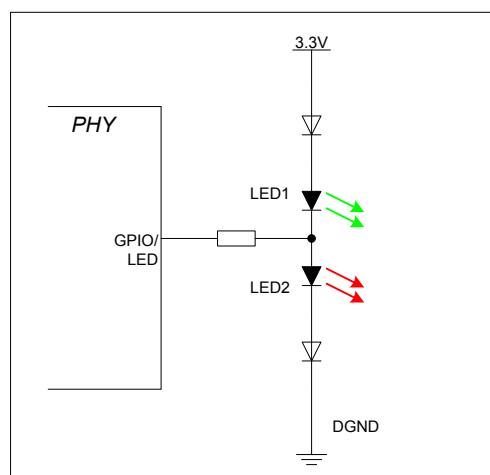
Note:

- This feature is available in single channel PHYs only.

As the single channel PHY has few GPIOs (especially in MII mode) it supports an option for LED multiplexing (abbr.: LED-MUX). This allows the device to drive two LEDs via one GPIO port.

All programmable LED configurations are listed in the UM. A LED-MUX signal is described with MUX "*data1/data2*". Referring to figure 2-1 (schematic of layout AN) *data1* is displayed in LED1 and *data2* is displayed in LED2.

Figure 2-1 Schematic for LED multiplexing



Chapter 3 Interrupts

The PHY ASSP devices have different interrupts that can be read from the interrupt registers and that can also be output via an interrupt pin.

The interrupt function can be selected for each GPIO pin. An interrupt output signal is active high.

The interrupt-related registers are:

- PHY0 interrupt register (0.29)
- PHY0 interrupt enable register (0.30)
- PHY1 interrupt register (1.29) *Dual Channel PHY only*
- PHY1 interrupt enable register (1.30) *Dual Channel PHY only*
- Top Level interrupt register (7.20)
- Top Level interrupt mask register (7.21)

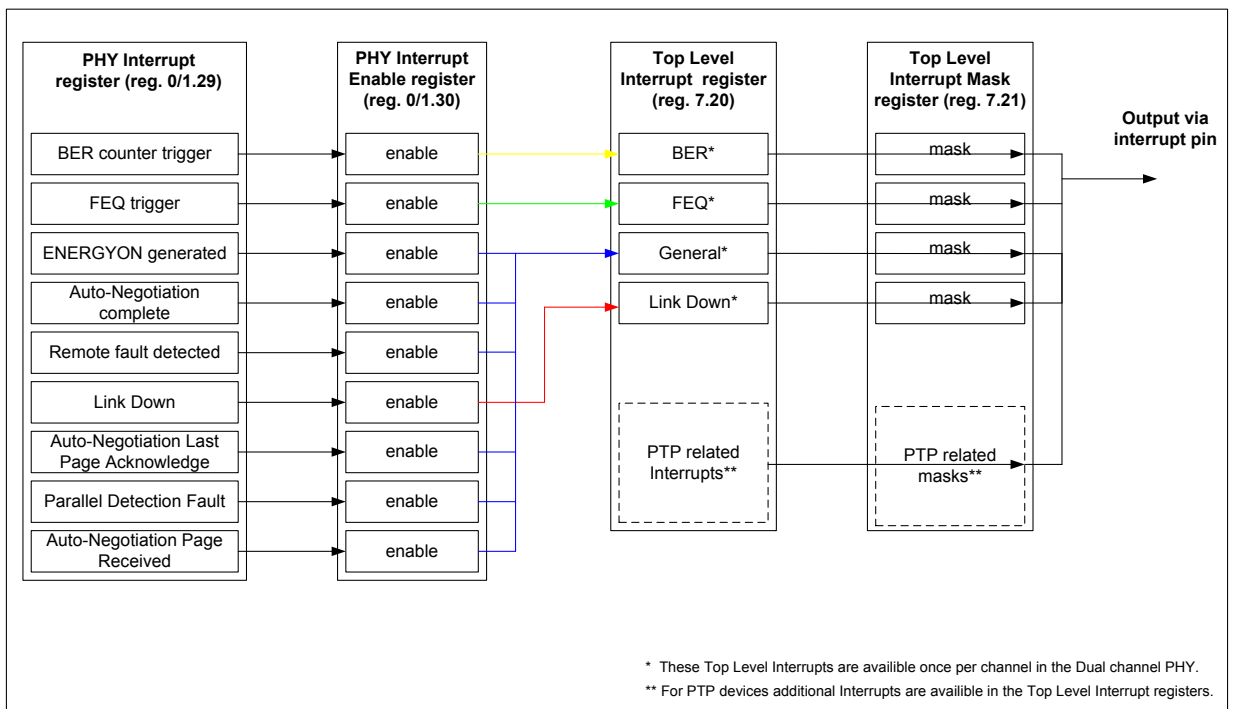
The single bit description of these registers is shown in the UM.

Table 3-1 shows the interrupt management and relationship between the PHY interrupts, the Top Level interrupts, and the interrupt output.

Notes:

- To display the PHY related Interrupts in the Top Level Interrupt register every single Interrupt has to be enabled in the PHY interrupt enable register.
'0' is disabled, '1' is enabled. All bits are '0' by default thus all interrupts disabled.
- If an interrupt is enabled to be flagged in the Top Level Interrupt registers it is directly forwarded to the output pin. To stop the forwarding the related Interrupt has to be masked in the Top Level Interrupt mask register.
'0' is enabled, '1' is masked. All bits are '0' by default thus all interrupts enabled
- To output an interrupt at the INT pin, only the 'enable' bit in the PHY interrupt enable register must be set.
- The interrupts in register 0.29 and 1.29 are cleared by read. The interrupts in 7.20 and the output INT signal are '1' (high) until the interrupt sources in 0.29 and 1.29 are read.
- The PTP related Interrupts of a PTP device are directly generated in the Top Level Interrupt register. Thus they are output enabled by default and need to be masked to be disabled.

Figure 3-1 Interrupt Management



Example:

To output an interrupt signal for the Auto-Negotiation complete: this interrupt needs to be enabled in the interrupt enable register 0/1.30. For Auto-Negotiation complete bit 6 has to be set to '1'. Now this interrupt is displayed in the Top Level Interrupt register in the general Interrupt bit (7.20.0 for PHY0 and 7.20.4 for PHY1) and by default output at the interrupt pin.

Chapter 4 Bit Error Counter

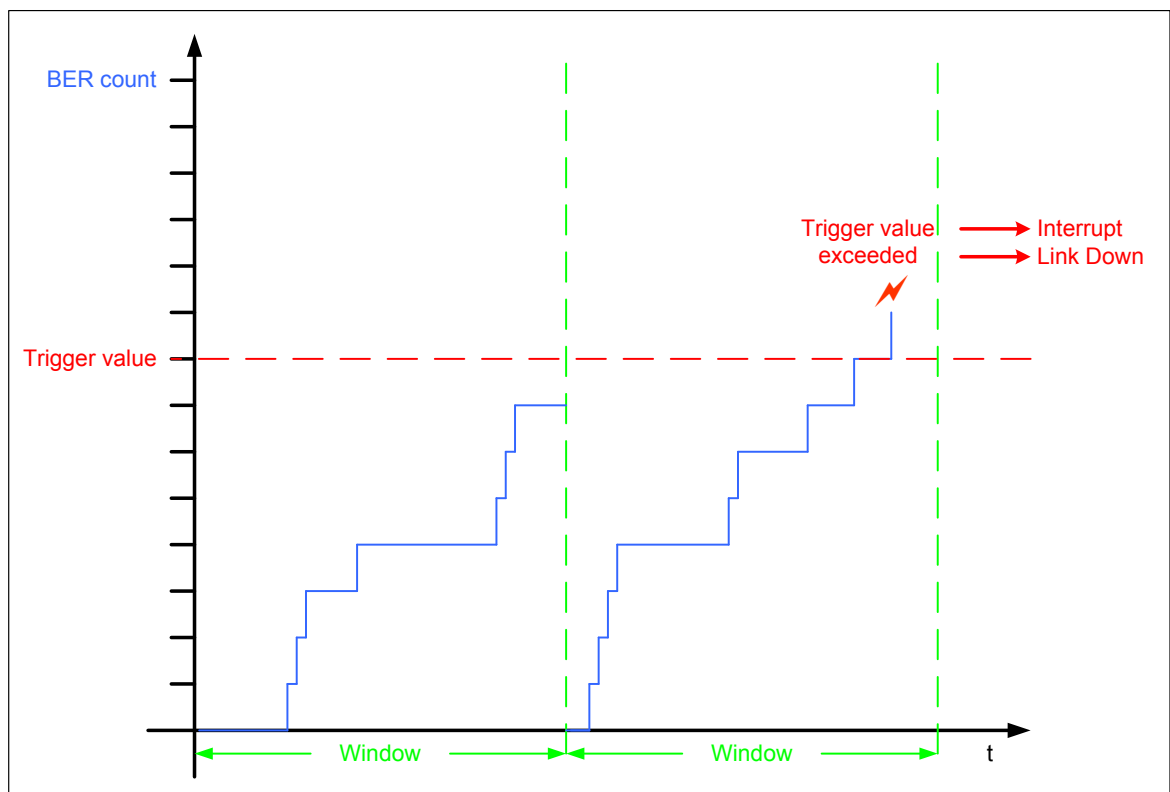
The Bit Error Counter (BER Counter) is a feature that supervises the received Data. All incoming data symbols are checked by the PHY to determine if they are valid or not. Invalid symbols are counted by the BER counter. The BER works not only for Data reception; the idle pattern is also supervised. Here only idle and starting frame delimiters are valid symbols.

The BER counter functions are available in PHY register 23.

Figure 4-1 shows the BER counter function.

The different input and output values are listed and explained below. The bits and names listed in the UM are shown in brackets.

Figure 4-1 BER Counter function



Inputs:

- **Window** (Bit 10:7 - BER_WINDOW)

The *window* defines the duration of the count interval. After this time the BER count is adjusted to zero.

The *window* can be configured via the four bits 10:7. For $n = 1-14$ the *window* is calculated by the formula:

$$0.005 * 2^n \text{ ms}$$

Hence the shortest *window* is 10µs.

Setting '0' (b0000) disables the BER counter.

Setting '15' (b1111) configures the *window* to unlimited run.

The default value is '1' (b0001) -> 10µs

- **Trigger Value** (Bit 13:11 - BER_CNT_TRIG)

The *trigger value* defines the maximum allowed BER count. If this value is exceeded the BER interrupt is flagged, the *link quality indication* is set to '0' and – if the function is enabled – the link is shut down.

The *trigger* can be configured via the three bits 13:11. It is calculated with the set value n in the formula:

$$2^{(n-1)}$$

The default value is '2' (b010)

- **Link Down Enable** (Bit 14 - BER_CNT_LNK_EN)

If the *link down enable* is set to '1' a exceeded *trigger value* causes a direct link down.

It is enabled by default.

Outputs:

- **BER Count** (Bit 6:0 - BER_Count)

The *BER count* displays the current count of Bit Errors. It is reset for every *window*.

For unlimited *window* the *BER count* is updated every 100µs

- **Link Quality Indication** (Bit 15 - BER_LNK_OK)

The *link quality indication* shows if the link up connection is reliable.

It is '1' if the link is up and the *BER count* does not exceed the *trigger value*.

It is '0' if the PHY is not linked up or the *BER count* is higher than the *trigger value*.

Notes:

- The BER counter is enabled by default to disable the BER counter set the *window* to '0'
- The Link analysis by the BER counter is done for every *window*, also after a BER counter reaction event. If the *BER count* is below the *trigger* again within the next *window* the *link quality indication* returns to '1' and the link is set up again.
- The function of the *link down enable* is also responsible for a link down caused by the FEQ monitor. See also chapter 5.

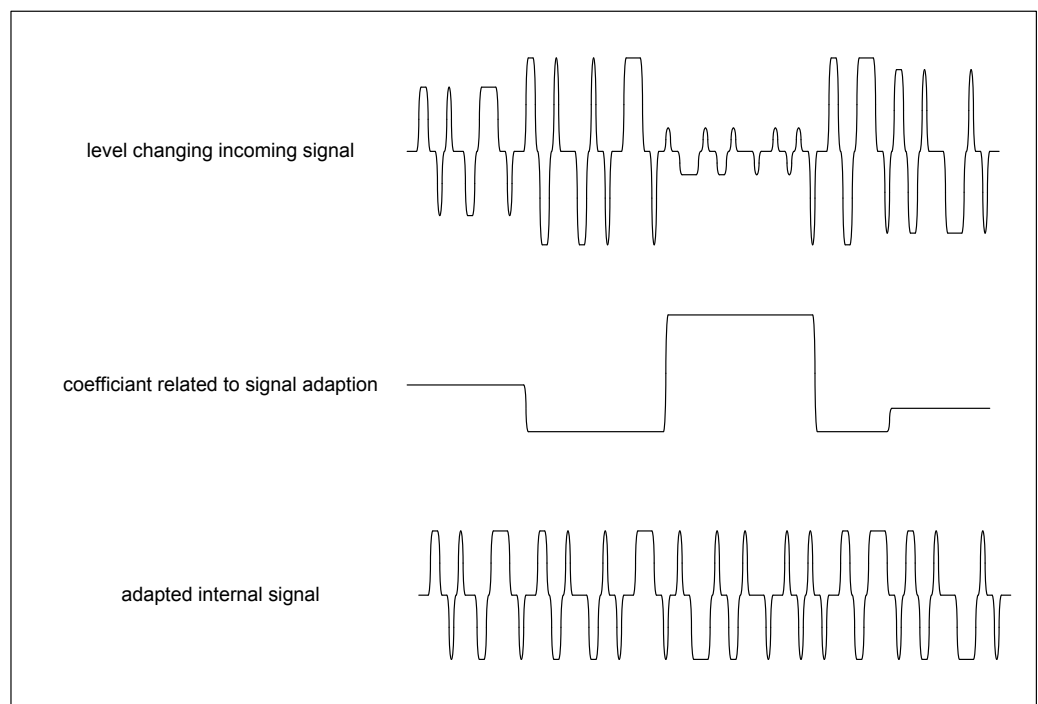
Chapter 5 FEQ Monitor

The FEQ monitor (FEQ = Forward Equalizer) is a feature that supervises the incoming signal. It can be used to detect changes of the quality of an Ethernet connection. This feature is not necessarily developed to detect cable breaks, as this can also be done quite fast by signal detection. The FEQ monitor also detects minor cable changes like single wire breaks or even changes of the cable characteristic. This could be used to provide a 'cable break forecast'. The FEQ monitor causes an Interrupt and can also cause a direct link down. This is done in just a few microseconds.

As the name implies, the FEQ monitor is monitoring the FEQ, a coefficient of the filter structures within the DSP. This FEQ value is directly related to the incoming signal. If the level of the incoming signal is low the FEQ has a higher value - for a high signal level the coefficient is small.

To visualize this behavior figure 5-1 shows simplified relation of such a signal adaption which is fairly comparable with the FEQ.

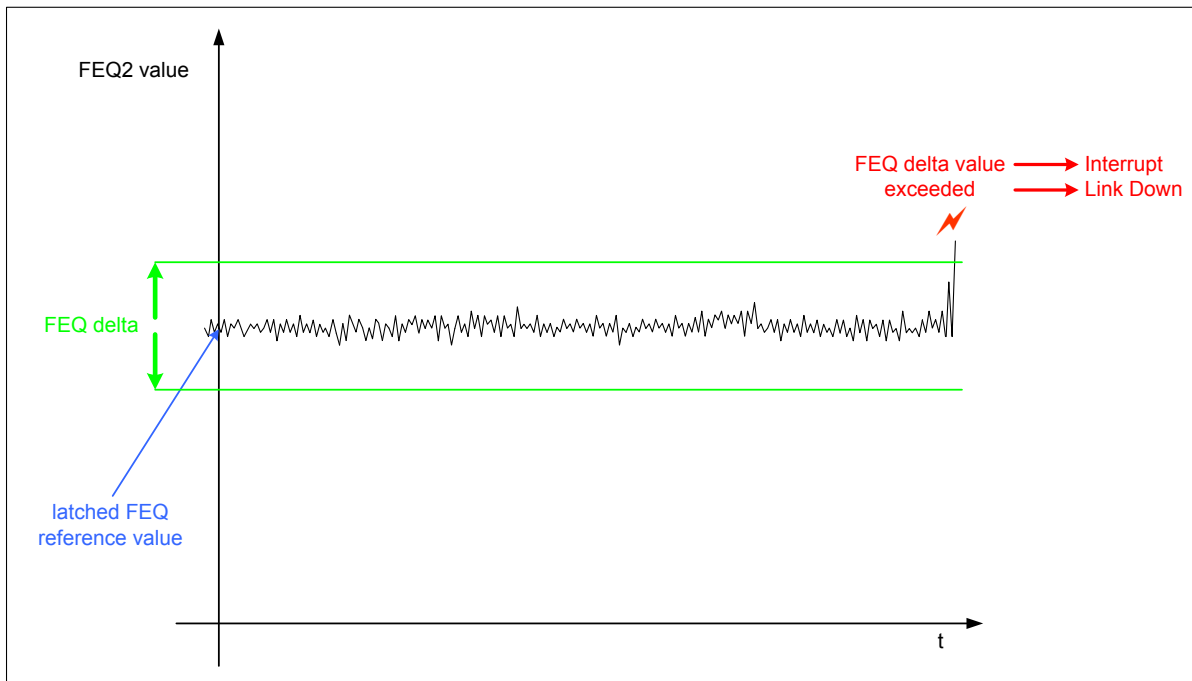
Figure 5-1 Example of a signal adaption to explain the basic FEQ procedure



To use the FEQ monitor individually the user can program an FEQ delta. This delta is the value that is allowed for the FEQ value to differ from a reference value. This reference value is latched by a link up. If the allowed FEQ delta is violated, the FEQ interrupt is flagged. If enabled, this can also trigger a link down. Returning into the FEQ delta range will re-establish the link up. The interrupt is not cleared until read out (see chapter 3).

The functionality of the FEQ monitor is visualized in figure 5-2.

Figure 5-2 FEQ monitor function



The FEQ monitor functions are available in PHY register 24.

The programming of the FEQ monitor is quite easy. The monitoring function is running by default when a copper based Ethernet connection is established. The current FEQ value can be read out in register 24 (all bit 15:0).

To activate the FEQ monitor to generate interrupts and optionally Link Downs a FEQ delta can be written into the same register (again all bits 15:0)

The Link Down function is coupled with the BER Link Down. That means if the Link Down Enable of the BER (Reg. 23 Bit 14) is set to '1' the FEQ monitor will also cause Link Downs.

The FEQ monitor is disabled by writing 0xFFFF to register 24.

Notes:

- The FEQ monitor is based on copper cable connections. Thus it is not operable in FX mode.
- The default value of the FEQ monitor is 0x7FFF (no link)
- Once activated due to set of an FEQ delta it is not possible to recognize if the FEQ monitor is active.

To give a practical example for the absolute FEQ values figure 5-3 shows the relation of the FEQ values and the line length between PHY and a PD.

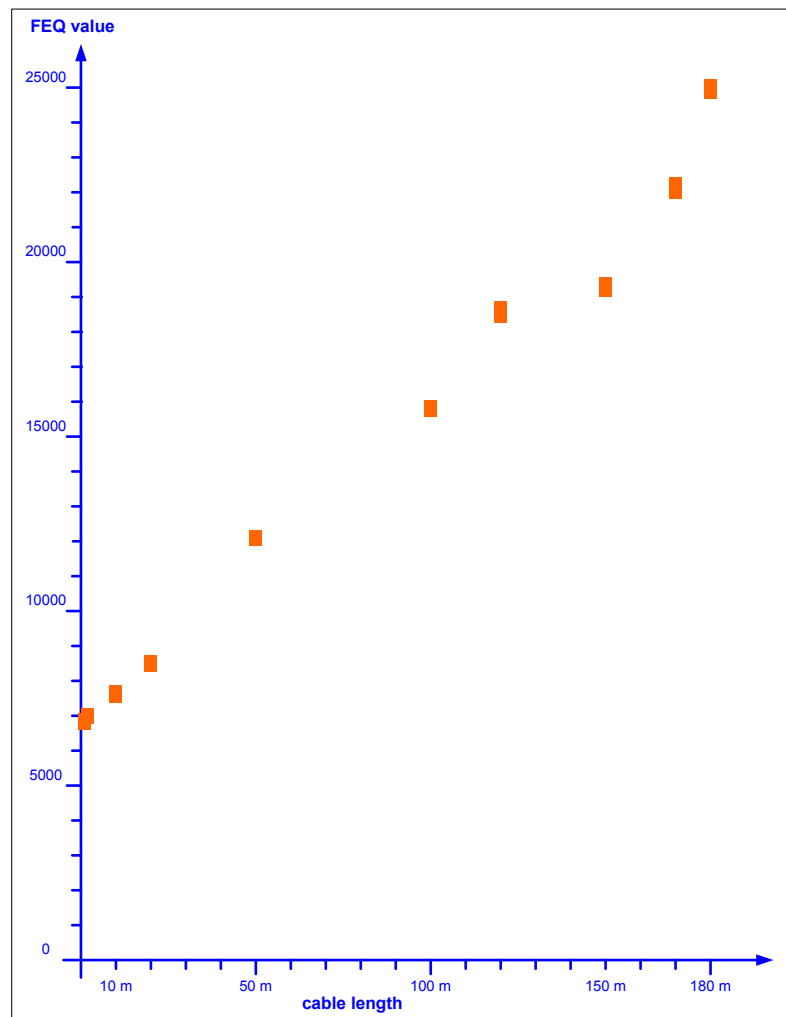
Note:

- These values are result of a measurement and not transferable to other setups.
- The high of the orange blocks show the FEQ value deviation range

To program a useful FEQ delta it is useful to screen the absolute FEQ values by reading the FEQ register. The FEQ value is dependent on all physical parts of an Ethernet connection: Cables, transceivers, connectors, etc..

A good standard value for an FEQ delta can be 0x0400 for a stable connection.

Figure 5-3 FEQ value vs. cable length



Chapter 6 Time Domain Reflectometer

The Time Domain Reflectometer (TDR) is a function that detects cable defects. Furthermore a defect can be localized and its characteristic can be analysed.

To execute a TDR measurement the normal network operation needs to be stopped. It is mandatory that there are no signals on the line that is tested thus no PD should be active.

Within a TDR measurement the PHY sends a well-defined test pulse to the line path. The TDR then waits for a reflection of this pulse. If there is a reflection the pulse is captured and its characteristic analysed.

The TDR is controlled via PHY registers 25 and 26. Inputs and Outputs and its detailed configuration are described below:

Inputs:

- **Line Selection** (Reg.25 Bit 5 – *DIAG_SEL_LINE*)

To choose which line is tested this bit should be set to '1' for TX path and to '0' for RX path.
- **Pulse Width** (Reg.25 Bit 4:0 – *PW_DIAG*)

This value defines the pulse width of the test pulse. The value in these 5 bits multiplied with 8ns is the pulse width of the outgoing test pulse. *Pulse widths* from 8ns to 246ns are possible.
- **Trigger** (Reg.25 Bit 13:8 – *ADC_Trigger*)

This *trigger* defines the voltage level that is needed to react on a reflected/incoming pulse. The resolution is 100mV per count.
- **Window** (Reg.26 Bit 15:8 – *CNT_WINDOW*)

This naming is a little bit misleading because this parameter does not define a time range. It defines the time when the capturing is enabled. Before this particular time all signals are ignored. This parameter is important to avoid capturing the outgoing pulse. How to program useful values is explained in the notes below and in figure 6-1.
- **Initiate Diagnose** (Reg.25 Bit 14 – *DIAG_INIT*)

Setting this bit initiates a TDR measurement.

Outputs:

- **Diagnose Done** (Reg.25 Bit 7 – *DIAG_Done*)

The *diagnose done* bit is set if a measurement is finished. This can be if a reflected wave is captured or after a timeout without any incoming signal.
- **Polarity** (Reg.25 Bit 6 – *DIAG_POL*)

The *polarity* bit shows the polarity of the last captured reflected pulse. '0' stands for a positive pulse, '1' for a negative one.

A negative pulse is reflected due to a short circuit of both paths. An open cable or a short to another signal or shield path result in a reflection.

- **Counter Value** (Reg.26 Bit 7:0 – *DIAGCNT*)

This is the most important output of the TDR. The counter stops when a reflected pulse is captured. With this count the distance to a defect can be calculated. For this calculation the internal delay has to be considered. The outgoing test pulse is sent to the line after 11 counts. One count of the internal counter represents 8ns.

A pulse on a line travels at about $2 * 10^8 \frac{m}{s}$. This means a pulse passes 1.6m in 8ns. Because a reflected pulse is passing the line twice this results in a factor of 0.8m per count.

Thus the distance to the defect can be calculated by the formula:

$$(DIAGCNT - 11) * 0.8 m$$

Note:

The runtime of a pulse on a cable depends on its exact physical characteristics. To have an exact TDR calculation it makes sense to define the factor with one of the used cables. This can be done with a long open cable with known length.

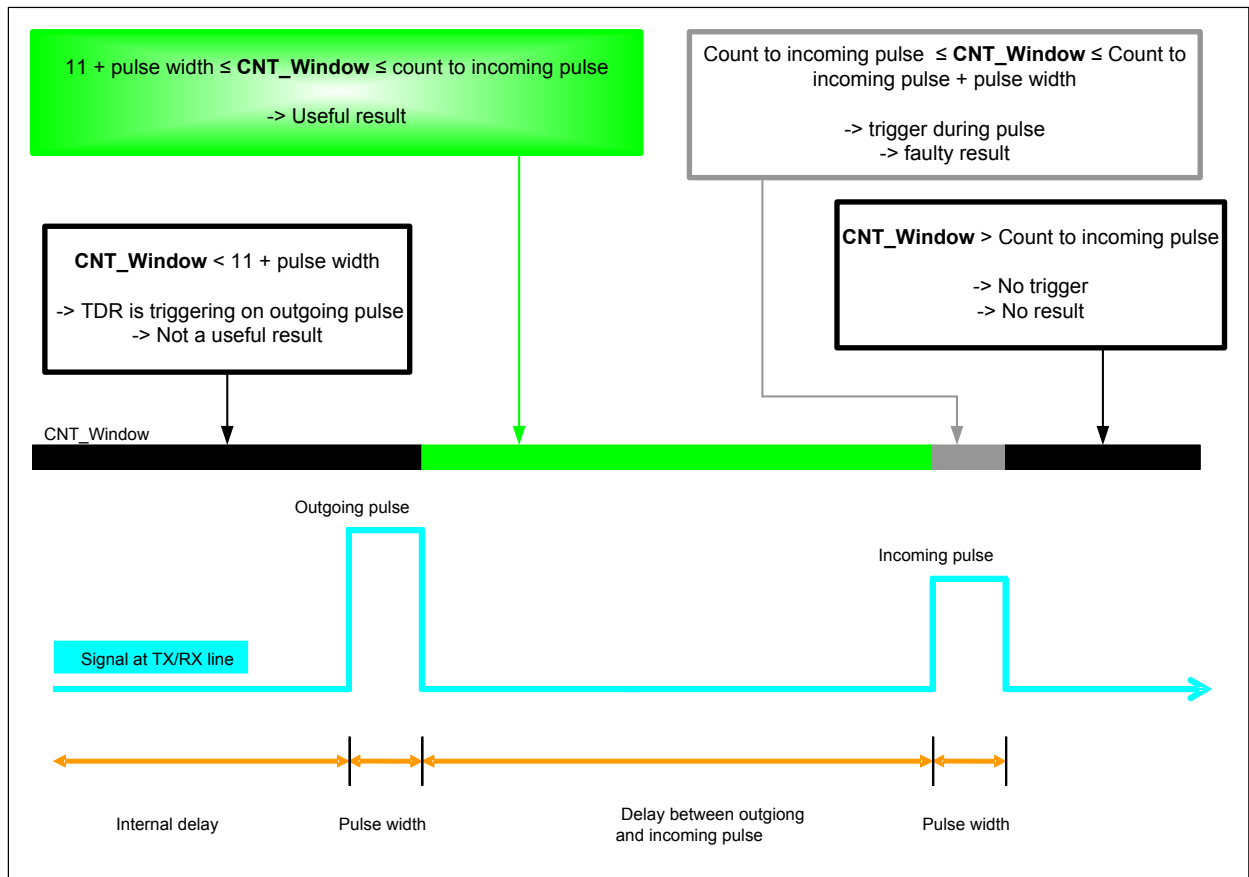
- **Pulse Level** (Reg.25 Bit 13:8 – *ADC_MAX_VALUE*)

The *pulse level* shows the voltage level of a captured pulse. This output value shares its bits with the input of the *trigger level*. After a measurement the *pulse level* can be read out. Similar to the *trigger* value this value has a resolution of 100mV. Negative values are shown in two's complement.

Notes:

- To use the TDR function the PHY should be set to 100Mbit fixed mode first.
- There should be no signals on the line. PD should be quiet or disabled.
- AutoMDIX has to be disabled.
- A useful pulse width depends on the distance to a possible defect. A small distance needs short pulses so that outgoing pulse and reflection do not overlap. For longer distances longer test pulses are necessary. A short pulse can be damped by the long line.
- As already explained the TDR has an internal delay of 11 counts. Thus the *window* has to set to a higher value to avoid a trigger at the outgoing pulse. Also the pulse width has to be considered. The TDR *window* value should be higher than the sum of internal delay and *pulse width*. See Figure 6-1.
- The TDR has no result for 100Ω termination. Resistive defects between the paths lower than this have similar characteristic to a short; a negative reflection. Higher resistive defects result in a positive reflection.

Figure 6-1 TDR window



Useful examples for a TDR configuration in the TDR registers 26 (0x1A) and 25 (0x199) are:

To detect a defect within a short connection (<50m):

Write 0x0D00 to register 26

Write 0x4321 to register 25

Read register 26 and 25

To detect a defect in a mid-range (15m – 100m)

Write 0x1800 to register 26

Write 0x432A to register 25

Read register 26 and 25

To detect a defect far away (>50m)

Write 0x2B00 to register 26

Write 0x433F to register 25

Read register 26 and 25

As the defect position is not known before the measurement it is useful to program a combination of measurements for longer cable connections.

Chapter 7 Quick Auto-Negotiation

The Quick Auto-Negotiation is an option to speed up the long duration of the Auto-Negotiation (Autoneg) process.

A simplified state diagram is shown in figure 7-1.

There are different timers that influence the duration of the Autoneg process. The two longest timers which have the main impact of the overall link up time are the **break link timer** and the **autoneg wait timer**.

To speed up the Autoneg process the Renesas PHY ASSP can be configured to shorten these timers. Both timers are highlighted in the diagram and explained in detail below:

The **break link timer** is started at the beginning of every new connection process: After a device start-up, an Autoneg enable, and after any link down or link loss event. While this timer is active, the PHY device is on hold. There is no transmit and no listening to the line. This timer guarantees that a PD also lost its link and prepares for a (re-)connection. The specified duration of this timer is 1200 - 1500ms.

After this break link timer the PHY starts sending FLPs (Fast Link Pulses) and listening to the line (Ability Detect).

If FLPs are received from a PD that supports Autoneg, the Autoneg FLP exchange starts.

If the PHY receives 10BT NLPs (normal links Pulses) or a 100BT idle pattern, then a parallel detection is started. The PHY stops sending FLPs, starts the **autoneg wait timer** and analyses the incoming signal. The specified duration of this timer is 500 - 1000ms.

Table 7-1 shows the timer values of the Renesas PHY ASSP regarding to the Autoneg mode.

Table 7-2 gives some examples for the overall linkup time of two Renesas PHYs regarding to the used modes.

Figure 7-1 Auto-Negotiation process

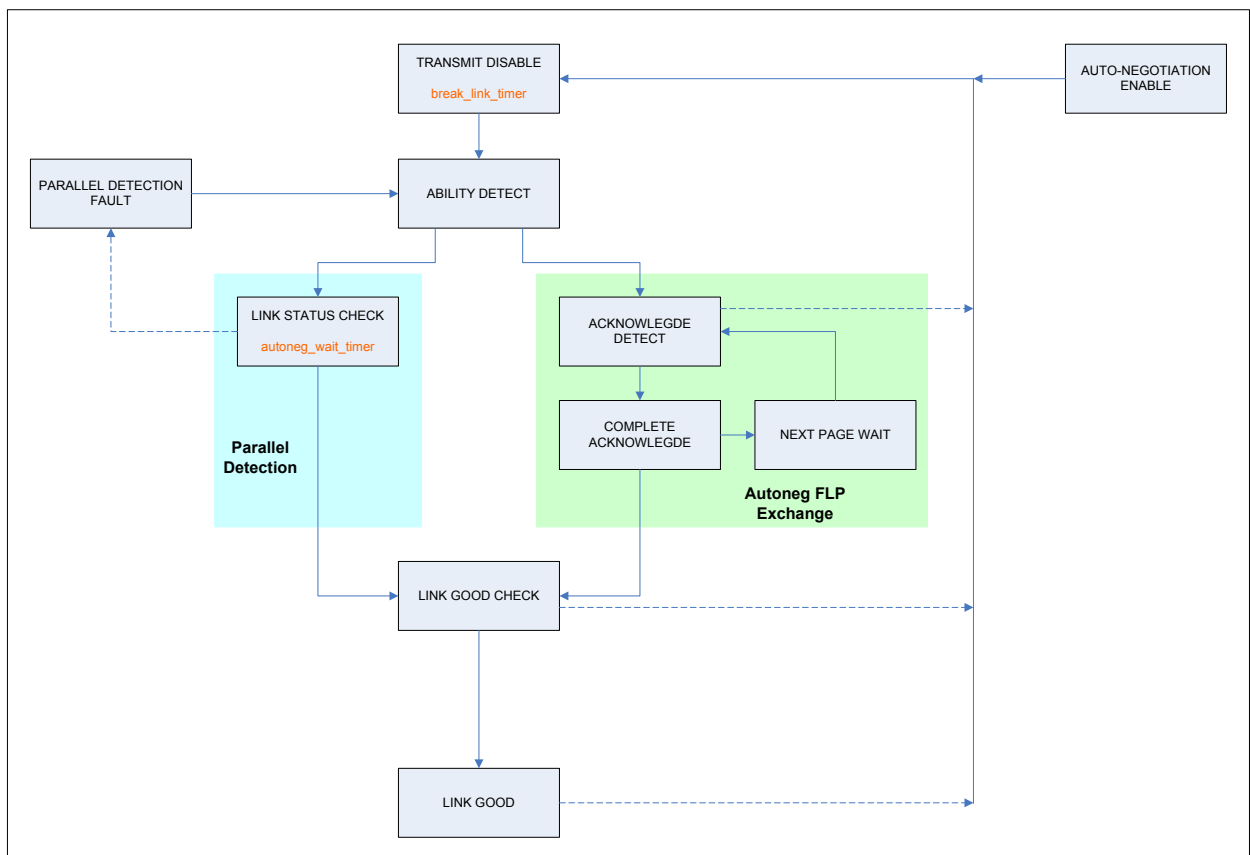


Table 7-1 Timer values

Auto-Negotiation Mode	Break_Link_Timer	Autoneg_wait_timer
Standard Auto-Negotiation	1250 ms	850 ms
Quick Auto-Negotiation	80 ms	35 ms

Table 7-2 Link-up times

PHY mode	PHY mode PD	Link-up time in ms
Standard Auto-Negotiation	Standard Auto-Negotiation	1500
Quick Auto-Negotiation	Quick Auto-Negotiation	~240
Standard Auto-Negotiation	100BT fixed	2110
Quick Auto-Negotiation	100BT fixed	120

Notes:

- Quick-Autoneg is an intended violation of the IEEE specification.
- Quick-Autoneg PHYs are still compatible with PHYs using standard Autoneg and all standard PHYs of other vendors.
- Link-up times of standard Autoneg combined with a Quick Autoneg are in between the shown link-up times and depend on the current states.

General Precautions in the Handling of MPU/MCU Products

The following usage notes are applicable to all MPU/MCU products from Renesas. For detailed usage notes on the products covered by this manual, refer to the relevant sections of the manual. If the descriptions under General Precautions in the Handling of MPU/MCU Products and in the body of the manual differ from each other, the description in the body of the manual takes precedence.

1. Handling of Unused Pins

Handle unused pins in accord with the directions given under Handling of Unused Pins in the manual.

The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible. Unused pins should be handled as described under Handling of Unused Pins in the manual.

2. Processing at Power-on

The state of the product is undefined at the moment when power is supplied.

The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the moment when power is supplied.

In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the moment when power is supplied until the reset process is completed.

In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the moment when power is supplied until the power reaches the level at which resetting has been specified.

3. Prohibition of Access to Reserved Addresses

Access to reserved addresses is prohibited.

The reserved addresses are provided for the possible future expansion of functions. Do not access these addresses; the correct operation of LSI is not guaranteed if they are accessed.

4. Clock Signals

After applying a reset, only release the reset line after the operating clock signal has become stable. When switching the clock signal during program execution, wait until the target clock signal has stabilized.

When the clock signal is generated with an external resonator (or from an external oscillator) during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Moreover, when switching to a clock signal produced with an external resonator (or by an external oscillator) while program execution is in progress, wait until the target clock signal is stable.

5. Differences between Products

Before changing from one product to another, i.e. to one with a different part number, confirm that the change will not lead to problems.

The characteristics of MPU/MCU in the same group but having different part numbers may differ because of the differences in internal memory capacity and layout pattern. When changing to products of different part numbers, implement a system-evaluation test for each of the products.

Notice

1. All information included in this document is current as of the date this document is issued. Such information, however, is subject to change without any prior notice. Before purchasing or using any Renesas Electronics products listed herein, please confirm the latest product information with a Renesas Electronics sales office. Also, please pay regular and careful attention to additional and different information to be disclosed by Renesas Electronics such as that disclosed through our website.
2. Renesas Electronics does not assume any liability for infringement of patents, copyrights, or other intellectual property rights of third parties by or arising from the use of Renesas Electronics products or technical information described in this document. No license, express, implied or otherwise, is granted hereby under any patents, copyrights or other intellectual property rights of Renesas Electronics or others.
3. You should not alter, modify, copy, or otherwise misappropriate any Renesas Electronics product, whether in whole or in part.
4. Descriptions of circuits, software and other related information in this document are provided only to illustrate the operation of semiconductor products and application examples. You are fully responsible for the incorporation of these circuits, software, and information in the design of your equipment. Renesas Electronics assumes no responsibility for any losses incurred by you or third parties arising from the use of these circuits, software, or information.
5. When exporting the products or technology described in this document, you should comply with the applicable export control laws and regulations and follow the procedures required by such laws and regulations. You should not use Renesas Electronics products or the technology described in this document for any purpose relating to military applications or use by the military, including but not limited to the development of weapons of mass destruction. Renesas Electronics products and technology may not be used for or incorporated into any products or systems whose manufacture, use, or sale is prohibited under any applicable domestic or foreign laws or regulations.
6. Renesas Electronics has used reasonable care in preparing the information included in this document, but Renesas Electronics does not warrant that such information is error free. Renesas Electronics assumes no liability whatsoever for any damages incurred by you resulting from errors in or omissions from the information included herein.
7. Renesas Electronics products are classified according to the following three quality grades: "Standard", "High Quality", and "Specific". The recommended applications for each Renesas Electronics product depends on the product's quality grade, as indicated below. You must check the quality grade of each Renesas Electronics product before using it in a particular application. You may not use any Renesas Electronics product for any application categorized as "Specific" without the prior written consent of Renesas Electronics. Further, you may not use any Renesas Electronics product for any application for which it is not intended without the prior written consent of Renesas Electronics. Renesas Electronics shall not be in any way liable for any damages or losses incurred by you or third parties arising from the use of any Renesas Electronics product for an application categorized as "Specific" or for which the product is not intended where you have failed to obtain the prior written consent of Renesas Electronics.

The quality grade of each Renesas Electronics product is "Standard" unless otherwise expressly specified in a Renesas Electronics data sheets or data books, etc.

"Standard": Computers; office equipment; communications equipment; test and measurement equipment; audio and visual equipment; home electronic appliances; machine tools; personal electronic equipment; and industrial robots.

"High Quality": Transportation equipment (automobiles, trains, ships, etc.); traffic control systems; anti-disaster systems; anti-crime systems; safety equipment; and medical equipment not specifically designed for life support.

"Specific": Aircraft; aerospace equipment; submersible repeaters; nuclear reactor control systems; medical equipment or systems for life support (e.g. artificial life support devices or systems), surgical implantations, or healthcare intervention (e.g. excision, etc.), and any other applications or purposes that pose a direct threat to human life.

8. You should use the Renesas Electronics products described in this document within the range specified by Renesas Electronics, especially with respect to the maximum rating, operating supply voltage range, movement power voltage range, heat radiation characteristics, installation and other product characteristics. Renesas Electronics shall have no liability for malfunctions or damages arising out of the use of Renesas Electronics products beyond such specified ranges.
9. Although Renesas Electronics endeavors to improve the quality and reliability of its products, semiconductor products have specific characteristics such as the occurrence of failure at a certain rate and malfunctions under certain use conditions. Further, Renesas Electronics products are not subject to radiation resistance design. Please be sure to implement safety measures to guard them against the possibility of physical injury, and injury or damage caused by fire in the event of the failure of a Renesas Electronics product, such as safety design for

hardware and software including but not limited to redundancy, fire control and malfunction prevention, appropriate treatment for aging degradation or any other appropriate measures. Because the evaluation of microcomputer software alone is very difficult, please evaluate the safety of the final products or system manufactured by you.

10. Please contact a Renesas Electronics sales office for details as to environmental matters such as the environmental compatibility of each Renesas Electronics product. Please use Renesas Electronics products in compliance with all applicable laws and regulations that regulate the inclusion or use of controlled substances, including without limitation, the EU RoHS Directive. Renesas Electronics assumes no liability for damages or losses occurring as a result of your noncompliance with applicable laws and regulations.
11. This document may not be reproduced or duplicated, in any form, in whole or in part, without prior written consent of Renesas Electronics.
12. Please contact a Renesas Electronics sales office if you have any questions regarding the information contained in this document or Renesas Electronics products, or if you have any other inquiries.

(Note 1) "Renesas Electronics" as used in this document means Renesas Electronics Corporation and also includes its majority-owned subsidiaries.

(Note 2) "Renesas Electronics product(s)" means any product developed or manufactured by or for Renesas Electronics.

**Sales Offices**

Renesas Electronics Corporation

www.renesas.com

Refer to "<http://www.renesas.com/>" for the latest and detailed information.

Renesas Electronics America Inc.

2880 Scott Boulevard Santa Clara, CA 95050-2554, U.S.A.

Tel: +1-408-588-6000, Fax: +1-408-588-6130

Renesas Electronics Canada Limited

1101 Nicholson Road, Newmarket, Ontario L3Y 9C3, Canada

Tel: +1-905-898-5441, Fax: +1-905-898-3220

Renesas Electronics Europe Limited

Dukes Meadow, Millboard Road, Bourne End, Buckinghamshire, SL8 5FH, U.K

Tel: +44-1628-585-100, Fax: +44-1628-585-900

Renesas Electronics Europe GmbH

Arcadiastrasse 10, 40472 Düsseldorf, Germany

Tel: +49-211-6503-0, Fax: +49-211-6503-1327

Renesas Electronics (China) Co., Ltd.

7th Floor, Quantum Plaza, No.27 ZhiChunLu Haidian District, Beijing 100083, P.R.China

Tel: +86-10-8235-1155, Fax: +86-10-8235-7679

Renesas Electronics (Shanghai) Co., Ltd.

Unit 204, 205, AZIA Center, No.1233 Lujiazui Ring Rd., Pudong District, Shanghai 200120, China

Tel: +86-21-5877-1818, Fax: +86-21-6887-7858 / -7898

Renesas Electronics Hong Kong Limited

Unit 1601-1613, 16/F., Tower 2, Grand Century Place, 193 Prince Edward Road West, Mongkok, Kowloon, Hong Kong

Tel: +852-2886-9318, Fax: +852 2886-9022/9044

Renesas Electronics Taiwan Co., Ltd.

7F, No. 363 Fu Shing North Road Taipei, Taiwan, R.O.C.

Tel: +886-2-8175-9600, Fax: +886 2-8175-9670

Renesas Electronics Singapore Pte. Ltd.

1 harbourFront Avenue, #06-10, keppel Bay Tower, Singapore 098632

Tel: +65-6213-0200, Fax: +65-6278-8001

Renesas Electronics Malaysia Sdn.Bhd.

Unit 906, Block B, Menara Amcorp, Amcorp Trade Centre, No. 18, Jln Persiaran Barat, 46050 Petaling Jaya,

Selangor Darul Ehsan, Malaysia

Tel: +60-3-7955-9390, Fax: +60-3-7955-9510

Renesas Electronics Korea Co., Ltd.

11F., Samik Lavied' or Bldg., 720-2 Yeoksam-Dong, Kangnam-Ku, Seoul 135-080, Korea

Tel: +82-2-558-3737, Fax: +82-2-558-5141