To our customers,

# Old Company Name in Catalogs and Other Documents

On April 1st, 2010, NEC Electronics Corporation merged with Renesas Technology Corporation, and Renesas Electronics Corporation took over all the business of both companies. Therefore, although the old company name remains in this document, it is a valid Renesas Electronics document. We appreciate your understanding.

Renesas Electronics website: http://www.renesas.com

April 1st, 2010
Renesas Electronics Corporation

Issued by: Renesas Electronics Corporation (http://www.renesas.com)

Send any inquiries to http://www.renesas.com/inquiry.

# Notice

1. All information included in this document is current as of the date this document is issued. Such information, however, is subject to change without any prior notice. Before purchasing or using any Renesas Electronics products listed herein, please confirm the latest product information with a Renesas Electronics sales office. Also, please pay regular and careful attention to additional and different information to be disclosed by Renesas Electronics such as that disclosed through our website.
2. Renesas Electronics does not assume any liability for infringement of patents, copyrights, or other intellectual property rights of third parties by or arising from the use of Renesas Electronics products or technical information described in this document. No license, express, implied or otherwise, is granted hereby under any patents, copyrights or other intellectual property rights of Renesas Electronics or others.
3. You should not alter, modify, copy, or otherwise misappropriate any Renesas Electronics product, whether in whole or in part.
4. Descriptions of circuits, software and other related information in this document are provided only to illustrate the operation of semiconductor products and application examples. You are fully responsible for the incorporation of these circuits, software, and information in the design of your equipment. Renesas Electronics assumes no responsibility for any losses incurred by you or third parties arising from the use of these circuits, software, or information.
5. When exporting the products or technology described in this document, you should comply with the applicable export control laws and regulations and follow the procedures required by such laws and regulations. You should not use Renesas Electronics products or the technology described in this document for any purpose relating to military applications or use by the military, including but not limited to the development of weapons of mass destruction. Renesas Electronics products and technology may not be used for or incorporated into any products or systems whose manufacture, use, or sale is prohibited under any applicable domestic or foreign laws or regulations.
6. Renesas Electronics has used reasonable care in preparing the information included in this document, but Renesas Electronics does not warrant that such information is error free. Renesas Electronics assumes no liability whatsoever for any damages incurred by you resulting from errors in or omissions from the information included herein.
7. Renesas Electronics products are classified according to the following three quality grades: "Standard", "High Quality", and "Specific". The recommended applications for each Renesas Electronics product depends on the product's quality grade, as indicated below. You must check the quality grade of each Renesas Electronics product before using it in a particular application. You may not use any Renesas Electronics product for any application categorized as "Specific" without the prior written consent of Renesas Electronics. Further, you may not use any Renesas Electronics product for any application for which it is not intended without the prior written consent of Renesas Electronics. Renesas Electronics shall not be in any way liable for any damages or losses incurred by you or third parties arising from the use of any Renesas Electronics product for an application categorized as "Specific" or for which the product is not intended where you have failed to obtain the prior written consent of Renesas Electronics. The quality grade of each Renesas Electronics product is "Standard" unless otherwise expressly specified in a Renesas Electronics data sheets or data books, etc.

   "Standard": Computers; office equipment; communications equipment; test and measurement equipment; audio and visual equipment; home electronic appliances; machine tools; personal electronic equipment; and industrial robots.

   "High Quality": Transportation equipment (automobiles, trains, ships, etc.); traffic control systems; anti-disaster systems; anti-crime systems; safety equipment; and medical equipment not specifically designed for life support.

   "Specific": Aircraft; aerospace equipment; submersible repeaters; nuclear reactor control systems; medical equipment or systems for life support (e.g. artificial life support devices or systems), surgical implantations, or healthcare intervention (e.g. excision, etc.), and any other applications or purposes that pose a direct threat to human life.
8. You should use the Renesas Electronics products described in this document within the range specified by Renesas Electronics, especially with respect to the maximum rating, operating supply voltage range, movement power voltage range, heat radiation characteristics, installation and other product characteristics. Renesas Electronics shall have no liability for malfunctions or damages arising out of the use of Renesas Electronics products beyond such specified ranges.
9. Although Renesas Electronics endeavors to improve the quality and reliability of its products, semiconductor products have specific characteristics such as the occurrence of failure at a certain rate and malfunctions under certain use conditions. Further, Renesas Electronics products are not subject to radiation resistance design. Please be sure to implement safety measures to guard them against the possibility of physical injury, and injury or damage caused by fire in the event of the failure of a Renesas Electronics product, such as safety design for hardware and software including but not limited to redundancy, fire control and malfunction prevention, appropriate treatment for aging degradation or any other appropriate measures. Because the evaluation of microcomputer software alone is very difficult, please evaluate the safety of the final products or system manufactured by you.
10. Please contact a Renesas Electronics sales office for details as to environmental matters such as the environmental compatibility of each Renesas Electronics product. Please use Renesas Electronics products in compliance with all applicable laws and regulations that regulate the inclusion or use of controlled substances, including without limitation, the EU RoHS Directive. Renesas Electronics assumes no liability for damages or losses occurring as a result of your noncompliance with applicable laws and regulations.
11. This document may not be reproduced or duplicated, in any form, in whole or in part, without prior written consent of Renesas Electronics.
12. Please contact a Renesas Electronics sales office if you have any questions regarding the information contained in this document or Renesas Electronics products, or if you have any other inquiries.

(Note 1) "Renesas Electronics" as used in this document means Renesas Electronics Corporation and also includes its majority-owned subsidiaries.

(Note 2) "Renesas Electronics product(s)" means any product developed or manufactured by or for Renesas Electronics.

# H8SX Family

## PPG Normal Operation (Unit 0) – DMAC Transfer –

### Introduction

This application note describes using the normal operation mode of the programmable pulse generator (PPG) function to produce pulse output. In addition, the DMA controller (DTC) is used to transfer the next unit of data for pulse output.

Coordinated operation with the DMAC the load on the CPU, enabling transfer of the next unit of data as the pulse output.

### Target Devices

H8SX/1648 Group, H8SX/1648A Group, H8SX/1648L Group, H8SX/1648G Group, H8SX/1648H Group

### Preface

This program can be used with other H8SX Family MCUs that have the same internal I/O registers as the devices on which operation has been confirmed.

Check the latest version of the manual for any additions and modifications to functions. Careful evaluation is recommended before using this application note.

### Contents

## 1. Specifications

The specifications of this application note cover using the PPG function and DMAC transfer to generate pulse output for 16 bytes of data. Then the DMAC performs a repeat transfer and pulse output is generated for 16 bytes of data a second time.

Figure 1 shows an overview of the operations described in this application note. The detailed specifications for the operations described in this application note are listed below.

- The PPG pulse output group used is group 0 (pins PO0 to PO3).
- Normal operation in direct output mode is used for PPG pulse output.
- The 16-bit timer pulse unit (TPU) channel 0 compare match is used as the PPG activation source.
- The TPU compare match period is set to 20 µs.
- The TPU output compare match is used as the DMAC activation source.
- The repeat transfer mode of the DMAC is used to transfer 16 bytes of data to the next data register (NDR) of the PPG.
- The data transferred by the DMAC consists of 16 bytes as follows: H'00, H'11, H'22, …, H'DD, H'EE, H'FF.

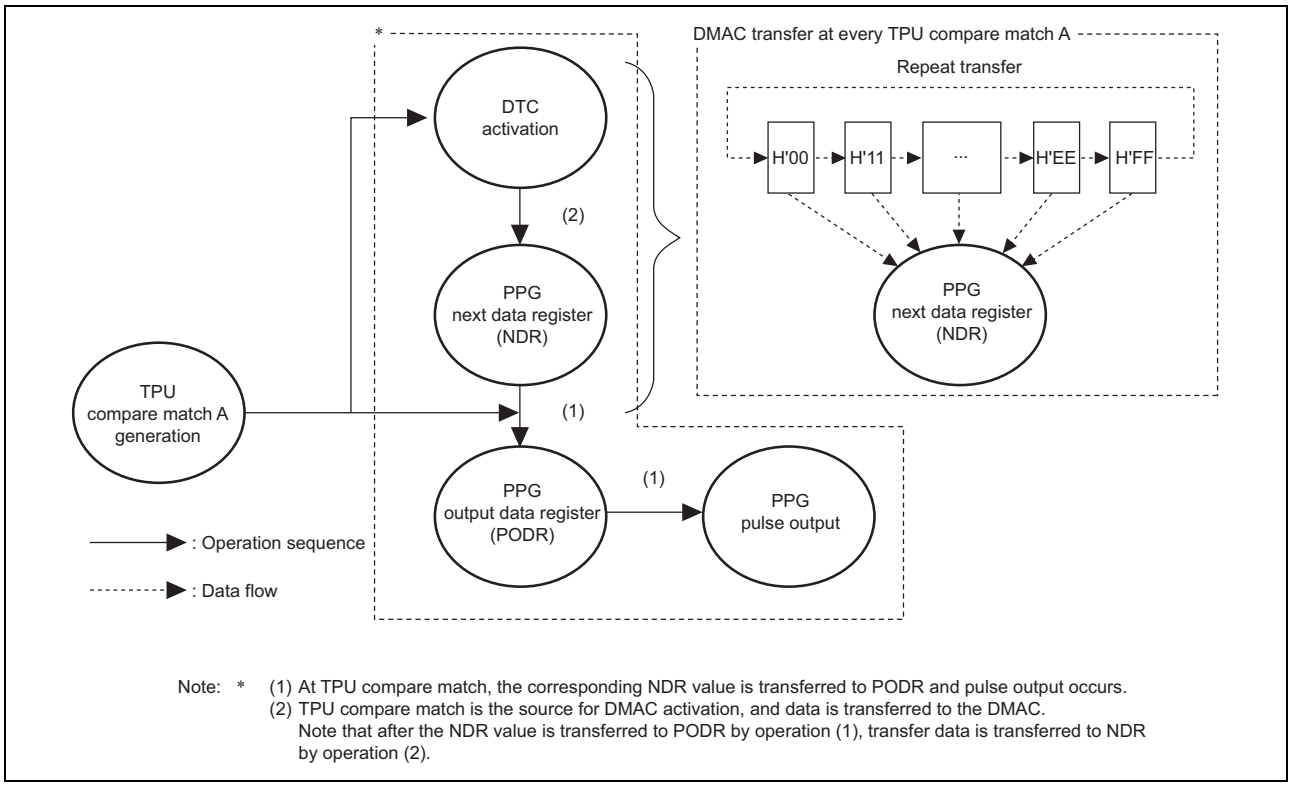


**Figure 1 Operation Overview**

## 2. Applicable Conditions

**Table 1 Applicable Conditions**

| Item | Description |
|---|---|
| Operating frequency | Input clock: 12.5 MHz<br>System clock(Iϕ): 50 MHz (12.5 MHz multiplied by 4)<br>Peripheral module clock (Pϕ): 25 MHz (12.5 MHz multiplied by 2)<br>External bus clock (Bϕ): 50 MHz (12.5 MHz multiplied by 4) |
| Operating voltage | 3.3V |
| Operating mode | Mode 7 (MD2 = 1, MD1 = 1, MD0 = 1) |
| Integrated development environment | High-performance Embedded Workshop (HEW) Ver.4.04.01 |
| C/C++ compiler | Renesas Technology<br>H8S/300, H8/300 C/C++ Compiler (V6.02.00) |
| Compile options | -cpu = H8SXA:24MD, -optimize = 1 |
| Optimizing linkage editor | Renesas Technology<br>Optimizing Linkage Editor (V9.03.00) |
| Linker options | start = PResetPRG,PIntPRG/0400,<br>P,C,C$DSEC,C$BSEC,D/0800,<br>B,R/0FF2000,<br>S/0FFBE00 |

# 3. Functions Used

## 3.1 Programmable Pulse Generator

The programmable pulse generator (PPG) generates pulse output by using the 16-bit timer pulse unit (TPU) as a time base. The PPG comprises 4-bit units (groups 7 to 0) that can operate either simultaneously or independently.

Figure 2 shows a schematic diagram of the PPG. PPG pulse output is enabled when the corresponding bits in the next data enable register (NDER) are set to 1. An initial output value is determined by its corresponding the output data register (PODR) initial setting. When the compare match event specified by the PPG output control register PCR occurs, the corresponding the next data register (NDR) bit contents are transferred to PODR to update the output values. Sequential output of data of up to 16 bits is possible by writing new output data to NDR before the next compare match.

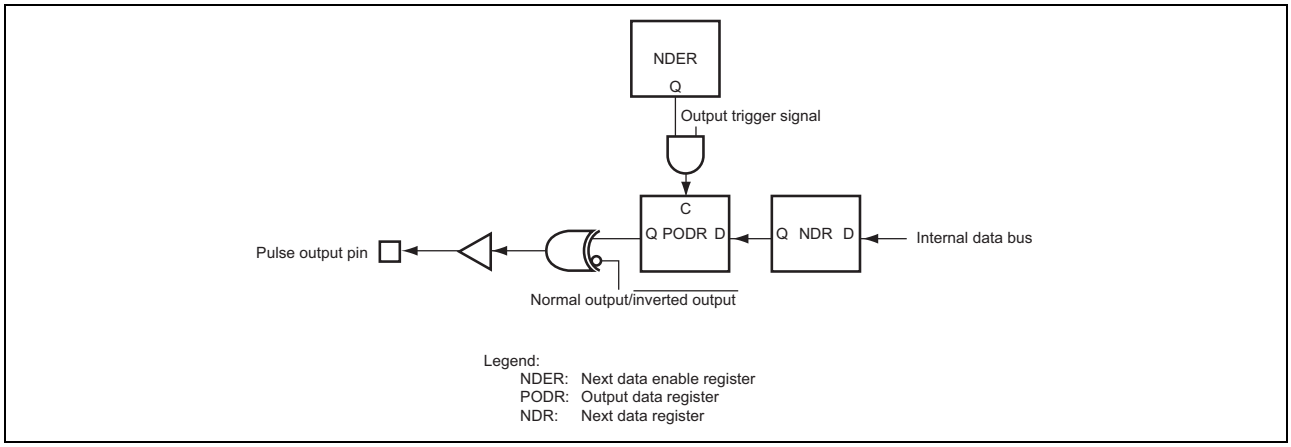


**Figure 2 Schematic Diagram of PPG**

## 4. Operation

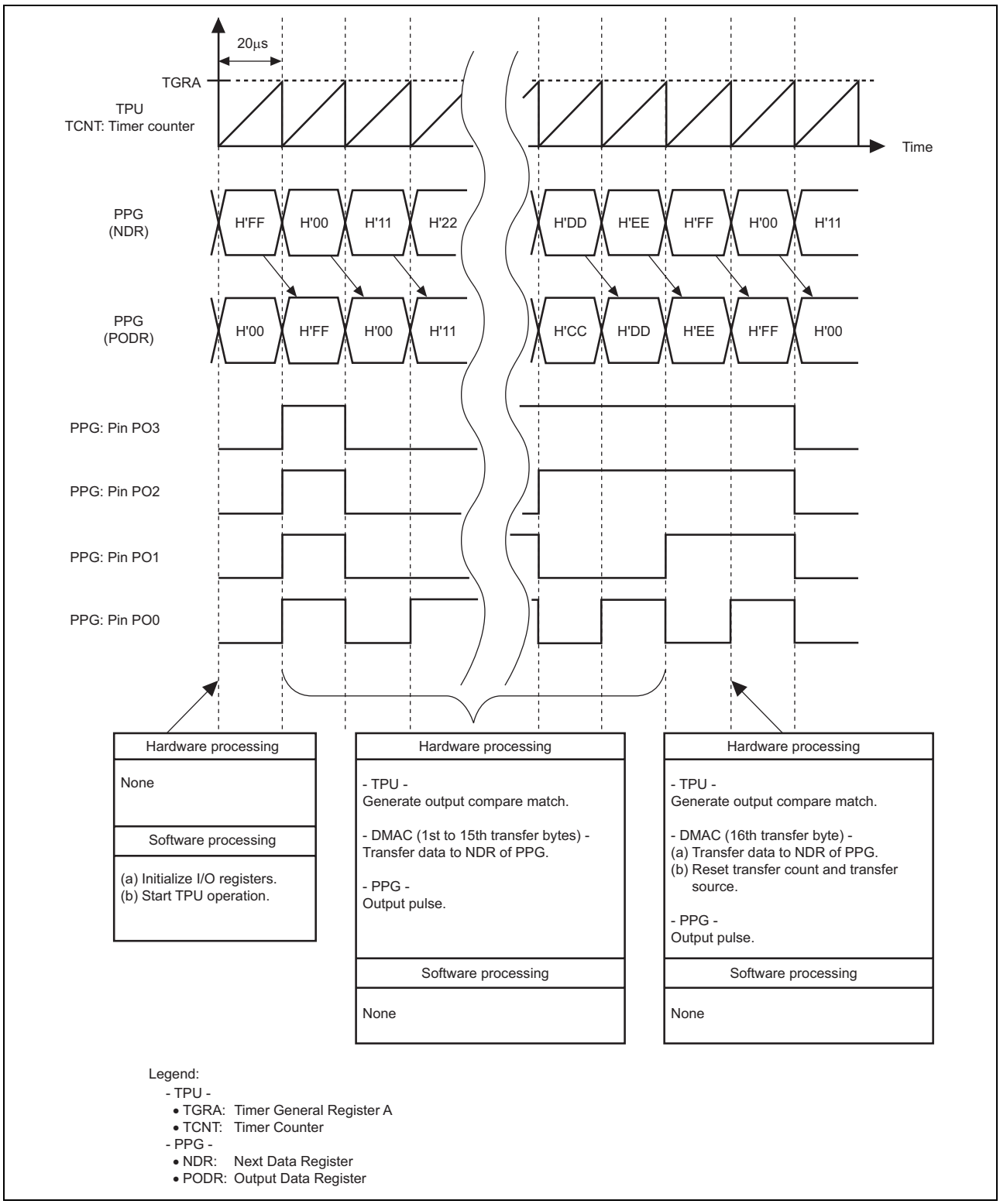


**Figure 3 Operation**

# 5. Software Description

## 5.1 Symbolic Constants

**Table 3 List of Symbolic Constants**

| Constant Name | Setting Value | Description | Used by Functions |
|---|---|---|---|
| MAX_PPG_DATA_CNT | 16 | Max. PPG output data count | — |

## 5.2 ROM Variables

**Table 4 List of ROM Variables**

| Type | Variable Name | Setting Value | Description | Used by Functions |
|---|---|---|---|---|
| const unsigned char | c_ppg_data [MAX_PPG_DATA_CNT] | 0x00, 0x11, 0x22, 0x33, 0x44, 0x55, 0x66, 0x77, 0x88, 0x99, 0xAA, 0xBB, 0xCC, 0xDD, 0xEE, 0xFF | PPG output data | init |

## 5.3 List of Functions

**Table 5 List of Functions**

| Function Name | Description |
|---|---|
| PowerON_Reset | • Initial settings function<br>Initializes status pointer (SP), sets interrupt mask bits, sets uninitialized/initialized data, calls main function. |
| main | • Main function<br>Calls init function and starts TPU operation. |
| init | • I/O register initialization function<br>Initializes registers. |

## 5.4 Functions

### 5.4.1 PowerON_Reset Function

(1) Functional Overview

The PowerON_Reset function initializes the status pointer (SP) and uses embedded functions and standard library functions to set interrupt mask bits and set uninitialized/initialized data. Then it calls the main function.

(2) Arguments

None

(3) Returned values

None

(4) Flowchart

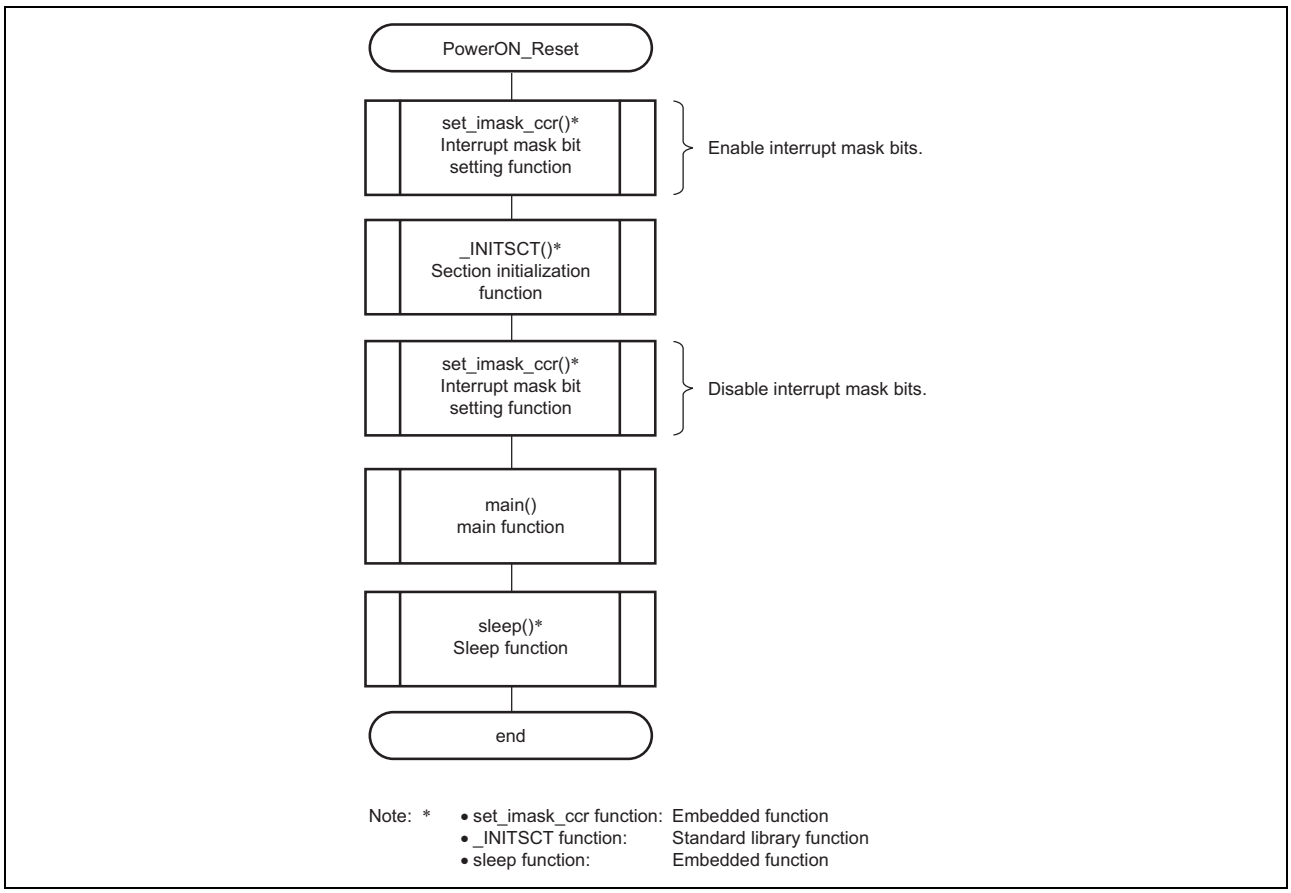


**Figure 4 Flowchart (PowerON_Reset)**

### 5.4.2 main Function

(1) Functional Overview

The main function calls the init function to initialize registers and starts the TPU.

(2) Arguments

None

(3) Returned values

None

(4) Description of internal registers used

The internal I/O registers used by this function are shown below. Note that the setting values shown are those used in this sample task and differ from the initial values.

- Timer Start Register (TSTR) - Number of bits: 8, Address: H'FFFFBC

| Bit | Bit Name | Set Value | R/W | Descriptions |
|---|---|---|---|---|
| 0 | CST0 | 1 | R/W | Counter Start 0<br>This bit selects operation or stoppage for TCNT.<br>1: TCNT0 performs count operation |

(5) Flowchart

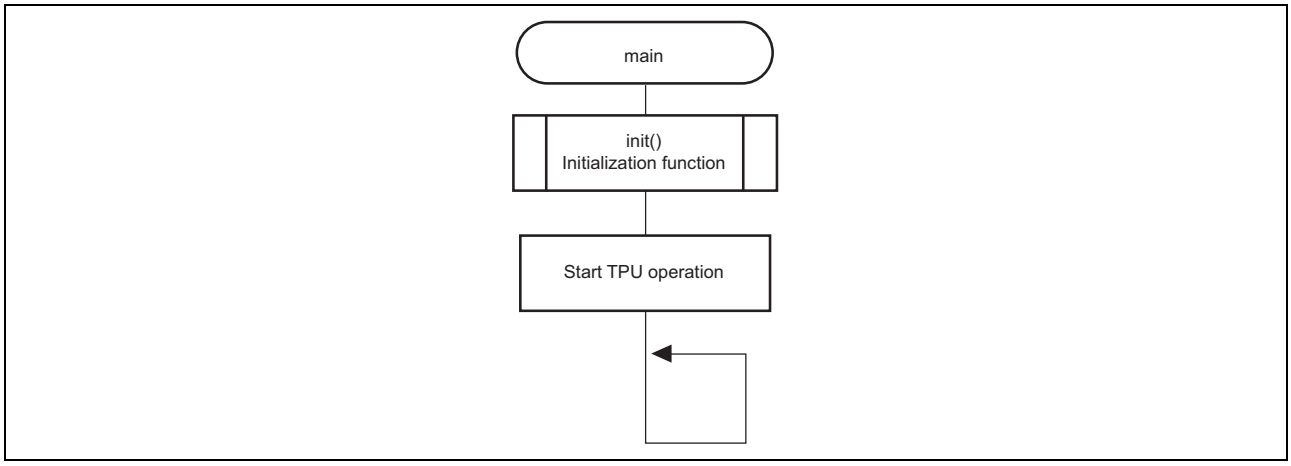


**Figure 5 Flowchart (main)**

### 5.4.3 init Function

(1) Functional Overview

The init function initializes various registers.

(2) Arguments

None

(3) Returned values

None

(4) Description of internal registers used

The internal I/O registers used by this function are shown below. Note that the setting values shown are those used in this sample task and differ from the initial values.

- System Clock Control Register (SCKCR) - Number of bits: 16, Address: H'FFFDC4

| Bit | Bit Name | Set Value | R/W | Descriptions |
|---|---|---|---|---|
| 10 | ICK2 | 0 | R/W | System Clock (Iϕ) Select |
| 9 | ICK1 | 0 | R/W | These bits select the frequency of the system clock provided to the |
| 8 | ICK0 | 0 | R/W | CPU, DMAC, and DTC.<br>000: Input clock × 4 |
| 6 | PCK2 | 0 | R/W | Peripheral Module Clock (Pϕ) Select |
| 5 | PCK1 | 0 | R/W | These bits select the frequency of the peripheral module clock. |
| 4 | PCK0 | 1 | R/W | 001: Input clock × 2 |
| 2 | BCK2 | 0 | R/W | External Bus Clock (Bϕ) Select |
| 1 | BCK1 | 0 | R/W | These bits select the frequency of the external bus clock. |
| 0 | BCK0 | 0 | R/W | 000: Input clock × 4 |

- MSTPCRA controls the module stop mode. Setting a bit to 1 makes the corresponding module enter the module stop state, and clearing the bit to 0 clears the module stop state.

- Module Stop Control Register A (MSTPCRA) - Number of bits: 16, Address: H'FFFDC8

| Bit | Bit Name | Set Value | R/W | Descriptions |
|---|---|---|---|---|
| 15 | ACSE | 0 | R/W | All-Module-Clock-Stop Mode Enable<br>Enables/disables all-module-clock-stop state for reducing current consumption by stopping the bus controller and I/O ports operations when the CPU executes the SLEEP instruction after module stop state has been set for all the on-chip peripheral modules controlled by MSTPCR.<br>0: All-module-clock-stop mode disabled |
| 0 | MSTPA0 | 0 | R/W | 16-bit timer pulse unit (TPU channels 5 to 0) |

- MSTPCRB controls the module stop mode. Setting a bit to 1 makes the corresponding module enter the module stop state, and clearing the bit to 0 clears the module stop state.

- Module Stop Control Register B (MSTPCRB) - Number of bits: 16, Address: H'FFFDCA

| Bit | Bit Name | Set Value | R/W | Descriptions |
|---|---|---|---|---|
| 15 | MSTPB15 | 0 | R/W | Programmable pulse generator (PPG_0: PO15 to PO0) |

- Timer Start Register (TSTR) - Number of bits: 8, Address: H'FFFFBC

| Bit | Bit Name | Set Value | R/W | Descriptions |
|---|---|---|---|---|
| 0 | CST0 | 0 | R/W | Counter Start 0<br>This bit selects operation or stoppage for TCNT.<br>0: TCNT0 count operation is stopped. |

- Timer Status Register (TSR) - Number of bits: 8, Address: H'FFFFC5

| Bit | Bit Name | Set Value | R/W | Descriptions |
|---|---|---|---|---|
| 0 | TGFA | 0 | R/(W) | Input Capture/Output Compare Match Flag A<br>Status flag that indicates the occurrence of TGRA input capture or compare match.<br>[Clearing condition]<br>When 0 is written to TGFA after reading TGFA as 1 |

- Timer Control Register (TCR) - Number of bits: 8, Address: H'FFFFC0

| Bit | Bit Name | Set Value | R/W | Descriptions |
|---|---|---|---|---|
| 7 | CCLR2 | 0 | R/W | Counter Clear 2 to 0 |
| 6 | CCLR1 | 0 | R/W | These bits select the TCNT counter clearing source. |
| 5 | CCLR0 | 1 | R/W | 001: TCNT is cleared at TGRA compare match /input capture. |
| 4 | CKEG1 | 0 | R/W | Clock Edge 1 and 0 |
| 3 | CKEG0 | 0 | R/W | These bits select the input clock edge.<br>00: Internal clock counts at falling edge. |
| 2 | TPSC2 | 0 | R/W | Timer Prescaler 2 to 0 |
| 1 | TPSC1 | 0 | R/W | These bits select the TCNT counter clock. |
| 0 | TPSC0 | 0 | R/W | 000: Internal clock counts on Pϕ/1. |

- Timer Mode Register (TMDR) - Number of bits: 8, Address: H'FFFFC1

| Bit | Bit Name | Set Value | R/W | Descriptions |
|---|---|---|---|---|
| 4 | BFA | 0 | R/W | Buffer Operation A<br>Specifies whether TGRA is to normally operate, or TGRA and TGRC are to be used together for buffer operation.<br>0: TGRA operates normally |
| 3 | MD3 | 0 | R/W | Modes 3 to 0 |
| 2 | MD2 | 0 | R/W | Set the timer operating mode. |
| 1 | MD1 | 0 | R/W | 0000: Operates normally |
| 0 | MD0 | 0 | R/W | |

- Timer I/O Control Register H (TIORH) - Number of bits: 8, Address: H'FFFFC2
- Timer I/O Control Register L (TIORL) - Number of bits: 8, Address: H'FFFFC3

| Bit | Bit Name | Set Value | R/W | Descriptions |
|---|---|---|---|---|
| 3 | IOA3 | 0 | R/W | I/O Control A3 to A0 |
| 2 | IOA2 | 0 | R/W | These bits specify the function of TGRA. |
| 1 | IOA1 | 0 | R/W | 0000: TIOCA pin output disabled |
| 0 | IOA0 | 0 | R/W | |

- Timer Interrupt Enable Register (TIER) - Number of bits: 8, Address: H'FFFFC4

| Bit | Bit Name | Set Value | R/W | Descriptions |
|---|---|---|---|---|
| 0 | TGIEA | 1 | R/W | TGR Interrupt Enable A<br>Enables/disables interrupt requests (TGIA) by the TGFA bit when the TGFA bit in TSR is set to 1.<br>1: Interrupt requests (TGIA) by TGFA bit enabled |

- Timer Counter (TCNT) - Number of bits: 16, Address: H'FFFFC6
  Function: TCNT is a 16-bit readable/writable counter.
  Setting value: H'0000

- Timer General Register A (TGRA) - Number of bits: 8, Address: H'FFFFC8
  Function: TGRA is a 16-bit readable/writable register that functions as both an output compare and an input capture register.
  Setting value: H'01F3 (period: 20 μs)

- Timer Synchronization Register (TSYR) - Number of bits: 8, Address: H'FFFFBD

| Bit | Bit Name | Set Value | R/W | Descriptions |
|---|---|---|---|---|
| 0 | SYNC0 | 0 | R/W | Timer Synchronization 0<br>This bit selects whether operation is independent of or synchronized with other channels.<br>0: TCNT0 operates independently. |

- Output Data Register L (PODRL) - Number of bits: 8, Address: H'FFFF7B
  Function: PODRL stores pulse output values.
  Setting value: H'00

- Next Data Enable Register H (NDERH) - Number of bits: 8, Address: H'FFFF79
  Function: NDERH selects the PPG pulse output pin on a bit-by-bit basis. When a bit is set to 1, the value in the corresponding NDRH bit is transferred to PODRH by the selected output trigger. Values are not transferred from NDRH to PODRH for bits cleared to 0.
  Setting value: H'00

- Next Data Enable Register L (NDERL) - Number of bits: 8, Address: H'FFFF78
  Function: NDERL selects the PPG pulse output pin on a bit-by-bit basis. When a bit is set to 1, the value in the corresponding NDRL bit is transferred to PODRL by the selected output trigger. Values are not transferred from NDRL to PODRL for bits cleared to 0.
  Setting value: H'0F

- PPG Output Control Register (PCR) - Number of bits: 8, Address: H'FFFF76

| Bit | Bit Name | Set Value | R/W | Descriptions |
|---|---|---|---|---|
| 1 | G0CMS1 | 0 | R/W | Group 0 Compare Match Select 1 and 0 |
| 0 | G0CMS0 | 0 | R/W | These bits select the output trigger of pulse output group 0.<br>00: Compare match in TPU channel 0 |

- PPG Output Mode Register (PMR) - Number of bits: 8, Address: H'FFFF77

| Bit | Bit Name | Set Value | R/W | Descriptions |
|---|---|---|---|---|
| 4 | G0INV | 1 | R/W | Group 0 Inversion<br>This bit selects direct output or inverted output for pulse output group 0.<br>1: Direct output |
| 0 | G0NOV | 1 | R/W | Group 0 Non-Overlap<br>Selects normal or non-overlapping operation for pulse output group 0.<br>0: Normal operation<br>(output values updated by compare match A on the selected TPU channel) |

- Next Data Register L (NDRL) - Number of bits: 8, Address: H'FFFF7D
  Function: NDRL stores the next data for pulse output. The NDR addresses differ depending on whether the pulse output groups have the same output trigger or different output triggers.
  Setting value: H'0F
- DMA Source Address Register (DSAR) - Number of bits: 32, Address: H'FFFC00
  Function: DSAR is a 32-bit readable/writable register that specifies the transfer source address.
  Setting value: c_ppg_data[0] address
- DMA Destination Address Register (DDAR) - Number of bits: 32, Address: H'FFFC04
  Function: DDAR is a 32-bit readable/writable register that specifies the transfer destination address.
  Setting value: H'00FFFF7D (NDRL register address)
- DMA Block Size Register (DBSR) - Number of bits: 32, Address: H'FFFC10
  Function: DBSR specifies the repeat size or block size.
  Setting value: H'00100010
- DMA Module Request Select Register (DMRSR) - Number of bits: 8, Address: H'FFFD20
  Function: DMRSR is an 8-bit readable/writable register that specifies on-chip module interrupt sources.
  Setting value: H'58 (TGI0A)
- DMA Address Control Register (DACR) - Number of bits: 32, Address: H'FFFC18

| Bit | Bit Name | Set Value | R/W | Descriptions |
|---|---|---|---|---|
| 31 | AMS | 0 | R/W | Address Mode Select<br>This bit selects between single and dual address mode.<br>0: Dual address mode |
| 21 | SAT1 | 1 | R/W | Source Address Update Mode 1 and 0 |
| 20 | SAT0 | 0 | R/W | These bits select whether the source address (DSAR) is increased, decreased, or fixed.<br>10: Increase source address. |
| 17 | DAT1 | 0 | R/W | Destination Address Update Mode 1 and 0 |
| 16 | DAT0 | 0 | R/W | These bits select whether the destination address (DDAR) is increased, decreased, or fixed.<br>00: Destination address is fixed. |

- DMA Mode Control Register (DMDR) - Number of bits: 32, Address: H'FFFC14

| Bit | Bit Name | Set Value | R/W | Descriptions |
|---|---|---|---|---|
| 31 | DTE | 1 | R/W | Data Transfer Enable<br>This bit enables or disables data transfer for the corresponding channel.<br>1: Data transfer enabled (during DMA operation) |
| 15 | DTSZ1 | 0 | R/W | Data Access Size 1 and 0 |
| 14 | DTSZ0 | 0 | R/W | These bits select the data access size for a transfer.<br>00: Byte size (8 bits) |
| 13 | MDS1 | 1 | R/W | Transfer Mode Select 1 and 0 |
| 12 | MDS0 | 0 | R/W | These bits select the transfer mode.<br>10: Repeat transfer mode |
| 8 | DTIE | 0 | R/W | Data Transfer End Interrupt Enable<br>This bit enables or disables a transfer end interrupt requests by the transfer counter.<br>0: Transfer end interrupt requests disabled |
| 7 | DTF1 | 1 | R/W | Data Transfer Factor 1 and 0 |
| 6 | DTF0 | 0 | R/W | These bits select the DMAC activation source.<br>10: On-chip module interrupt |
| 5 | DTA | 1 | R/W | Data Transfer Acknowledge<br>This bit is valid when DMA transfer is activated by an on-chip module interrupt.<br>1: Clearing the interrupt source when DMA transfer is activated by an on-chip module interrupt is enabled. The on-chip module interrupt source is cleared by the DMA transfer, so no interrupt request to the CPU or DTC is necessary. |
| 2 | DMAP2 | 1 | R/W | DMA Priority Level 2 to 0 |
| 1 | DMAP1 | 1 | R/W | These bits select the DMAC and DTC priority level relative to the CPU.<br>111: Priority level 7 (highest) |
| 0 | DMAP0 | 1 | R/W | |

(5) Flowchart

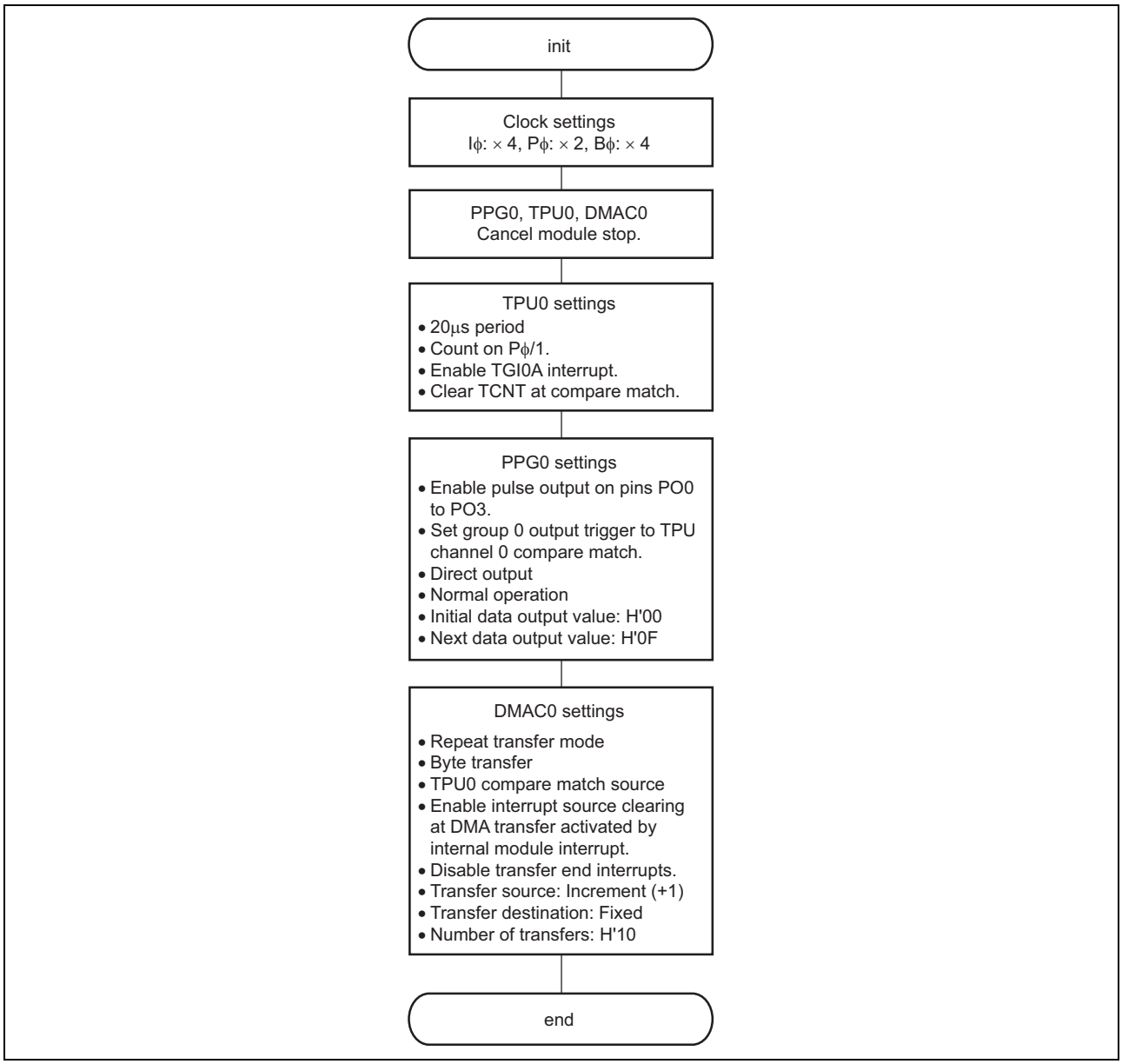


**Figure 6 Flowchart (init)**

## 6. Notes

(1) PO0 to PO15 of the PPG also function as pins for other peripheral functions such as the TPU. It is not possible to generate pulse output on these pins if output on them is enabled for another peripheral function. However, transfers from NDR to PODR can always proceed regardless of the pin states. Make changes to the pin functions when in a state where no output trigger will be generated. For details, see the relevant hardware manual.
(2) The address of the next data register (NDR) differs depending on whether the pulse output groups have the same output trigger or different output triggers. For details, see the relevant hardware manual.

## 7. Reference Documents

- Hardware Manual
  H8SX/1648, H8SX/1648A, H8SX/1648L, H8SX/1648G, H8SX/1648H Group Hardware Manual
  (The latest version can be downloaded from the Renesas Technology Web site.)
- Development Environment Manual
  H8S/300, H8/300 Series C/C++ Compiler Package User's Manual
  (The latest version can be downloaded from the Renesas Technology Web site.)
- Technical News/Technical Updates
  (The latest information can be downloaded from the Renesas Technology Web site.)

## Website and Support

Renesas Technology Website
http://www.renesas.com/

Inquiries
http://www.renesas.com/inquiry
csc@renesas.com

## Revision Record

| | | Description | |
|---|---|---|---|
| **Rev.** | **Date** | **Page** | **Summary** |
| 1.00 | Jan.22.09 | — | First edition issued |

## Notes regarding these materials

1. This document is provided for reference purposes only so that Renesas customers may select the appropriate Renesas products for their use. Renesas neither makes warranties or representations with respect to the accuracy or completeness of the information contained in this document nor grants any license to any intellectual property rights or any other rights of Renesas or any third party with respect to the information in this document.
2. Renesas shall have no liability for damages or infringement of any intellectual property or other rights arising out of the use of any information in this document, including, but not limited to, product data, diagrams, charts, programs, algorithms, and application circuit examples.
3. You should not use the products or the technology described in this document for the purpose of military applications such as the development of weapons of mass destruction or for the purpose of any other military use. When exporting the products or technology described herein, you should follow the applicable export control laws and regulations, and procedures required by such laws and regulations.
4. All information included in this document such as product data, diagrams, charts, programs, algorithms, and application circuit examples, is current as of the date this document is issued. Such information, however, is subject to change without any prior notice. Before purchasing or using any Renesas products listed in this document, please confirm the latest product information with a Renesas sales office. Also, please pay regular and careful attention to additional and different information to be disclosed by Renesas such as that disclosed through our website. (http://www.renesas.com )
5. Renesas has used reasonable care in compiling the information included in this document, but Renesas assumes no liability whatsoever for any damages incurred as a result of errors or omissions in the information included in this document.
6. When using or otherwise relying on the information in this document, you should evaluate the information in light of the total system before deciding about the applicability of such information to the intended application. Renesas makes no representations, warranties or guaranties regarding the suitability of its products for any particular application and specifically disclaims any liability arising out of the application and use of the information in this document or Renesas products.
7. With the exception of products specified by Renesas as suitable for automobile applications, Renesas products are not designed, manufactured or tested for applications or otherwise in systems the failure or malfunction of which may cause a direct threat to human life or create a risk of human injury or which require especially high quality and reliability such as safety systems, or equipment or systems for transportation and traffic, healthcare, combustion control, aerospace and aeronautics, nuclear power, or undersea communication transmission. If you are considering the use of our products for such purposes, please contact a Renesas sales office beforehand. Renesas shall have no liability for damages arising out of the uses set forth above.
8. Notwithstanding the preceding paragraph, you should not use Renesas products for the purposes listed below:
   (1) artificial life support devices or systems
   (2) surgical implantations
   (3) healthcare intervention (e.g., excision, administration of medication, etc.)
   (4) any other purposes that pose a direct threat to human life
   Renesas shall have no liability for damages arising out of the uses set forth in the above and purchasers who elect to use Renesas products in any of the foregoing applications shall indemnify and hold harmless Renesas Technology Corp., its affiliated companies and their officers, directors, and employees against any and all damages arising out of such applications.
9. You should use the products described herein within the range specified by Renesas, especially with respect to the maximum rating, operating supply voltage range, movement power voltage range, heat radiation characteristics, installation and other product characteristics. Renesas shall have no liability for malfunctions or damages arising out of the use of Renesas products beyond such specified ranges.
10. Although Renesas endeavors to improve the quality and reliability of its products, IC products have specific characteristics such as the occurrence of failure at a certain rate and malfunctions under certain use conditions. Please be sure to implement safety measures to guard against the possibility of physical injury, and injury or damage caused by fire in the event of the failure of a Renesas product, such as safety design for hardware and software including but not limited to redundancy, fire control and malfunction prevention, appropriate treatment for aging degradation or any other applicable measures. Among others, since the evaluation of microcomputer software alone is very difficult, please evaluate the safety of the final products or system manufactured by you.
11. In case Renesas products listed in this document are detached from the products to which the Renesas products are attached or affixed, the risk of accident such as swallowing by infants and small children is very high. You should implement safety measures so that Renesas products may not be easily detached from your products. Renesas shall have no liability for damages arising out of such detachment.
12. This document may not be reproduced or duplicated, in any form, in whole or in part, without prior written approval from Renesas.
13. Please contact a Renesas sales office if you have any questions regarding the information contained in this document, Renesas semiconductor products, or if you have any other inquiries.