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H8S/2400 Series

Watchdog Timer Mode Operation of the Watchdog Timer (WDT) Module

Introduction

This Application Note presents a system operation example that uses the watchdog timer (WDT) module in watchdog timer mode.

A system reset can be generated automatically on a system runaway or other abnormal operation by using the WDT module in watchdog timer mode.

Target Devices

- H8S/2472, H8S/2463, H8S/2462 Group

Preface

This program can be used with other H8S Family MCUs that have the same internal I/O registers as the devices on which operation has been confirmed. Check the latest version of the manual for any additions and modifications to functions.

Careful evaluation is recommended before using this application note.

Contents

1. Specifications

This application note presents a program that periodically clears the TCNT_0 value to 0 so that the WDT module timer counter 0 (TCNT_0) does not overflow.

Furthermore, to simulate the occurrence of a system abnormality, this application can disable the periodic TCNT_0 clear to 0 operation by the input of a falling edge signal to the NMI pin. When TCNT_0 overflows due to the TCNT_0 clear to 0 operation being disabled, an internal reset signal is generated.

Figure 1 presents an overview of the operation presented in this application note. The detailed specifications are as follows.

- The WDT module is used in WDT_0 watchdog timer mode.
- The TCNT_0 input clock is set to be $\phi/2$.
- The port A0 (PA0) output will be inverted as long as the system is operating normally.
- To verify the reset factor, the content of the system control register (SYSCR) external reset bit (XRST) is output from port 40 (P40).

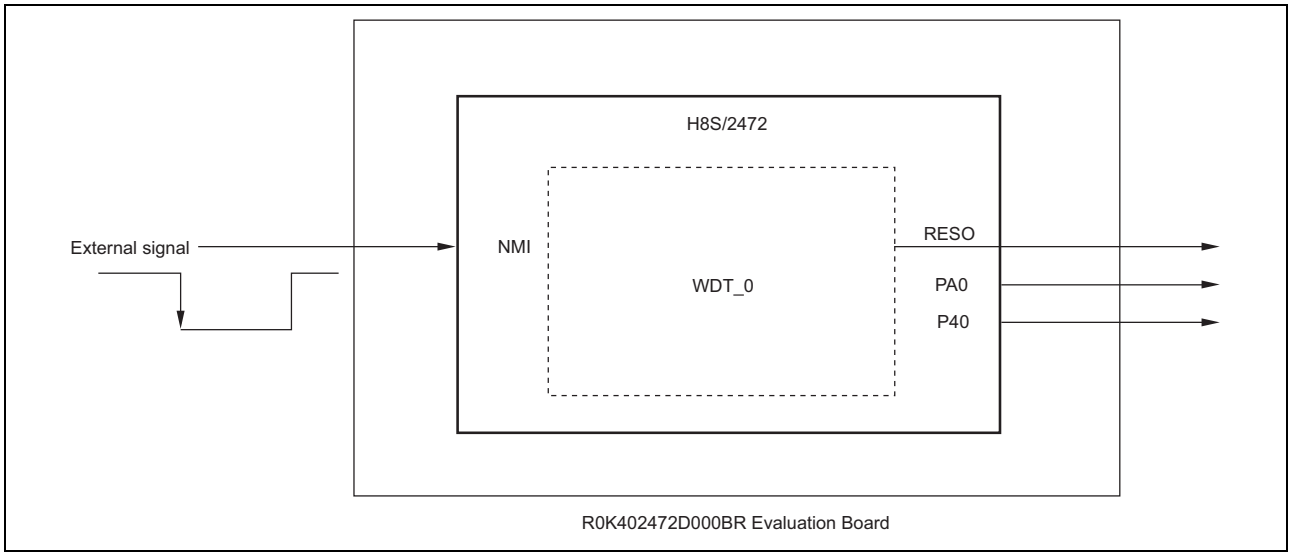


Figure 1 Operational Overview

2. Applicable Conditions

Table 1 Applicable Conditions

Item	Description
Operating frequency	Input clock: 8 MHz System clock (ϕ): 32 MHz (8 MHz multiplied by 4)
Operating voltage	3.3V
Operating mode	Mode 2 ($\overline{MD2}$ = 1, MD1 = 1)
Integrated development environment	High-performance Embedded Workshop(HEW) Version 4.04.01.001
Evaluation board	Renesas Technology Corp. R0K402472D000BR
C/C++ compiler	Renesas Technology Corp. H8S,H8/300 C/C++ Compiler (V.6.02.01.000)
Compiler options	-cpu=2600A:24 -optimize=0
Optimizing linkage editor	Renesas Technology Corp. Optimizing Linkage Editor (V.9.04.01.000)
Link options	-start = PResetPRG,PIntPRG/0400, P,C$DSEC,C$BSEC,D/0800, B,R/0FF0800, S/0FF9600

3. Functions Used

Figure 2 shows the operation in watchdog timer mode (RST/$\overline{\text{NMI}}$ = 1). Watchdog timer mode is described below.

To use the WDT as a watchdog timer, set the WT/$\overline{\text{IT}}$ bit and the TME bit in Timer Control/Status Register (TCSR) to 1. While the WDT is used as a watchdog timer, if TCNT overflows without being rewritten because of a system malfunction or another error, an internal reset or NMI interrupt request is generated. TCNT does not overflow while the system is operating normally. Software must prevent TCNT overflows by rewriting the TCNT value (normally be writing H'00) before overflows occurs.

If the RST/$\overline{\text{NMI}}$ bit of TCSR is set to 1, when the TCNT overflows, an internal reset signal for this LSI is issued for 518 system clocks, and the low level signal is simultaneously output from the $\overline{\text{RESO}}$ pin for 132 states, as shown in figure 2. If the RST/$\overline{\text{NMI}}$ bit is cleared to 0, when the TCNT overflows, an NMI interrupt request is generated. Here, the output from the $\overline{\text{RESO}}$ pin remains high.

An internal reset request from the watchdog timer and a reset input from the $\overline{\text{RES}}$ pin are processed in the same vector. Reset source can be identified by the XRST bit status in SYSCR.
If a reset caused by a signal input to the $\overline{\text{RES}}$ pin occurs at the same time as a reset caused by a WDT overflow, the $\overline{\text{RES}}$ pin reset has priority and the XRST bit in SYSCR is set to 1.

An NMI interrupt request from the watchdog timer and an interrupt request from the NMI pin are processed in the same vector. Do not handle an NMI interrupt request from the watchdog timer and an interrupt request from the NMI pin at the same time.

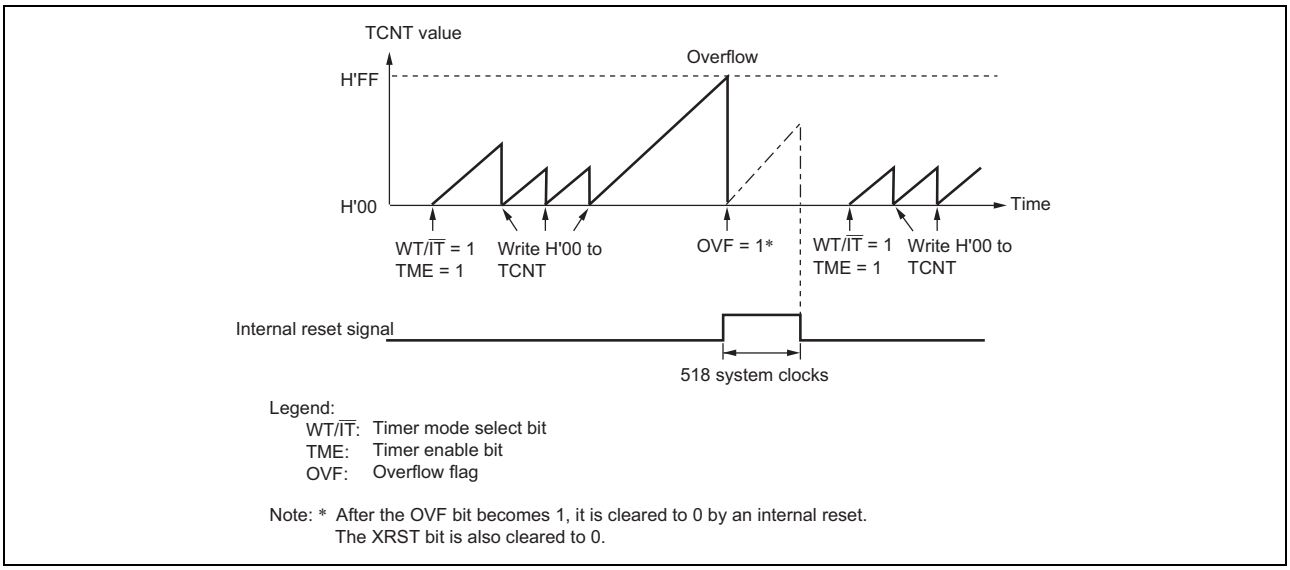


Figure 2 Watchdog Timer Mode (RST/$\overline{\text{NMI}}$ = 1) Operation

4. Operation

Figure 3 shows the watchdog timer operation used in this application note.

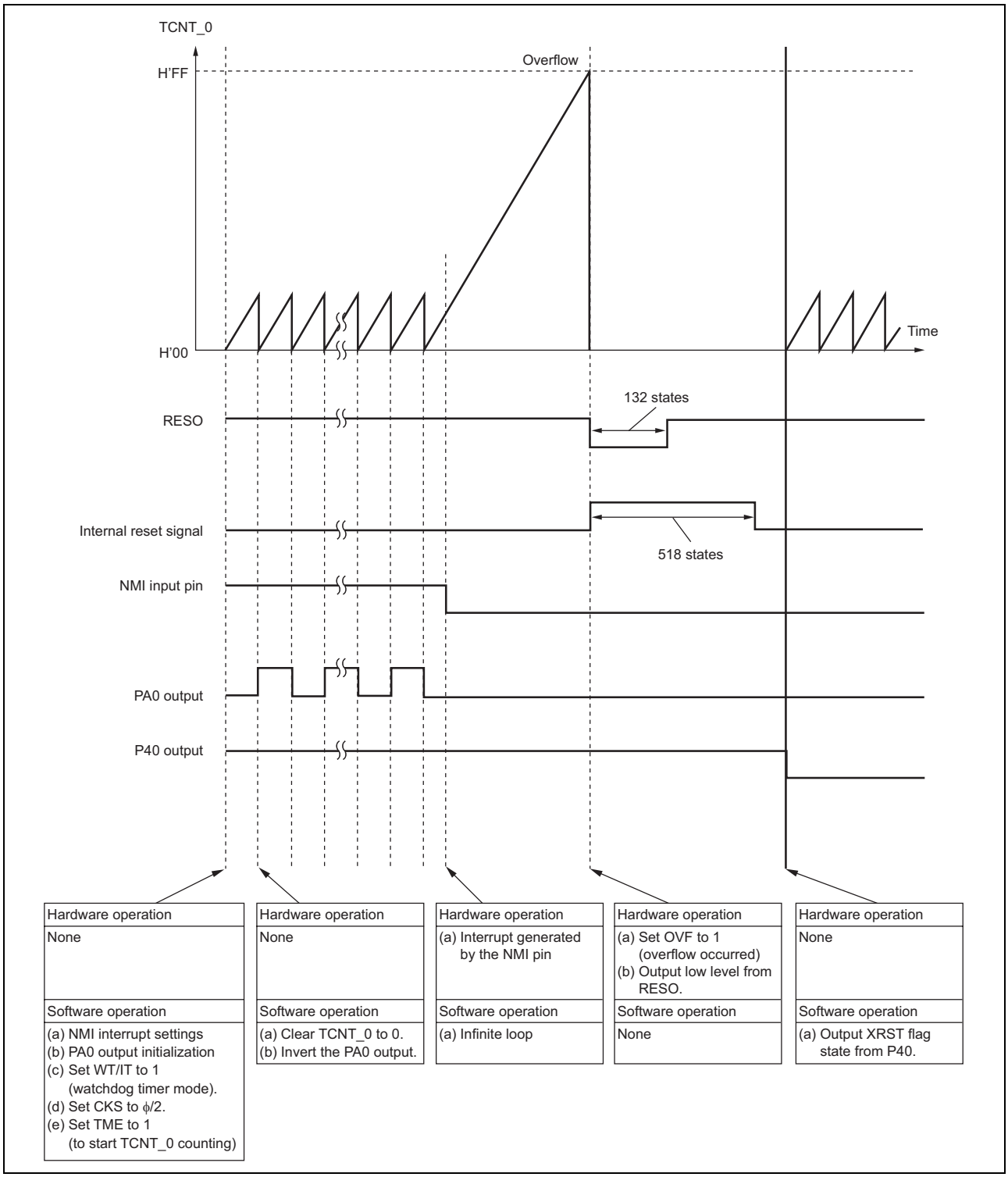


Figure 3 Watchdog Timer Operation

5. Software

5.1 Functions

Table 2 Functions

Function Name	Description
PowerOn_Reset	• Initialization function Initializes the stack pointer (SP), sets interrupt mask bits, sets up uninitialized and initialized data, and calls the main function.
main	• Main function Calls the init_CPU and init_WDT functions.
init_CPU	• I/O register initialization function Enables the WDT interrupt and initializes the pulse output port.
init_WDT	• WDT initialization function Sets up reset factor discrimination, sets the WDT operating mode, and starts operation.
INT_NMI	• Nonmaskable interrupt handler This function executes an infinite loop.

5.2 Function Descriptions

5.2.1 PowerON_Reset Function

(1) Function overview

The PowerON_Reset function initializes the stack pointer (SP), prepares the embedded functions and standard library functions, sets the interrupt mask bits, and sets up the uninitialized and initialized data. Then it calls the main function.

(2) Arguments

None

(3) Returned value

None

(4) Description of internal I/O registers used

None

(5) Flowchart

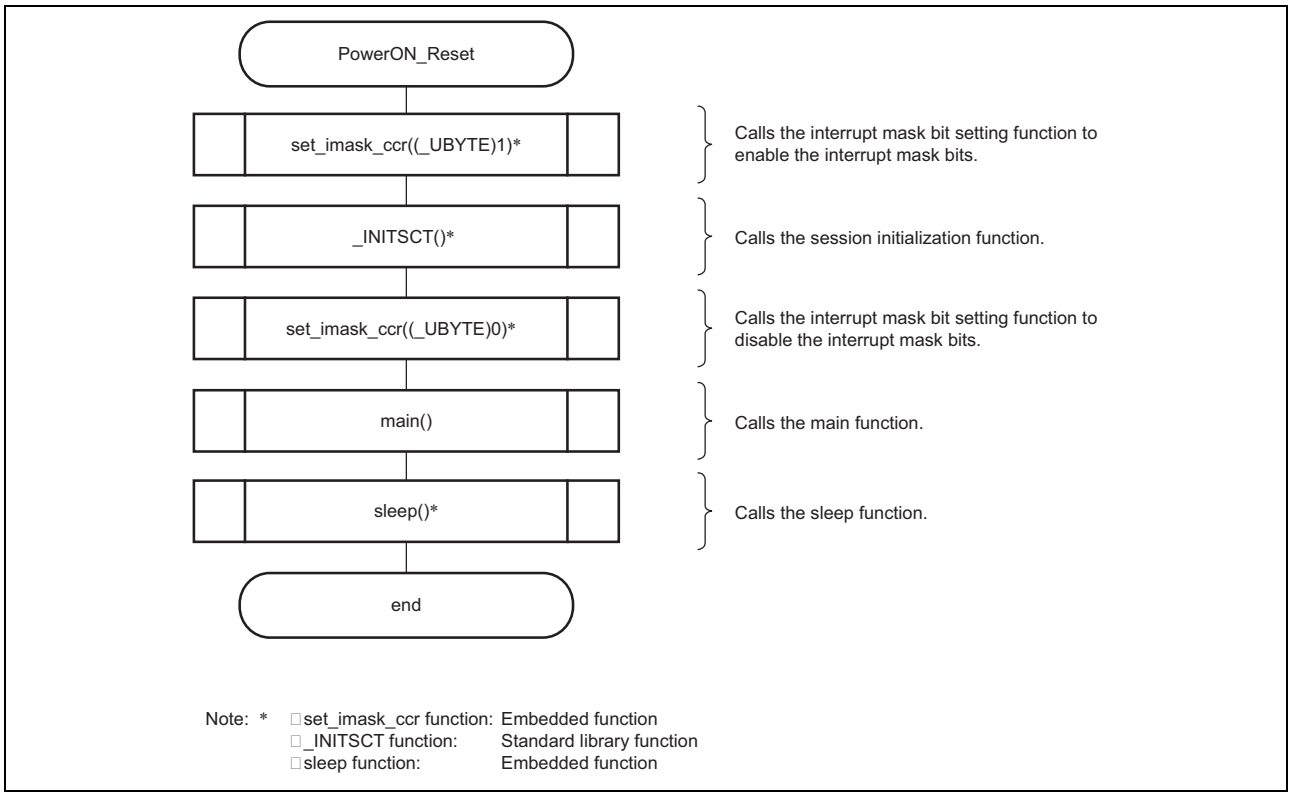


Figure 4 Flowchart (PowerON_Reset)

5.2.2 main Function

(1) Function overview

The main function calls the init_CPU and init_WDT functions.

(2) Arguments

None

(3) Returned value

None

(4) Description of internal I/O registers used

This function uses the internal registers shown below.

Note that the set values shown here are for use in this application note and differ from the initial values.

- Timer Counter_0 (write) (TCNT_0) - Number of bits: 16 bits, Address: H'FFFFA8

Bit	Bit Name	Set Value	R/W	Descriptions
15 to 0	—	H'5A00	R/W	TCNT_0 is an 8-bit read/write increment-only counter. TCNT and TCSR are allocated to the same address. Therefore, when writing to TCNT, applications must transfer data in which the upper byte is H'5A and the lower byte is the desired write data value.

- Port A Output Data Register (PAODR) - Number of bits: 8 bits, Address: H'FFFFAA

Bit	Bit Name	Set Value	R/W	Descriptions
0	PA0ODR	0/1	R/W	Holds the output data for pins used as general-purpose output ports.

(5) Flowchart

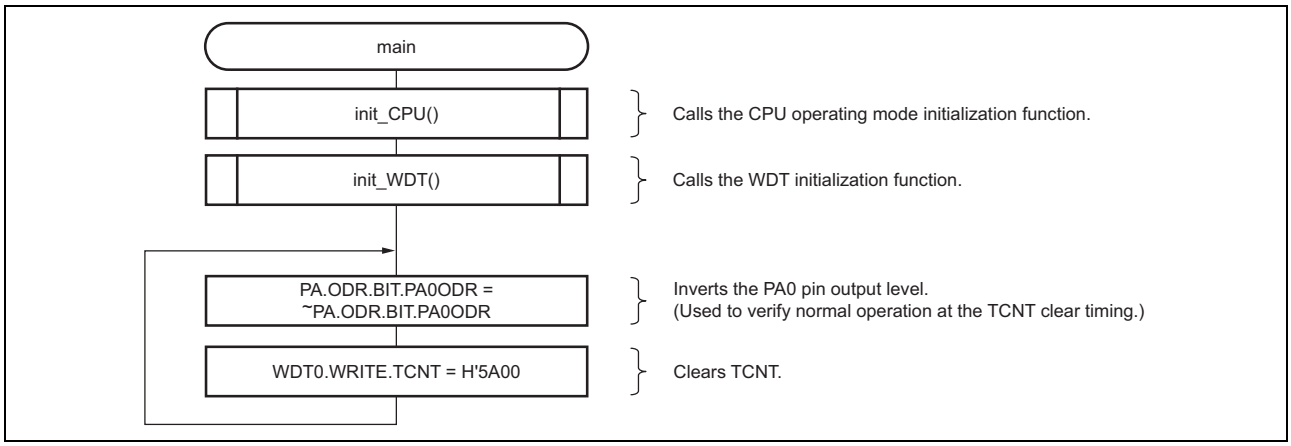


Figure 5 Flowchart (main)

5.2.3 init_CPU Function

(1) Function overview

The init_CPU function initializes the system cock settings and the CPU operating mode.

(2) Arguments

None

(3) Returned value

None

(4) Description of internal I/O registers used

This function uses the internal registers shown below.

Note that the set values shown here are for use in this application note and differ from the initial values.

- Standby Control Register (SBYCR) - Number of bits: 8 bits, Address: H'FFFF84

Bit	Bit Name	Set Value	R/W	Descriptions
2	SCK2	0	R/W	System Clock Select 2 to 0
1	SCK1	0	R/W	Select a clock for the bus master in high-speed mode or medium-speed mode.
0	SCK0	0	R/W	000: High-speed mode (Initial value) 001: Medium-speed clock: ϕ/2 010: Medium-speed clock: ϕ/4 011: Medium-speed clock: ϕ/8 100: Medium-speed clock: ϕ/16 101: Medium-speed clock: ϕ/32 11x: Must not be set.

Legend:
x: Don't care

- Mode Control Register (MDCR) - Number of bits: 8 bits, Address: H'FFFFC5

Bit	Bit Name	Set Value	R/W	Descriptions
7	EXPE	0	R/W	Extended Mode Enable Specifies extended mode. 0: Single-chip mode 1: Extended mode

- System Control Register (SYSCR) - Number of bits: 8 bits, Address: H'FFFFC4

Bit	Bit Name	Set Value	R/W	Descriptions
3	XRST	1	R	External Reset This bit indicates the reset source. A reset is caused by an external reset input, or when the watchdog timer overflows. 0: A reset is caused when the watchdog timer overflows. 1: A reset is caused by an external reset.
2	NMIEG	0	R/W	NMI Edge Select Selects the valid edge of the NMI interrupt input. 0: An interrupt is requested at the falling edge of NMI input 1: An interrupt is requested at the rising edge of NMI input
0	RAME	1	R/W	RAM Enable Enables or disables on-chip RAM. The RAME bit is initialized when the reset state is released. 0: On-chip RAM is disabled 1: On-chip RAM is enabled

- Port A Data Direction Register (PADDR) - Number of bits: 8 bits, Address: H'FFFFAB

Bit	Bit Name	Set Value	R/W	Descriptions
0	PA0DDR	1	W	When set to 1, the corresponding pins function as output port pins; when cleared to 0, function as input port pins. As the address of this register is the same as that of Port A Input Data Register (PAPIN), reading from this register indicates the state of port A.

- Port A Output Data Register (PAODR) - Number of bits: 8 bits, Address: H'FFFFAA

Bit	Bit Name	Set Value	R/W	Descriptions
0	PA0ODR	0	R/W	PAODR stores output data for the port A pins that are used as the general output port.

(5) Flowchart

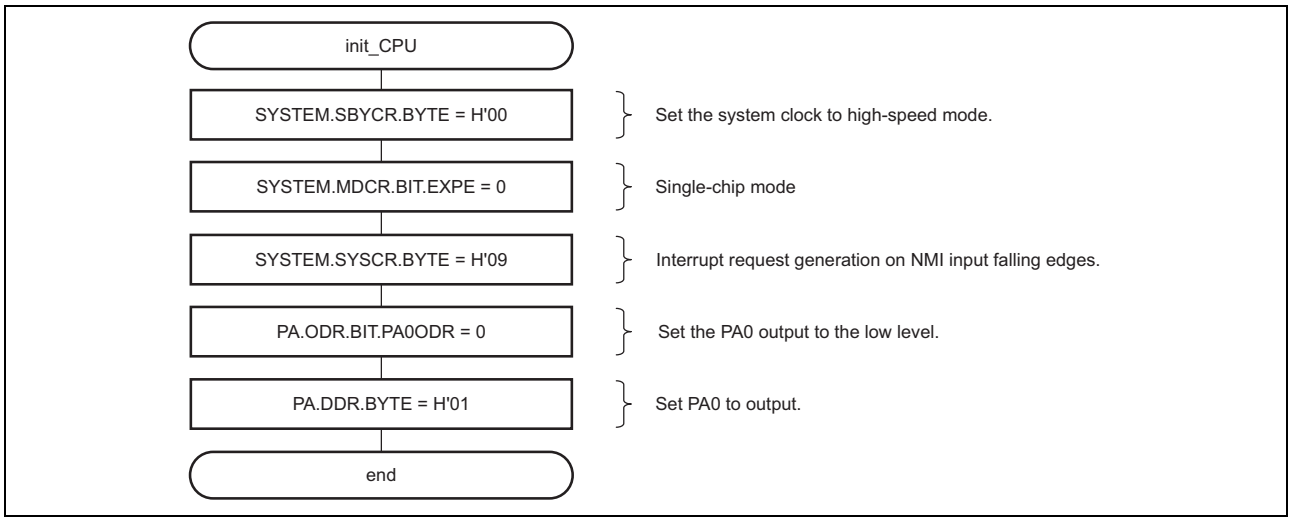


Figure 6 Flowchart (init_CPU)

5.2.4 init_WDT Function

(1) Function overview

The init_WDT function discriminates the previous reset factor (the SYSCR XRST bit level is reflected in the P40 pin output level) and initializes the WDT module operating mode.

(2) Arguments

None

(3) Returned value

None

(4) Description of internal I/O registers used

This function uses the internal registers shown below.

Note that the set values shown here are for use in this application note and differ from the initial values.

- Port 4 Data Register (P4DR) - Number of bits: 8 bits, Address: H'FFFFB7

Bit	Bit Name	Set Value	R/W	Descriptions
0	P40DR	0/1	R/W	• Normal extended mode (16-bit data bus) Since the corresponding pins function as bidirectional data bus pins, the value in these bits has no effect on operation. If this register is read, the P4DR values are read for the bits with the corresponding P4DDR bits set to 1. For the bits with the corresponding P4DDR bits cleared to 0, 1 is read.

- Port 4 Data Direction Register (P4DDR) - Number of bits: 8 bits, Address: H'FFFFB5

Bit	Bit Name	Set Value	R/W	Descriptions
0	P40DDR	1	W	• Normal extended mode (16-bit data bus) These bits have no effect on operation. • Other modes If port 4 pins are specified for use as the general I/O port, the corresponding pins function as output port when the P4DDR bits are set to 1, and as input port when cleared to 0.

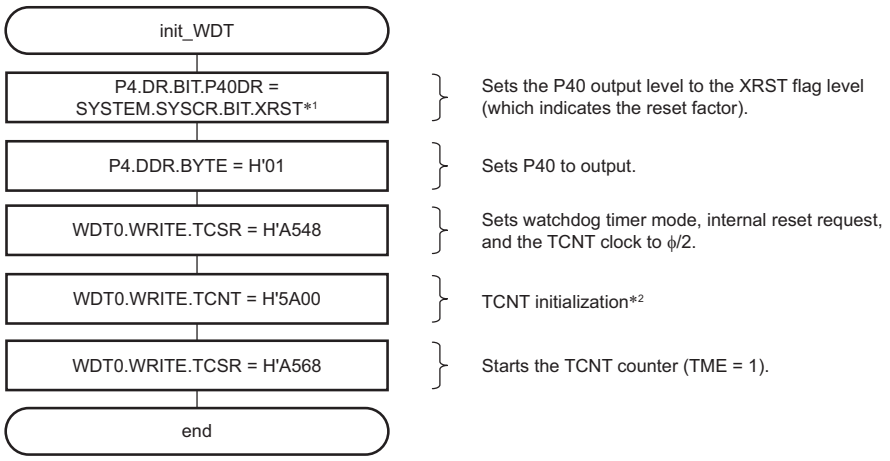
- Timer Control/Status Register_0 (write) (TCSR_0) - Number of bits: 16 bits, Address: H'FFFFA8

Bit	Bit Name	Set Value	R/W	Descriptions
6	WT/$\overline{IT}$	1	R/W	Timer Mode Select Selects whether the WDT is used as a watchdog timer or interval timer. 0: Interval timer mode 1: Watchdog timer mode
5	TME	0/1	R/W	Timer Enable When this bit is set to 1, TCNT starts counting. When this bit is cleared, TCNT stops counting and is initialized to H'00.
3	RST/$\overline{NMI}$	1	R/W	Reset or NMI Selects to request an internal reset or an NMI interrupt when TCNT has overflowed. 0: An NMI interrupt is requested 1: An internal reset is requested
2	CKS2	0	R/W	Clock Select 2 to 0
1	CKS1	0	R/W	Select the clock source to be input to TCNT. The overflow period
0	CKS0	0	R/W	for ϕ = 34 MHz is enclosed in parentheses. 000: ϕ/2 (period: 15.1 μs) 001: ϕ/64 (period: 481.9 μs) 010: ϕ/128 (period: 963.8 μs) 011: ϕ/512 (period: 3.856 ms) 100: ϕ/2048 (period: 15.42 ms) 101: ϕ/8192 (period: 61.68 ms) 110: ϕ/32768 (period: 246.7 ms) 111: ϕ/131072 (period: 986.9 ms)

- Timer Counter_0 (write) (TCNT_0) - Number of bits: 16 bits, Address: H'FFFFA8

Bit	Bit Name	Set Value	R/W	Descriptions
15 to 0	—	H'5A00	R/W	TCNT_0 is an 8-bit read/write increment-only counter. TCNT and TCSR are allocated to the same address. Therefore, when writing to TCNT, applications must transfer data in which the upper byte is H'5A and the lower byte is the desired write data value.

(5) Flowchart



Notes: 1. Port 4 is set to retain state output (the output level is retained through a reset).
2. This register can be initialized to H'00 by setting the TME bit in TCSR to 0.

Figure 7 Flowchart (init_WDT)

5.2.5 INT_NMI Function

(1) Function overview

The INT_NMI function loops indefinitely.

Since this function does not return to main, the TCNT_0 clear operation cannot be performed and TCNT overflows.

(2) Arguments

None

(3) Returned value

None

(4) Description of internal I/O registers used

None

(5) Flowchart

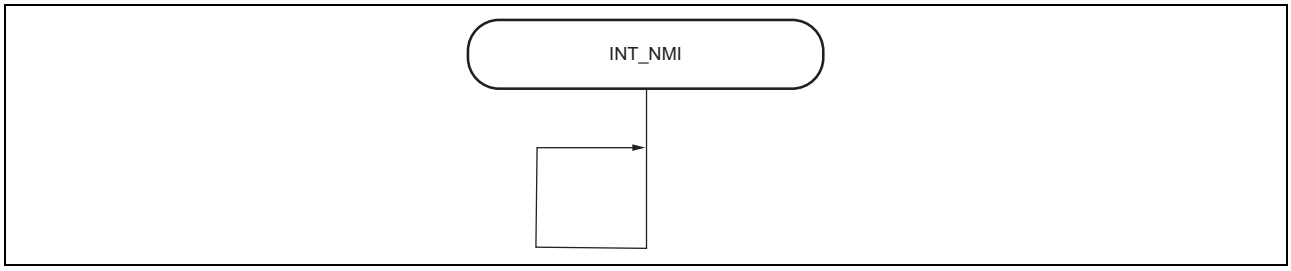


Figure 8 Flowchart (INT_NMI)

6. Reference Documents

- Hardware Manual
  H8S/2472, H8S/2463, H8S/2462 Group Hardware Manual
  (The latest version can be downloaded from the Renesas Technology Web site.)
- Development Environment Manual
  H8S/300, H8/300 Series C/C++ Compiler Package User's Manual
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