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H8S/2400 Series

SCI Asynchronous Serial Data Transmit/Receive

Introduction

This application note presents a simultaneous transmit/receive serial data transmission operation for 8 frames (8 bytes) of data that uses the serial communications interface (SCI) in asynchronous mode.

Since the transmission block and reception block are independent within the SCI module, full-duplex communication can be performed. Also, since both the transmission block and reception block have a double buffered structure, continuous transmit/receive operations are possible by writing the next transmit data during transmission and by reading the previous frame during reception.

Target Devices

- H8S/2472, H8S/2463, H8S/2462 Group

Preface

This program can be used with other H8S Family MCUs that have the same internal I/O registers as the devices on which operation has been confirmed. Check the latest version of the manual for any additions and modifications to functions.

Careful evaluation is recommended before using this application note.

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1. Specifications

This application note presents a program that transmits and receives 8 frames (8 bytes) of data at the same time, verifies the received data consistency, and outputs a high level from port A0 (PA0) if the data is normal.

Figure 1 presents an overview of the operation presented in this application note. The detailed specifications are as follows.

- Of the two SCI channels (SCI_1 and SCI_3) SCI_1 is used.
- Eight frames (8 bytes) of data are received and transmitted at the same time in asynchronous mode.
- The communication format is 8 bits, no parity, and one stop bit.
- The baud rate is set to 38,400 bps.
- The test data is set to be the ASCII codes for "R", "E", "N", "E", "S", "A", and "S".

Note: The transmitted and received used in this application note are the same.

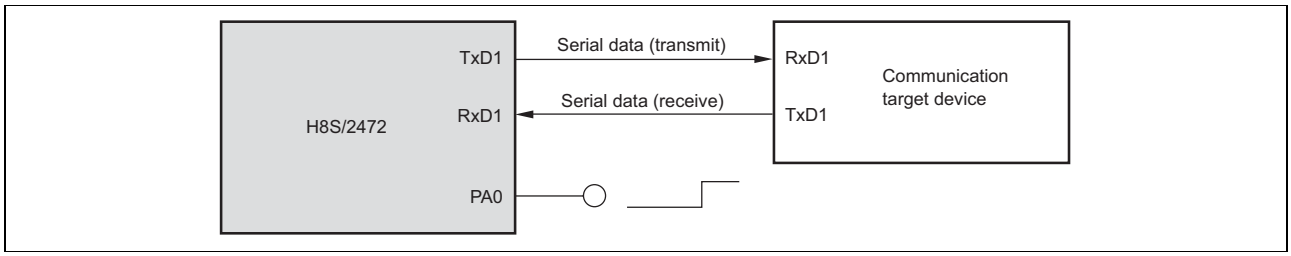

Figure 1 Asynchronous Serial Data Simultaneous Transmit/Receive Operation Overview

2. Applicable Conditions

Table 1 Applicable Conditions

Item	Description
Operating frequency	Input clock: 8 MHz System clock (ϕ): 32 MHz (8 MHz clock multiplied by 4)
Operating voltage	3.3V
Operating mode	Mode 2 ($\overline{MD2}$ = 1, MD1 = 1)
Integrated development environment	High-performance Embedded Workshop (HEW) Ver.4.04.01
Evaluation board	Renesas Technology R0K402472D000BR
C/C++ compiler	Renesas Technology H8S,H8/300 C/C++ Compiler (V.6.02.01.000)
Compiler options	-cpu=2600A:24 -optimize=0
Optimizing linkage editor	Renesas Technology Optimizing Linkage Editor (V.9.04.01.000)
Linker options	-start = PResetPRG,PIntPRG/0400, P,C,C$DSEC,C$BSEC,D/0800, B,R/0FF0800, S/0FF9600

3. Functions Used

3.1 Operation in Asynchronous Mode

Figure 2 shows the general format for asynchronous serial communication. One frame consists of a start bit (low level), followed by transmit/receive data, a parity bit, and finally stop bits (high level). In asynchronous serial communication, the transmission line is usually held in the mark state (high level). The SCI monitors the transmission line, and when it goes to the space state (low level), recognizes a start bit and starts serial communication. Inside the SCI, the transmitter and receiver are independent units, enabling full-duplex communication. Both the transmitter and the receiver also have a double-buffered structure, so that data can be read or written during transmission or reception, enabling continuous data transfer and reception.

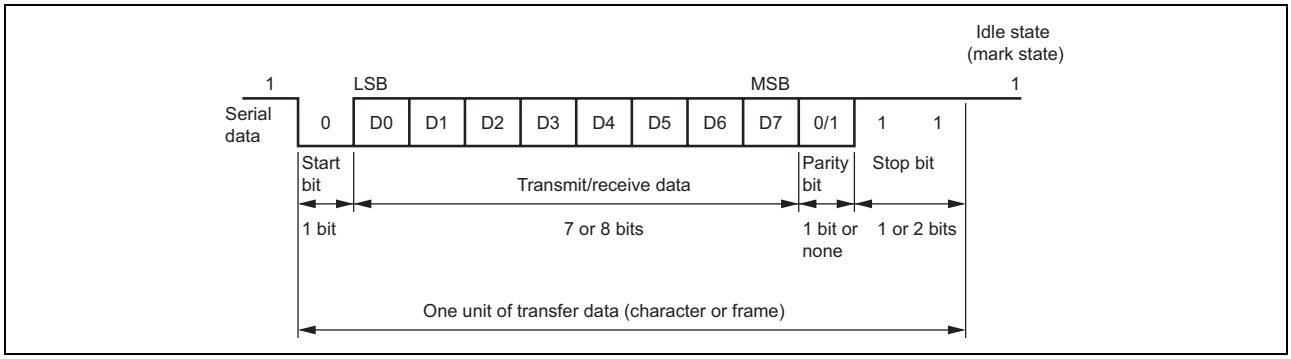

Figure 2 Data Format in Asynchronous Communication (Example with 8-Bit Data, Parity, Two Stop Bits)

3.2 Serial Data Transmission (Asynchronous Mode)

Figure 3 shows an example of the operation for transmission in asynchronous mode. In transmission, the SCI operates as described below.

1. The SCI monitors the TDRE flag in the serial status register (SSR), and if it is cleared to 0, recognizes that data has been written to the transmit data register (TDR), and transfers the data from TDR to the transmit shift register (TSR).
2. After transferring data from TDR to TSR, the SCI sets the TDRE flag to 1 and starts transmission. If the TIE bit in the serial control register (SCR) is set to 1 at this time, a transmit data empty interrupt request (TXI) is generated. Because the TXI interrupt routine writes the next transmit data to TDR before transmission of the current transmit data has finished, continuous transmission can be enabled.
3. Data is sent from the transmit data output (TxD) pin in the following order: start bit, transmit data, parity bit or multiprocessor bit (may be omitted depending on the format), and stop bit.
4. The SCI checks the TDRE flag at the timing for sending the stop bit.
5. If the TDRE flag is 0, the data is transferred from TDR to TSR, the stop bit is sent, and then serial transmission of the next frame is started.
6. If the TDRE flag is 1, the TEND flag in SSR is set to 1, the stop bit is sent, and then the "mark state" is entered in which 1 is output. If the TEIE bit in SCR is set to 1 at this time, a TEI interrupt request is generated.

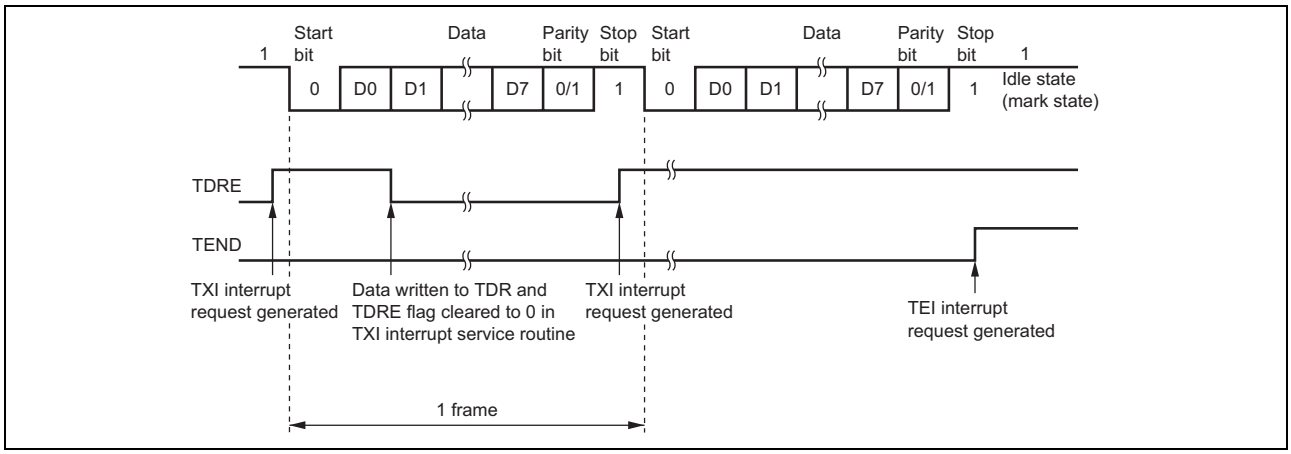

Figure 3 Example of Operation in Transmission in Asynchronous Mode (Example with 8-Bit Data, Parity, One Stop Bit)

3.3 Serial Data Reception (Asynchronous Mode)

Figure 4 shows an example of the operation for reception in asynchronous mode. In serial reception, the SCI operates as described below.

1. The SCI monitors the communication line, and if a start bit is detected, performs internal synchronization, receives receive data in the receive shift register (RSR), and checks the parity bit and stop bit.
2. If an overrun error (when reception of the next data is completed while the RDRF flag in the serial status register (SSR) is still set to 1) occurs, the ORER bit in SSR is set to 1. If the RIE bit in SCR is set to 1 at this time, an ERI interrupt request is generated. Receive data is not transferred to the receive data register (RDR). The RDRF flag remains to be set to 1.
3. If a parity error is detected, the PER bit in SSR is set to 1 and receive data is transferred to RDR. If the RIE bit in SCR is set to 1 at this time, an ERI interrupt request is generated.
4. If a framing error (when the stop bit is 0) is detected, the FER bit in SSR is set to 1 and receive data is transferred to RDR. If the RIE bit in SCR is set to 1 at this time, an ERI interrupt request is generated.
5. If reception finishes successfully, the RDRF bit in SSR is set to 1, and receive data is transferred to RDR. If the RIE bit in SCR is set to 1 at this time, an RXI interrupt request is generated. Because the RXI interrupt routine reads the receive data transferred to RDR before reception of the next receive data has finished, continuous reception can be enabled.

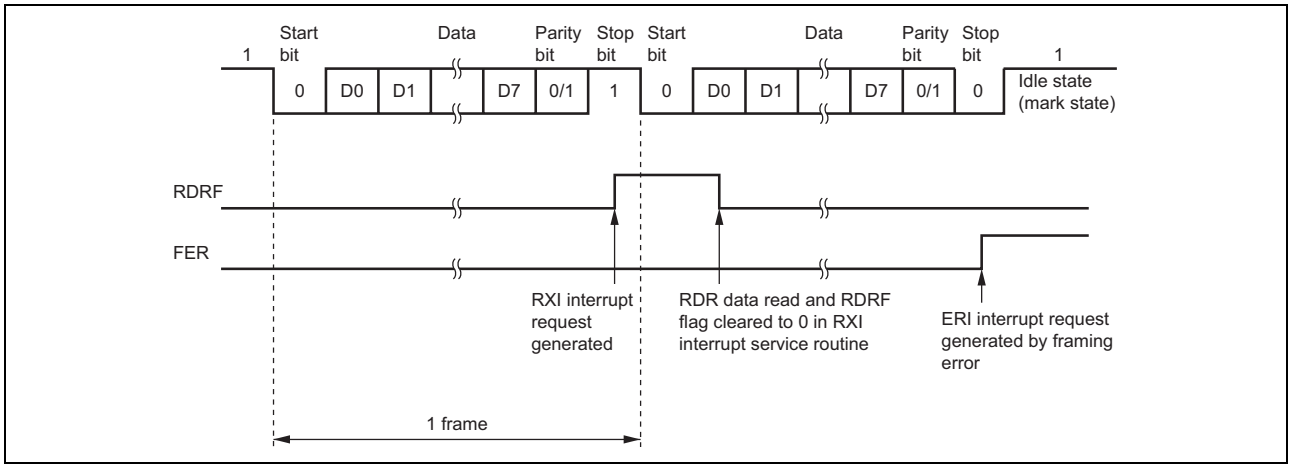

Figure 4 Example of Operation in Reception in Asynchronous Mode (Example with 8-Bit Data, Parity, One Stop Bit)

4. Operation

Figure 5 shows the asynchronous mode transmit/receive operation described in this application note.

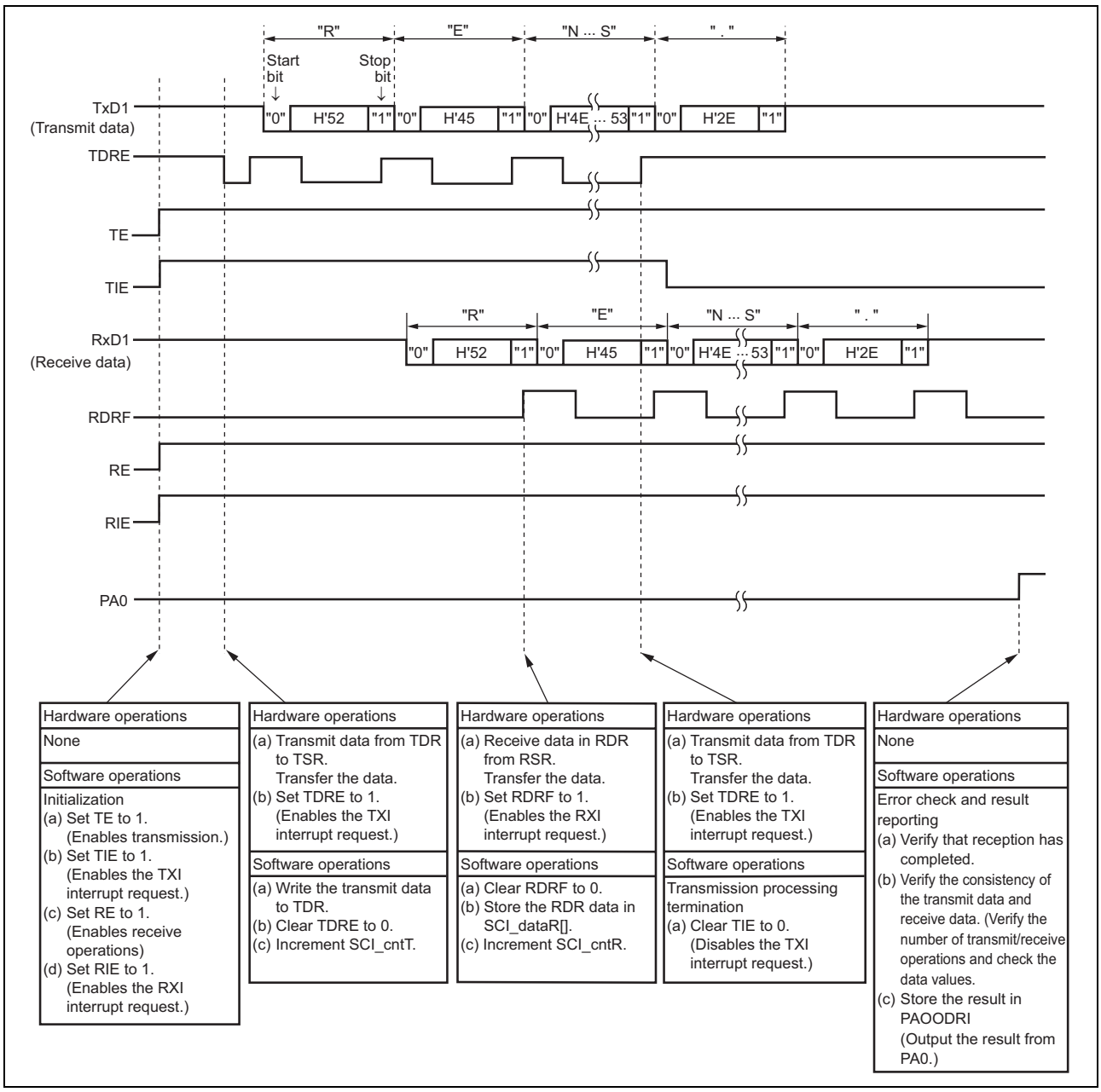

Figure 5 Asynchronous Mode Serial Data Transmit/Receive Operation

5. Software

5.1 Signal Constants

Table 2 Signal Constants

Constant	Setting	Description	Functions
FIXSCI	8	Serial communication data count	main, init_SCI, INT_SCI1_TXI1

5.2 ROM Variables

Table 3 ROM Variables

Type	Variable	Setting	Description	Functions
const unsigned char	SCI_dataT[0]	H'52	Transmission data 1	main, INT_SCI1_TXI1
	SCI_dataT[1]	H'45	Transmission data 2	main, INT_SCI1_TXI1
	SCI_dataT[2]	H'4E	Transmission data 3	main, INT_SCI1_TXI1
	SCI_dataT[3]	H'45	Transmission data 4	main, INT_SCI1_TXI1
	SCI_dataT[4]	H'53	Transmission data 5	main, INT_SCI1_TXI1
	SCI_dataT[5]	H'41	Transmission data 6	main, INT_SCI1_TXI1
	SCI_dataT[6]	H'53	Transmission data 7	main, INT_SCI1_TXI1
	SCI_dataT[7]	H'2E	Transmission data 8	main, INT_SCI1_TXI1

5.3 RAM Variables

Table 4 RAM Variables

Type	Variable	Description	Functions
unsigned char	USER_error	Error detection count counter	main, INT_SCI1_ERI1
unsigned char	SCI_dataR[ ]	SCI receive data storage destination	main, init_SCI, INT_SCI1_RXI1
unsigned char	SCI_cntT	SCI transmit counter	main, init_SCI, INT_SCI1_TXI1
unsigned char	SCI_cntR	SCI receive counter	main, init_SCI, INT_SCI1_RXI1

5.4 Functions

Table 5 Functions

Function Name	Description
PowerOn_Reset	• Initialization function Initializes the stack pointer (SP), sets interrupt mask bits, sets up uninitialized and initialized data, and calls the main function.
main	• Main function Calls the init_CPU and init_SCI functions.
init_CPU	• I/O register initialization function Initializes the registers.
init_SCI	• SCI initialization function Sets the SCI communication mode and starts operation.
INT_SCI1_RXI1	• Receive data full interrupt handler Manages storage of the receive data and the reception event count.
INT_SCI1_TXI1	• Transmit data empty interrupt handler Manages setting up the transmit data and the transmission event count.
INT_SCI1_ERI1	• Receive error interrupt handler Manages the overrun and framing error detection counts.

5.5 Function Descriptions

5.5.1 PowerON_Reset Function

(1) Function overview

The PowerON_Reset function initializes the stack pointer (SP), prepares the embedded functions and standard library functions, sets the interrupt mask bits, and sets up the uninitialized and initialized data. Then it calls the main function.

(2) Arguments

None

(3) Returned value

None

(4) Description of internal I/O registers used

None

(5) Flowchart

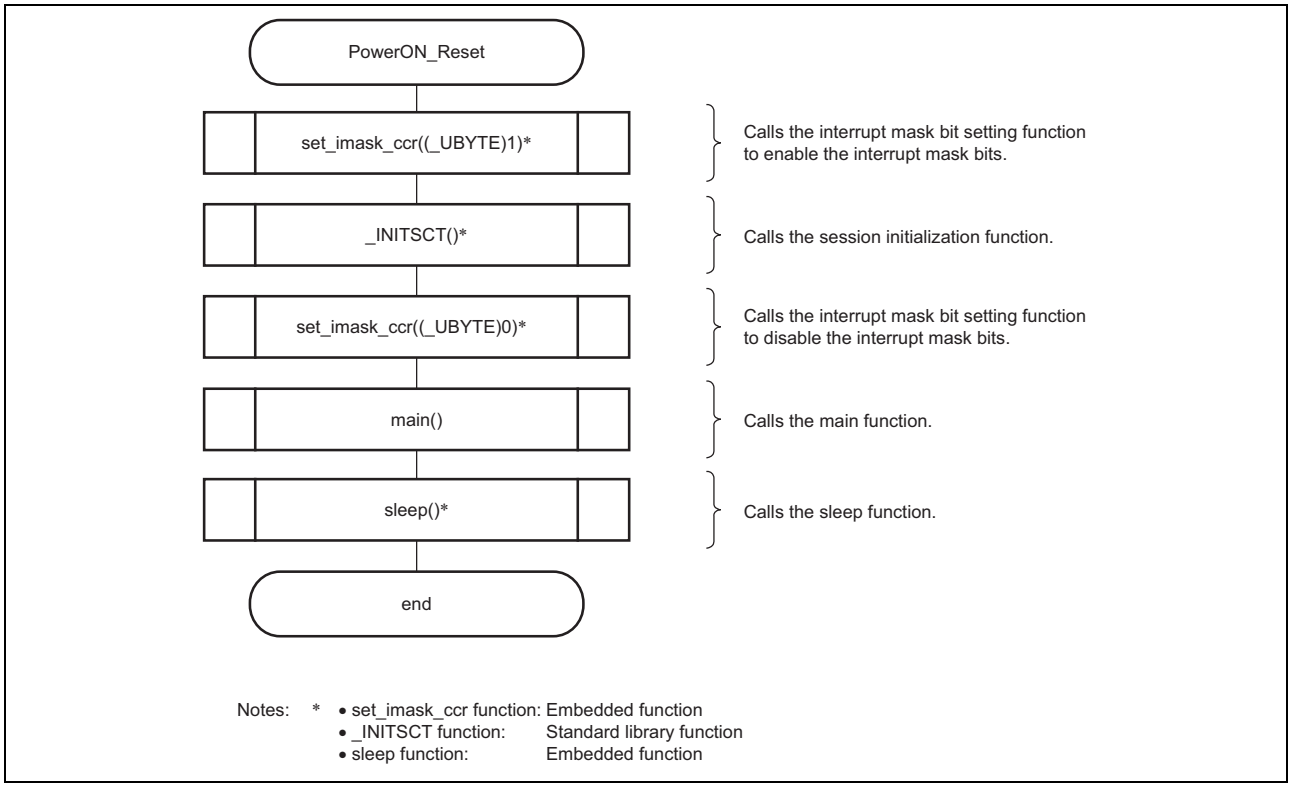

Figure 6 Flowchart (PowerON_Reset)

5.5.2 main Function

(1) Function overview

The main function calls the init_CPU and init_SCI functions. Also, after the serial transmit/receive operation completes, it verifies the transmit and receive counts, compares and evaluates the data, and outputs the result from PA0.

(2) Arguments

None

(3) Returned value

None

(4) Description of internal I/O registers used

This function uses the internal registers shown below.

Note that the set values shown here are for use in this application note and differ from the initial values.

- Port A Output Data Register (PAODR) - Number of bits: 8 bits, Address: H'FFFFAA

Bit	Bit Name	Set Value	R/W	Descriptions
0	PA0ODR	0/1	R/W	Holds the output data for pins used as general-purpose output ports.

(5) Flowchart

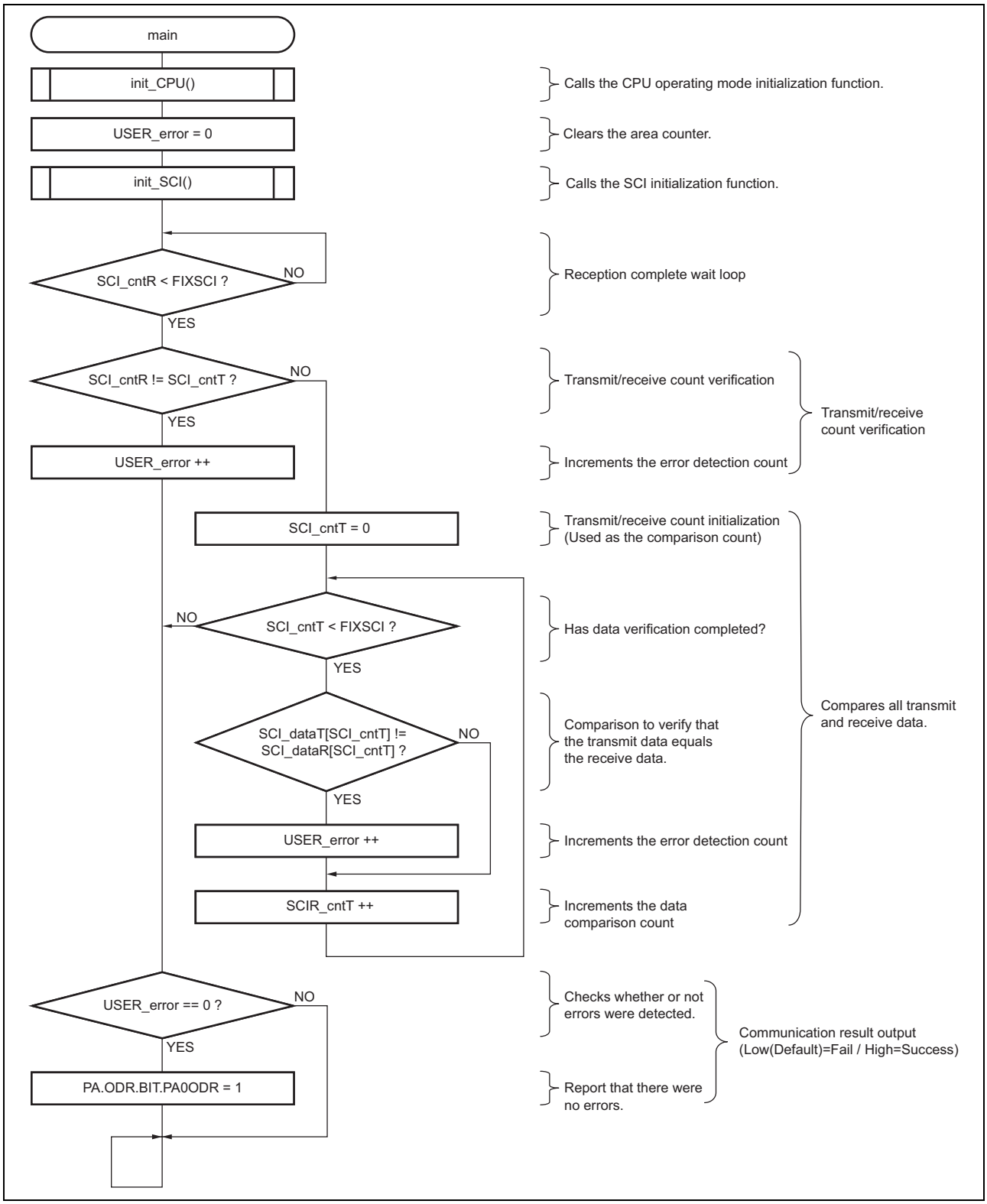

Figure 7 Flowchart (main)

5.5.3 init_CPU Function

(1) Function overview

The init_CPU function initializes the system cock settings and the CPU operating mode.

(2) Arguments

None

(3) Returned value

None

(4) Description of internal I/O registers used

This function uses the internal registers shown below.

Note that the set values shown here are for use in this application note and differ from the initial values.

- Standby Control Register (SBYCR) - Number of bits: 8 bits, Address: H'FFFF84

Bit	Bit Name	Set Value	R/W	Descriptions
2	SCK2	0	R/W	System Clock Select 2 to 0
1	SCK1	0	R/W	Select a clock for the bus master in high-speed mode or medium-speed mode.
0	SCK0	0	R/W	000: High-speed mode 001: Medium-speed clock: φ/2 010: Medium-speed clock: φ/4 011: Medium-speed clock: φ/8 100: Medium-speed clock: φ/16 101: Medium-speed clock: φ/32 11x: Must not be set.

Legend:
x: Don't care

- Mode Control Register (MDCR) - Number of bits: 8 bits, Address: H'FFFFC5

Bit	Bit Name	Set Value	R/W	Descriptions
7	EXPE	0	R/W	Extended Mode Enable Specifies extended mode. 0: Single-chip mode 1: Extended mode

- Port A Data Direction Register (PADDR) - Number of bits: 8 bits, Address: H'FFFFAB

Bit	Bit Name	Set Value	R/W	Descriptions
0	PA0DDR	1	W	When set to 1, the corresponding pins function as output port pins; when cleared to 0, function as input port pins. As the address of this register is the same as that of Port A Input Data Register (PAPIN), reading from this register indicates the state of port A.

- Port A Output Data Register (PAODR) - Number of bits: 8 bits, Address: H'FFFFAA

Bit	Bit Name	Set Value	R/W	Descriptions
0	PA0ODR	0	R/W	Holds the output data for pins used as general-purpose output ports.

(5) Flowchart

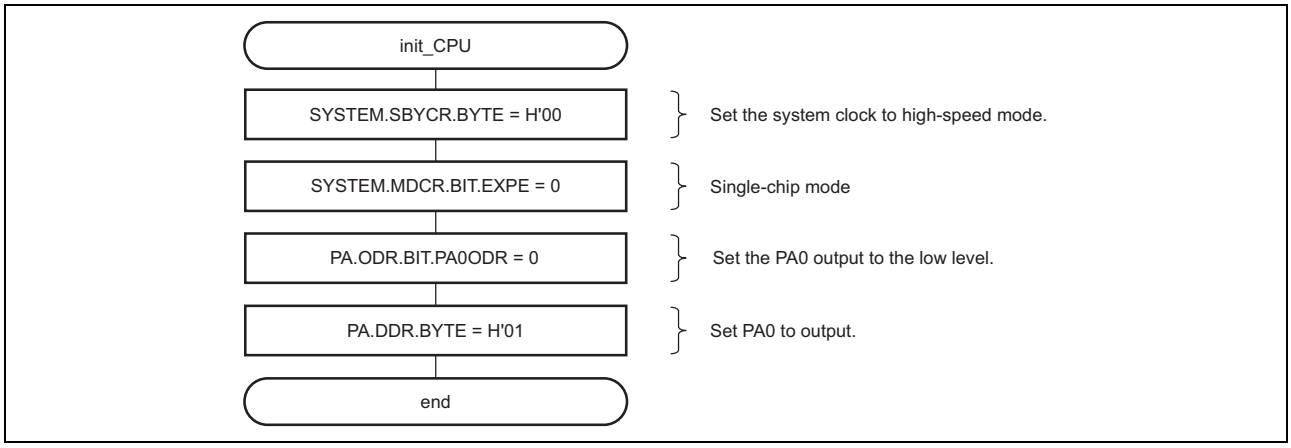

Figure 8 Flowchart (init_CPU)

5.5.4 init_SCI Function

(1) Function overview

The init_SCI function initializes the receive data and the SCI module.

(2) Arguments

None

(3) Returned value

None

(4) Description of internal I/O registers used

This function uses the internal registers shown below.

Note that the set values shown here are for use in this application note and differ from the initial values.

- Module Stop Control Register L (MSTPCRL) - Number of bits: 8 bits, Address: H'FFFF87

Bit	Bit Name	Set Value	R/W	Descriptions
6	MSTP6	0	R/W	Serial communications interface 1 (SCI_1) 1: The module switches to module stop mode at the point the bus cycle completes. 0: Module stop mode is cleared and operation restarts at the point the bus cycle completes.

- Serial Mode Register_1 (SMR_1) - Number of bits: 8 bits, Address: H'FFFE98

Bit	Bit Name	Set Value	R/W	Descriptions
7	C/$\overline{A}$	0	R/W	Communication Mode 0: Asynchronous mode 1: Clock synchronous mode
6	CHR	0	R/W	Character Length (enabled only in asynchronous mode) 0: Selects 8 bits as the data length. 1: Selects 7 bits as the data length. LSB-first is fixed and the MSB of TDR is not transmitted in transmission.
5	PE	0	R/W	Parity Enable (enabled only in asynchronous mode) When this bit is set to 1, the parity bit is added to transmit data before transmission, and the parity bit is checked in reception. For a multiprocessor format, parity bit addition and checking are not performed regardless of the PE bit setting.
4	O/$\overline{E}$	0	R/W	Parity Mode (enabled only when the PE bit is 1 in asynchronous mode) 0: Selects even parity. 1: Selects odd parity.
3	STOP	0	R/W	Stop Bit Length (enabled only in asynchronous mode) Selects the stop bit length in transmission. 0: 1 stop bit 1: 2 stop bits
2	MP	0	R/W	Multiprocessor Mode (enabled only in asynchronous mode) When this bit is set to 1, the multiprocessor communication function is enabled. The PE bit and O/$\overline{E}$ bit settings are invalid in multiprocessor mode.
1	CKS1	0	R/W	Clock Select 1 and 0
0	CKS0	0	R/W	These bits select the clock source for the baud rate generator. 00: ϕ clock (n = 0) 01: ϕ/4 clock (n = 1) 10: ϕ/16 clock (n = 2) 11: ϕ/64 clock (n = 3)

- Bit Rate Register_1 (BBR_1) - Number of bits: 8 bits, Address: H'FFFE99
  The bit rate register (BBR_1) is an 8-bit register that sets the transmit/receive bit rate to match the baud rate register's operating clock selected by CKS1 and CKS0 in SMR_1. Since the SCI module has an independent baud rate register for each channel, different bit rates can be set for each channel. The initial value of BRR is H'FF and it can be read from or written to by the CPU at all times.

Table 6 lists sample settings for BRR in asynchronous mode.

Table 6 BRR Setting Examples for Specific Bit Rates

	Operating frequency ϕ = 32 MHz		
Bit Rate (bit/s)	**n**	**N**	**Error (%)**
4800	0	207	0.16
9600	0	103	0.16
19200	0	51	0.16
31250	0	31	0.00
38400	0	25	0.16

Notes: n: Determined by the SMR_1 CKS1 and CKS0 settings. When CKS1 and CKS0 are both 0, n will be 1.
N: The BRR setting.
See the hardware manual for details on these settings.

- Serial Control Register_1 (SCR_1) - Number of bits: 8 bits, Address: H'FFFE9A

Bit	Bit Name	Set Value	R/W	Descriptions
7	TIE	1	R/W	Transmit Interrupt Enable When this bit is set to 1, a TXI interrupt request is enabled.
6	RIE	1	R/W	Receive Interrupt Enable When this bit is set to 1, RXI and ERI interrupt requests are enabled.
5	TE	1	R/W	Transmit Enable When this bit is set to 1, transmission is enabled.
4	RE	1	R/W	Receive Enable When this bit is set to 1, reception is enabled.
3	MPIE	0	R/W	Multiprocessor Interrupt Enable (enabled only when the MP bit in SMR is 1 in asynchronous mode) When this bit is set to 1, receive data in which the multiprocessor bit is 0 is skipped, and setting of the RDRF, FER, and ORER status flags in SSR is disabled. On receiving data in which the multiprocessor bit is 1, this bit is automatically cleared and normal reception is resumed.
2	TEIE	0	R/W	Transmit End Interrupt Enable When this bit is set to 1, a TEI interrupt request is enabled.
1	CKE1	0	R/W	Clock Enable 1 and 0
0	CKE0	1	R/W	These bits select the clock source and SCK pin function. Asynchronous mode: 00: Internal clock 01: Internal clock 1x: External clock Clock synchronous mode: 0x: Internal clock 1x: External clock

Legend:
x: Don't care

- Smart Card Mode Register_1 (SCMR_1) - Number of bits: 8 bits, Address: H'FFFE9E

Bit	Bit Name	Set Value	R/W	Descriptions
7 to 4	—	1	R	Reserved These bits are always read as 1 and cannot be modified.
3	SDIR	0	R/W	Smart Card Data Transfer Direction Selects the serial/parallel conversion format. 0: TDR contents are transmitted with LSB-first. Stores receive data as LSB first in RDR. 1: TDR contents are transmitted with MSB-first. Stores receive data as MSB first in RDR. The SDIR bit is valid only when the 8-bit data format is used for transmission/reception; when the 7-bit data format is used, data is always transmitted/received with LSB-first.
2	SINV	0	R/W	Smart Card Data Invert Specifies inversion of the data logic level. The SINV bit does not affect the logic level of the parity bit. When the parity bit is inverted, invert the O/$\overline{E}$ bit in SMR. 0: TDR contents are transmitted as they are. Receive data is stored as it is in RDR. 1: TDR contents are inverted before being transmitted. Receive data is stored in inverted form in RDR.
1	—	1	R	Reserved This bit is always read as 1 and cannot be modified.
0	SMIF	0	R/W	Smart Card Interface Mode Select When this bit is set to 1, smart card interface mode is selected. 0: Normal asynchronous or clock synchronous mode 1: Smart card interface mode

(5) Flowchart

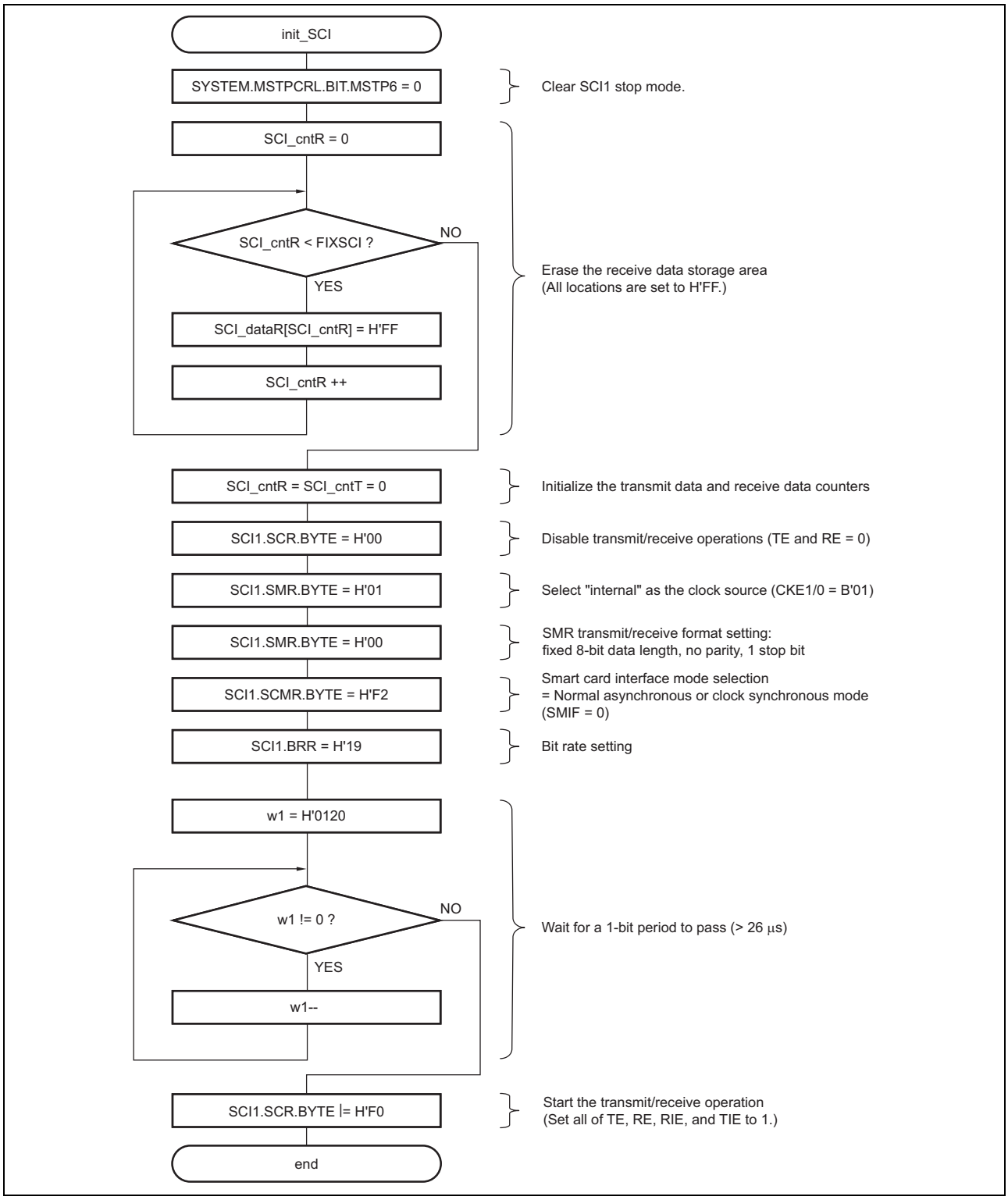

Figure 9 Flowchart (init_SCI)

5.5.5 INT_SCI1_RXI1 Function

(1) Function overview

The INT_SCI1_RXI1 function stores the RDR receive data, determines whether or not reception has completed, and clears the RDRF flag.

(2) Arguments

None

(3) Returned value

None

(4) Description of internal I/O registers used

This function uses the internal registers shown below.

Note that the set values shown here are for use in this application note and differ from the initial values.

- Serial Status Register_1 (SSR_1) - Number of bits: 8, Address: H'FFFE9C

Bit	Bit Name	Set Value	R/W	Descriptions
6	RDRF	0/1	R/(W)*	Receive Data Register Full Indicates that receive data is stored in RDR. [Setting condition] • When serial reception ends normally and receive data is transferred from RSR to RDR [Clearing conditions] • When 0 is written to RDRF after reading RDRF = 1 • When an RXI interrupt request is issued allowing DTC to read data from RDR The RDRF flag is not affected and retains its previous value when the RE bit in SCR is cleared to 0.

Note: * Only 0 can be written to clear the flag.

- Receive Data Register_1 (RDR_1) - Number of bits: 8, Address: H'FFFE9D
  Receive data register (RDR_1) is an 8-bit register that holds receive data. When one frame of data has been received, the receive data is transferred from RSR to this register making it possible for RSR to accept the next receive data.

(5) Flowchart

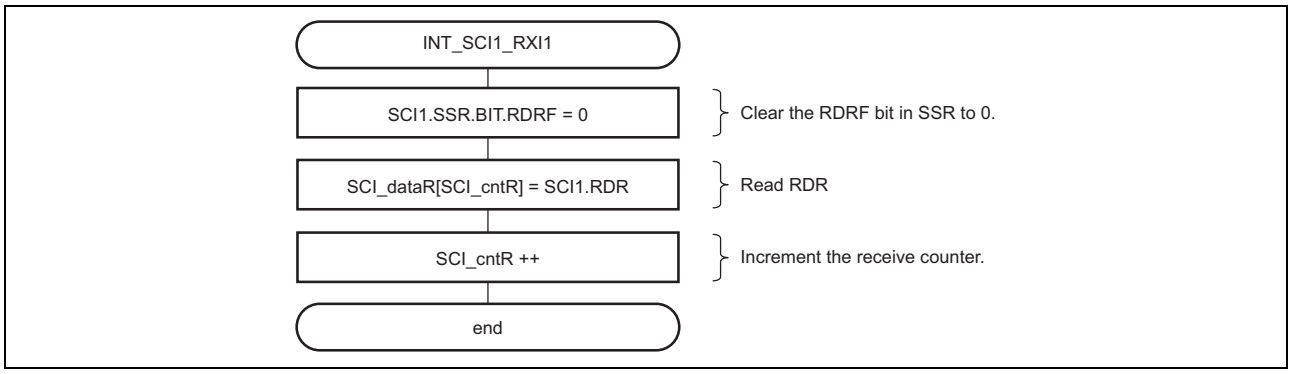

Figure 10 Flowchart (INT_SCI1_RXI1)

5.5.6 INT_SCI1_TXI1 Function

(1) Function overview

The INT_SCI1_TXI1 function stores the transmit data in TDR, determines whether or not the data to be transmitted has been competed, and clears the TDRE flag.

(2) Arguments

None

(3) Returned value

None

(4) Description of internal I/O registers used

This function uses the internal registers shown below.

Note that the set values shown here are for use in this application note and differ from the initial values.

- Serial Status Register_1 (SSR_1) - Number of bits: 8, Address: H'FFFE9C

Bit	Bit Name	Set Value	R/W	Descriptions
7	TDRE	0/1	R/(W)*	Transmit Data Register Empty Indicates whether TDR contains transmit data. [Setting conditions] • When the TE bit in SCR is 0 • When data is transferred from TDR to TSR and TDR is ready for data write [Clearing conditions] • When 0 is written to TDRE after reading TDRE = 1 • When a TXI interrupt request is issued allowing DTC to write data to TDR

Note: * Only 0 can be written to clear the flag.

- Serial Control Register_1 (SCR_1) - Number of bits: 8, Address: H'FFFE9A

Bit	Bit Name	Set Value	R/W	Descriptions
7	TIE	0	R/W	Transmit Interrupt Enable When this bit is set to 1, a TXI interrupt request is enabled.
6	RIE	0/1	R/W	Receive Interrupt Enable When this bit is set to 1, RXI and ERI interrupt requests are enabled.
5	TE	0/1	R/W	Transmit Enable When this bit is set to 1, transmission is enabled.
4	RE	0/1	R/W	Receive Enable When this bit is set to 1, reception is enabled.
3	MPIE	0/1	R/W	Multiprocessor Interrupt Enable (enabled only when the MP bit in SMR is 1 in asynchronous mode) When this bit is set to 1, receive data in which the multiprocessor bit is 0 is skipped, and setting of the RDRF, FER, and ORER status flags in SSR is disabled. On receiving data in which the multiprocessor bit is 1, this bit is automatically cleared and normal reception is resumed.
2	TEIE	0/1	R/W	Transmit End Interrupt Enable When this bit is set to 1, a TEI interrupt request is enabled.
1	CKE1	0/1	R/W	Clock Enable 1 and 0
0	CKE0	0/1	R/W	These bits select the clock source and SCK pin function. Asynchronous mode: 00: Internal clock 01: Internal clock 1x: External clock Clock synchronous mode: 0x: Internal clock 1x: External clock

Legend:
x: Don't care

- Transmit Data Register (TDR_1) - Number of bits: 8, Address: H'FFFE9B
  The transmit data register (TDR_1) is an 8-bit register that holds the transmit data. When the transmit shift register (TSR) empty state is detected, the transmit data written to TDR is transferred to TSR. When one frame of data has been transmitted, if the next transmit data has been written to TDR, that data will be transferred to TSR and data transmission will continue.

(5) Flowchart

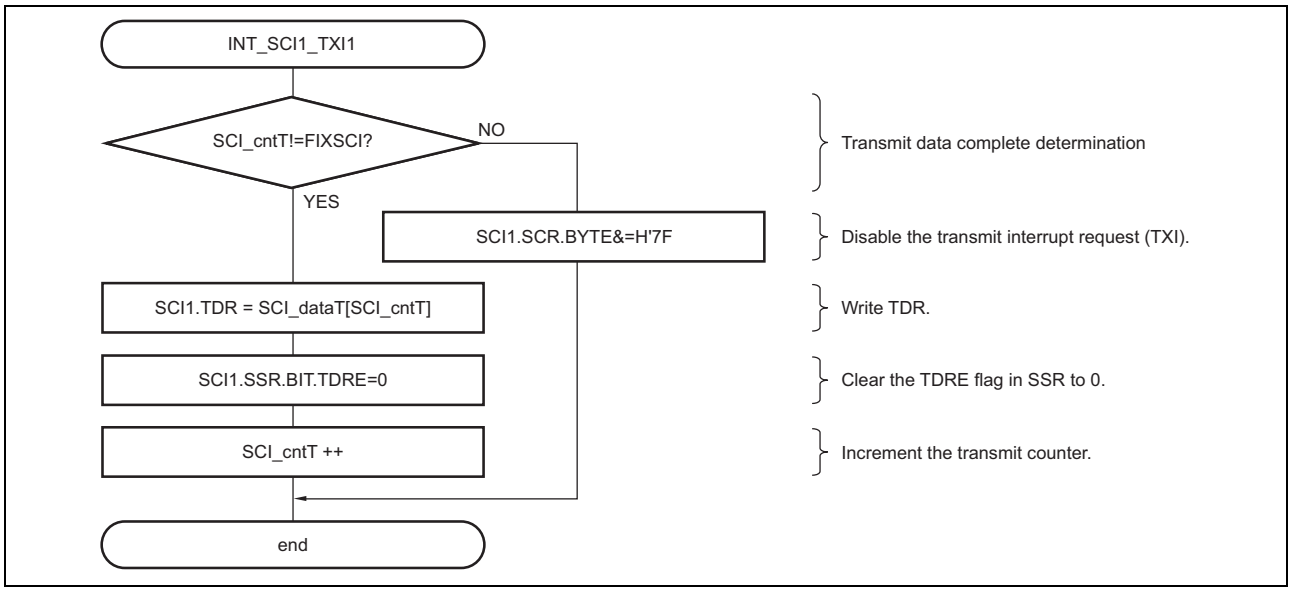

Figure 11 Flowchart (INT_SCI1_TXI1)

5.5.7 INT_SCI1_ERI1 Function

(1) Function overview

The INT_SCI1_ERI1 function increments the error detection count each time an overrun error is detected.

(2) Arguments

None

(3) Returned value

None

(4) Description of internal I/O registers used

This function uses the internal registers shown below.

Note that the set values shown here are for use in this application note and differ from the initial values.

- Serial Status Register_1 (SSR_1) - Number of bits: 8, Address: H'FFFE9C

Bit	Bit Name	Set Value	R/W	Descriptions
5	ORER	0	R/(W)*	Overrun Error [Setting condition] When the next serial reception is completed while RDRF = 1 [Clearing condition] When 0 is written to ORER after reading ORER = 1
4	FER	0	R/(W)*	Framing Error [Setting condition] When the stop bit is 0 [Clearing condition] When 0 is written to FER after reading FER = 1 In 2-stop-bit mode, only the first stop bit is checked.

Note: * Only 0 can be written to clear the flag.

(5) Flowchart

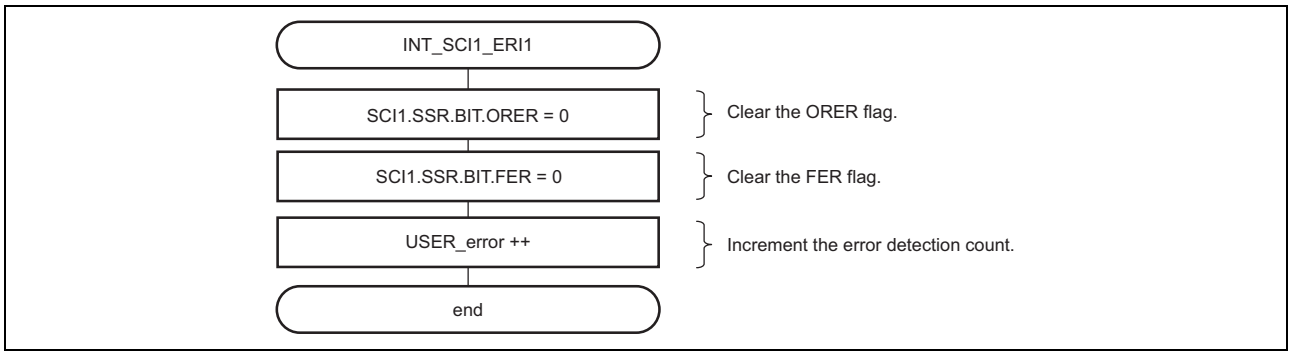

Figure 12 Flowchart (INT_SCI1_ERI1)

6. Reference Documents

- Hardware Manual
  H8S/2472, H8S/2463, H8S/2462 Group Hardware Manual
  (The latest version can be downloaded from the Renesas Technology Web site.)
- Development Environment Manual
  H8S/300, H8/300 Series C/C++ Compiler Package User's Manual
  (The latest version can be downloaded from the Renesas Technology Web site.)
- Technical News/Technical Updates
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