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H8S/2400 Series

Pulse Generation Example Using an 8-Bit Timer (TMR)

Introduction

This Application Note presents an 8-bit timer (TMR) based pulse generation sample application.

This application generates a continuous pulse signal with a fixed period using the TMR module's compare match A and compare match B functions.

Target Devices

- H8S/2472, H8S/2463, H8S/2462 Group

Preface

This program can be used with other H8S Family MCUs that have the same internal I/O registers as the devices on which operation has been confirmed. Check the latest version of the manual for any additions and modifications to functions.

Careful evaluation is recommended before using this application note.

Contents

1. Specifications

This application note presents a program that uses the compare match A and B interrupts and port A0 (PA0) to generate a 10 kHz, 50% duty pulse signal.

Figure 1 presents an overview of the operation presented in this application note. The detailed specifications are as follows.

- Of the two 8-bit timer channels (TMR_0 and TMR_1), this application uses TMR_0.
- The pulse period (100 μs) is set in the TMR timer constant register A (TCORA) and the duty of 50% (50 μs) is set in timer constant register B (TCORB).
- Compare match A is set as the clear condition for the timer counter (TCNT_0).
- The PA0 pin is set to the high-level output state in compare match A interrupt handling.
- The PA0 pin is set to the low-level output state in compare match B interrupt handling.

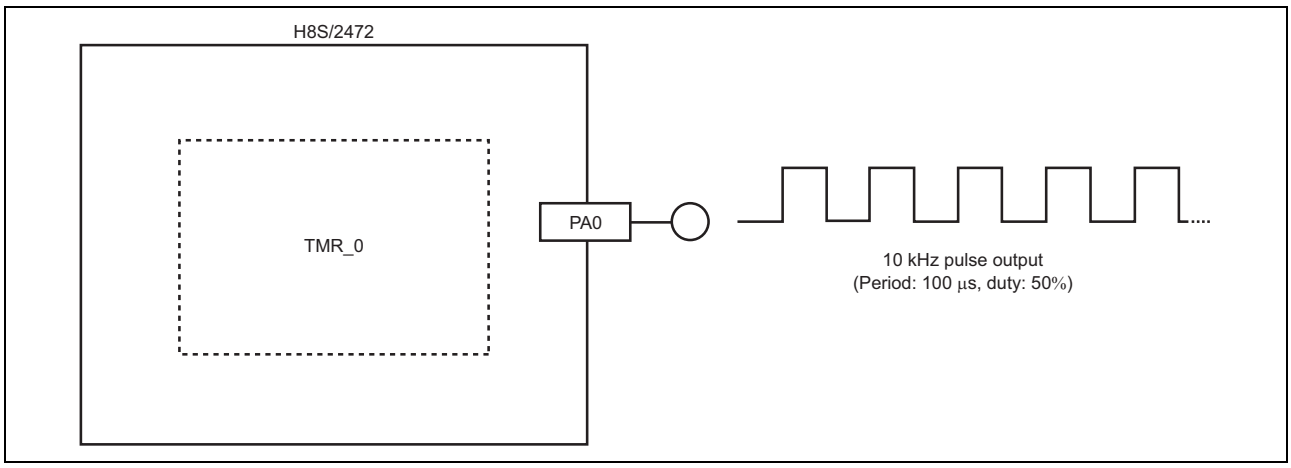

Figure 1 Operational Overview

2. Applicable Conditions

Table 1 Applicable Conditions

Item	Description
Operating frequency	Input clock: 8 MHz System clock (ϕ): 32 MHz (8 MHz clock multiplied by 4)
Operating voltage	3.3V
Operating mode	Mode 2 ($\overline{MD2}$ = 1, MD1 = 1)
Integrated development environment	High-performance Embedded Workshop(HEW) Version 4.04.01.001
Evaluation board	Renesas Technology Corp. R0K402472D000BR
C/C++ compiler	Renesas Technology Corp. H8S,H8/300 C/C++ Compiler (V.6.02.01.000)
Compiler options	-cpu=2600A:24 -optimize=0
Optimizing linkage editor	Renesas Technology Corp. Optimizing Linkage Editor (V.9.04.01.000)
Link options	-start = PResetPRG,PIntPRG/0400, P,C$DSEC,C$BSEC,D/0800, B,R/0FF0800, S/0FF9600

3. Functions Used

3.1 TCNT Count Timing

Figure 2 shows the Timer Counter (TCNT) count timing with an internal clock source.

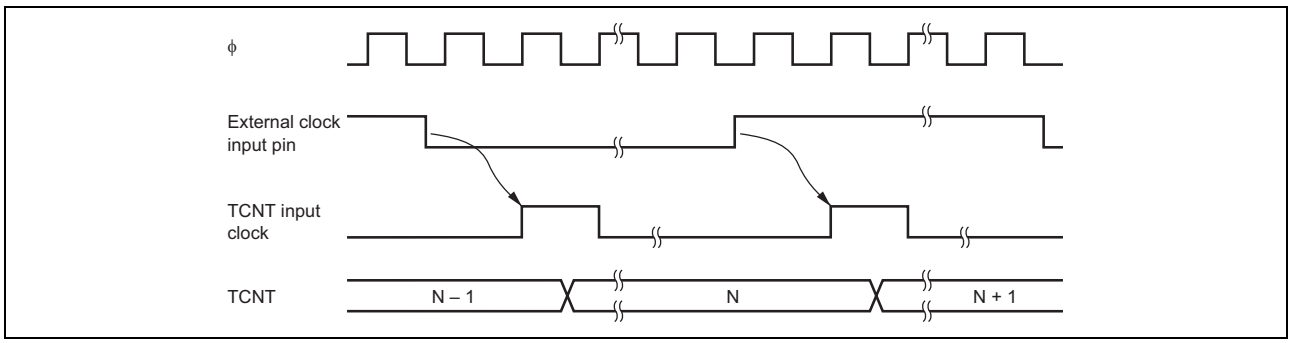

Figure 2 Count Timing for Internal Clock Input

3.2 Timing of CMFA and CMFB Setting at Compare-Match

The CMFA and CMFB flags in Timer Control/Status Register (TCSR) are set to 1 by a compare-match signal generated when the TCNT and TCOR values match. The compare-match signal is generated at the last state in which the match is true, just when the timer counter is updated. Therefore, when TCNT and TCOR match, the compare-match signal is not generated until the next TCNT input clock. Figure 3 shows the timing of CMF flag setting.

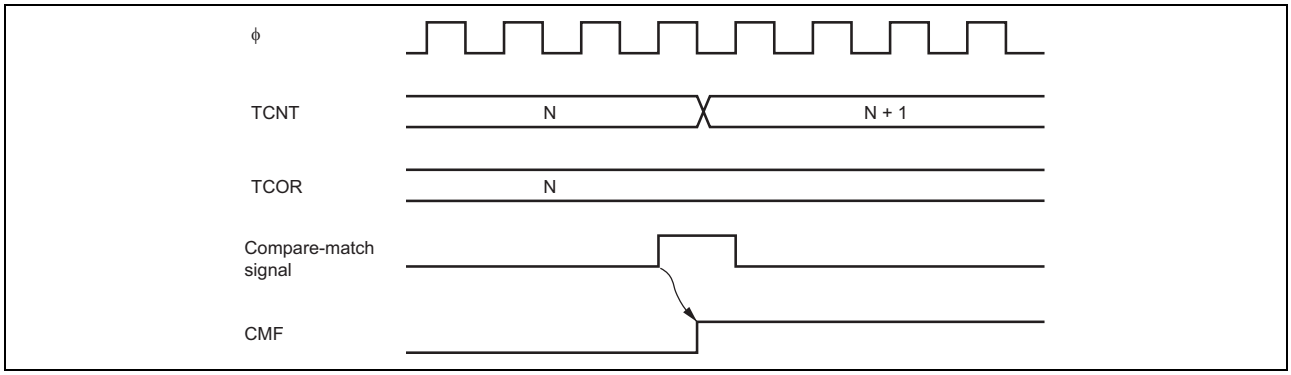

Figure 3 Timing of CMF Setting at Compare-Match

3.3 Timing of Counter Clear at Compare-Match

TCNT is cleared when compare-match A or compare-match B occurs, depending on the setting of the CCLR1 and CCLR0 bits in Timer Control Register (TCR). Figure 4 shows the timing of clearing the counter by a compare-match.

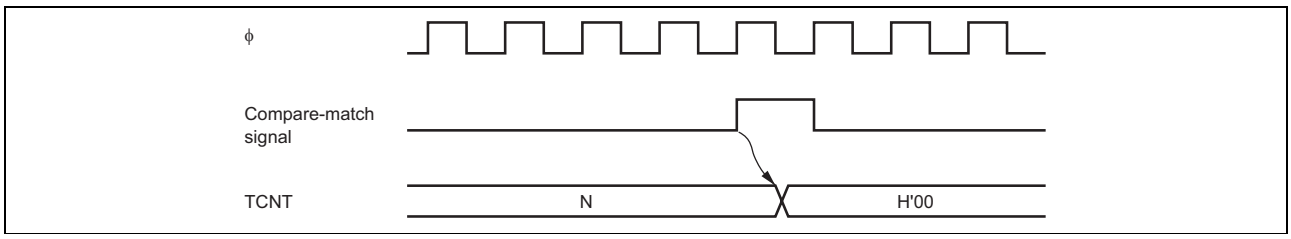

Figure 4 Timing of Counter Clear by Compare-Match

4. Operation

Figure 5 shows the TMR-based pulse generation function described in this application note.

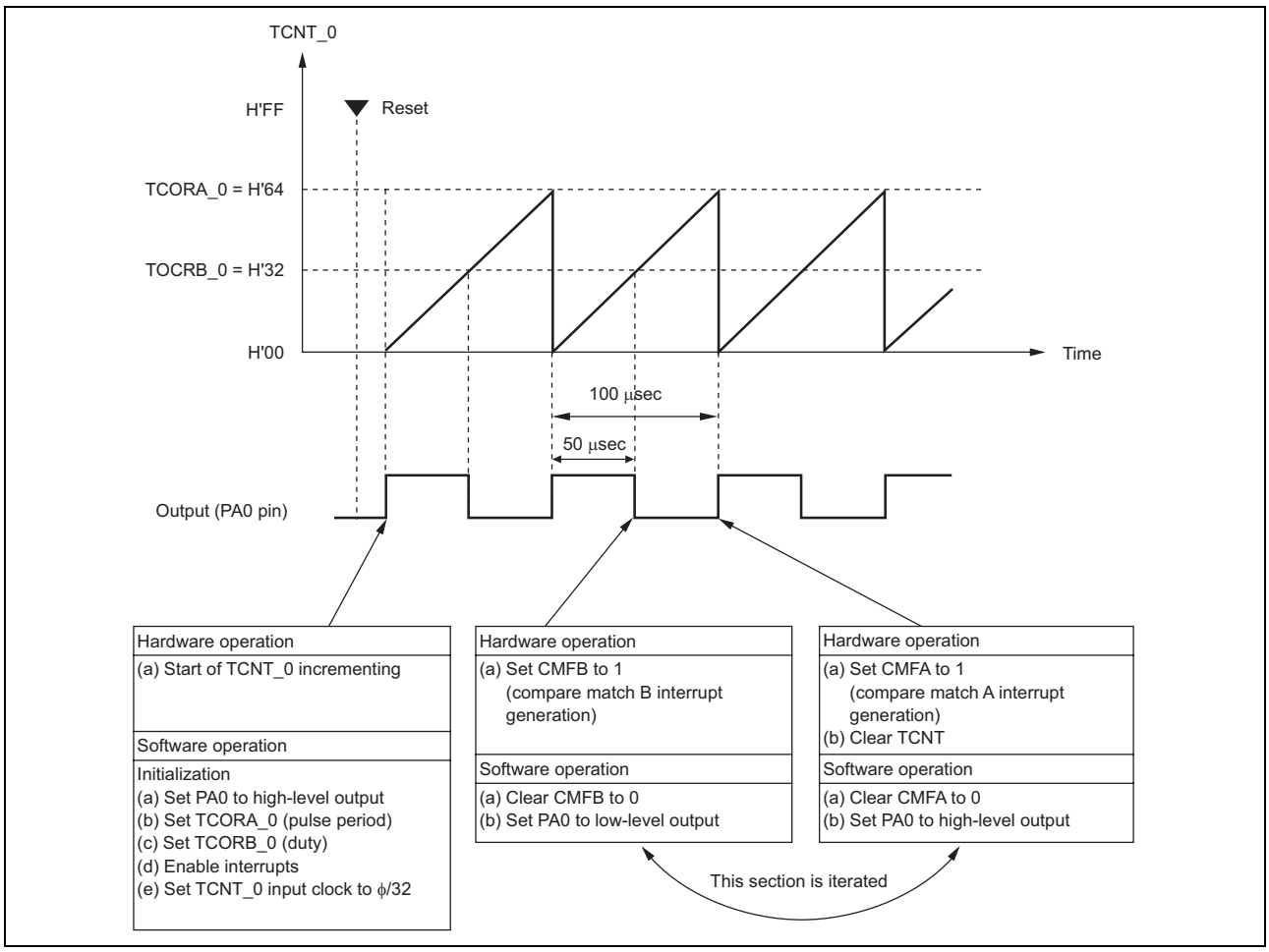

Figure 5 8-Bit Timer (TMR) Pulse Signal Generation

5. Software

5.1 Functions

Table 2 Functions

Function Name	Description
PowerOn_Reset	• Initialization function Initializes the stack pointer (SP), sets interrupt mask bits, sets up uninitialized and initialized data, and calls the main() function.
main	• Main function Calls the init_CPU and init_TMR functions.
init_CPU	• I/O register initialization function Initializes each of the registers.
init_TMR	• TMR initialization function Sets up TMR operation and starts that operation.
INT_TMR0_CMIA0	• Output compare interrupt A function Sets the PA0 pin output level to high (pulse period management)
INT_TMR0_CMIB0	• Output compare interrupt B function Sets the PA0 pin output level to low (duty management)

5.2 Function Descriptions

5.2.1 PowerON_Reset Function

(1) Function overview

The PowerON_Reset function initializes the stack pointer (SP), prepares the embedded functions and standard library functions, sets the interrupt mask bits, and sets up the uninitialized and initialized data. Then it calls the main function.

(2) Arguments

None

(3) Returned value

None

(4) Description of internal I/O registers used

None

(5) Flowchart

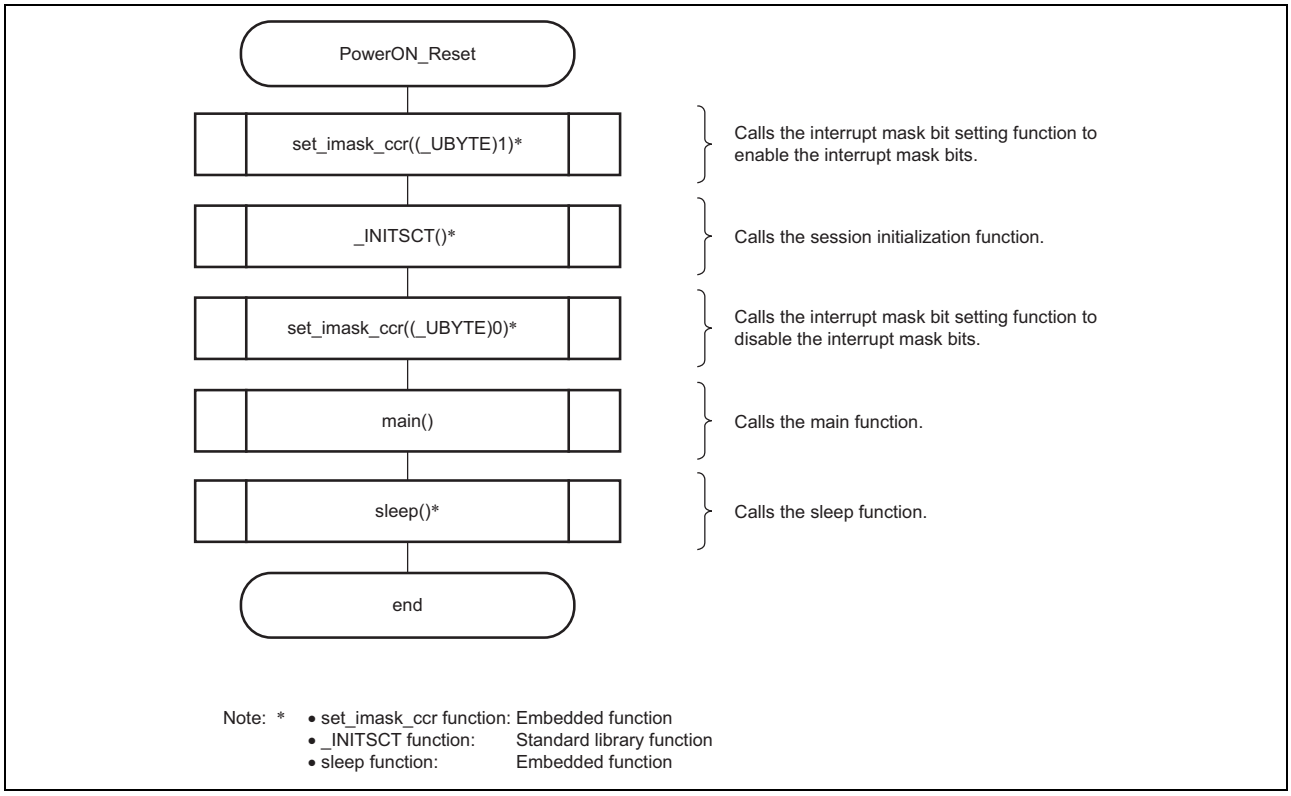

Figure 6 Flowchart (PowerON_Reset)

5.2.2 main Function

(1) Function overview

The main function calls the init_CPU and init_TMR functions.

(2) Arguments

None

(3) Returned value

None

(4) Description of internal I/O registers used

None

(5) Flowchart

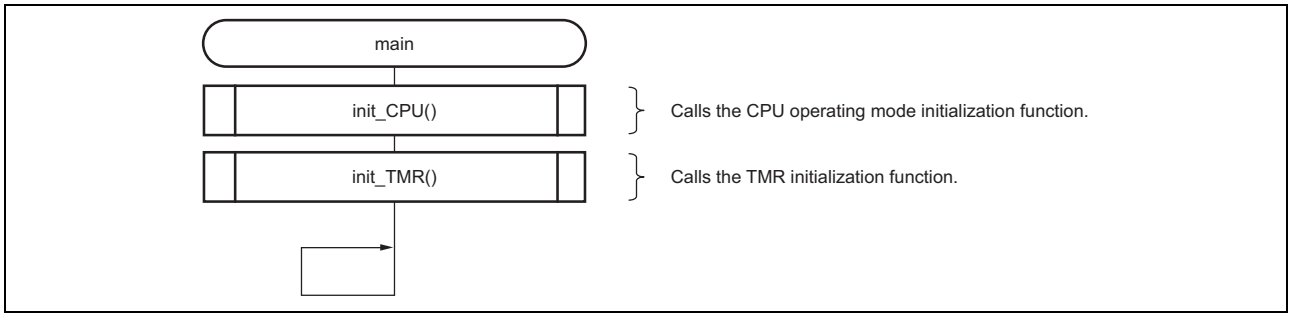

Figure 7 Flowchart (main)

5.2.3 init_CPU Function

(1) Function overview

The init_CPU function initializes the system cock settings and the pulse output port.

(2) Arguments

None

(3) Returned value

None

(4) Description of internal I/O registers used

This function uses the internal registers shown below.

Note that the set values shown here are for use in this application note and are not initial values.

- Standby Control Register (SBYCR) - Number of bits: 8 bits, Address: H'FFFF84

Bit	Bit Name	Set Value	R/W	Descriptions
2	SCK2	0	R/W	System Clock Select 2 to 0
1	SCK1	0	R/W	Select a clock for the bus master in high-speed mode or medium-speed mode.
0	SCK0	0	R/W	000: High-speed mode 001: Medium-speed clock: φ/2 010: Medium-speed clock: φ/4 011: Medium-speed clock: φ/8 100: Medium-speed clock: φ/16 101: Medium-speed clock: φ/32 11x: Must not be set.

- Mode Control Register (MDCR) - Number of bits: 8 bits, Address: H'FFFFC5

Bit	Bit Name	Set Value	R/W	Descriptions
7	EXPE	0	R/W	Extended Mode Enable Specifies extended mode. 0: Single-chip mode 1: Extended mode

- Port A Data Direction Register (PADDR) - Number of bits: 8 bits, Address: H'FFFFAB

Bit	Bit Name	Set Value	R/W	Descriptions
0	PA0DDR	1	W	When set to 1, the corresponding pins function as output port pins; when cleared to 0, function as input port pins. As the address of this register is the same as that of Port A Input Data Register (PAPIN), reading from this register indicates the state of port A.

- Port A Output Data Register (PAODR) - Number of bits: 8 bits, Address: H'FFFFAA

Bit	Bit Name	Set Value	R/W	Descriptions
0	PA0ODR	1	R/W	PAODR stores output data for the port A pins that are used as the general output port.

(5) Flowchart

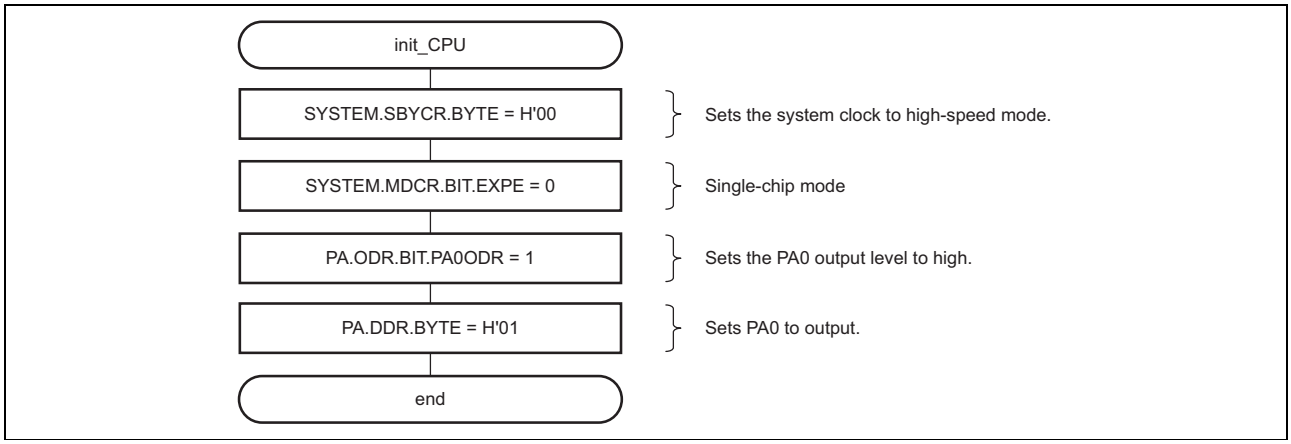

Figure 8 Flowchart (init_CPU)

5.2.4 init_TMR Function

(1) Function overview

The init_TMR function Initializes the TMR module.

(2) Arguments

None

(3) Returned value

None

(4) Description of internal I/O registers used

This function uses the internal registers shown below.

Note that the set values shown here are for use in this application note and are not initial values.

- Module Stop Control Register H (MSTPCRH) - Number of bits: 8 bits, Address: H'FFFF86

Bit	Bit Name	Set Value	R/W	Descriptions
4	MSTP12	0	R/W	8-bit timer (TMR_0 and TMR_1) 1: The module switches to module stop mode at the point the bus cycle completes. 0: Module stop mode is cleared and operation restarts at the point the bus cycle completes.

- Serial Timer Control Register (STCR) - Number of bits: 8 bits, Address: H'FFFFC3

Bit	Bit Name	Set Value	R/W	Descriptions
1	ICKS1	0	R/W	Internal Clock Source Select 1, 0
0	ICKS0	1	R/W	These bits select a clock to be input to the timer counter TCNT and a count condition together with bits CKS2 to CKS0 in the timer control register TCR.

- Timer Control/Status Register_0 (TCSR_0) - Number of bits: 8 bits, Address: H'FFFFCA

Bit	Bit Name	Set Value	R/W	Descriptions
7	CMFB	0	R/(W)*	Compare-Match Flag B [Setting condition] When the values of TCNT_0 and TCORB_0 match [Clearing condition] Read CMFB when CMFB = 1, then write 0 in CMFB
6	CMFA	0	R/(W)*	Compare-Match Flag A [Setting condition] When the values of TCNT_0 and TCORA_0 match [Clearing condition] Read CMFA when CMFA = 1, then write 0 in CMFA
5	OVF	0	R/(W)*	Timer Overflow Flag [Setting condition] When TCNT_0 overflows from H'FF to H'00 [Clearing condition] Read OVF when OVF = 1, then write 0 in OVF
4	ADTE	1	R/W	A/D Trigger Enable Selects whether the A/D conversion start request on compare match A is enabled or disabled. 0: A/D conversion start request is disabled 1: A/D conversion start request is enabled

Note: * Only 0 can be written to clear the flag.

- Time Constant Register A_0 (TCORA_0) - Number of bits: 8 bits, Address: H'FFFFCC

Bit	Bit Name	Set Value	R/W	Descriptions
7 to 0	—	H'64	R/W	TCORA is an 8-bit readable/writable register. TCORA_0 and TCORA_1 comprise a single 16-bit register, so they can be accessed together by word access. TCORA is continually compared with the value in TCNT. When a match is detected, the corresponding compare-match flag A (CMFA) in TCSR is set to 1. However, comparison is disabled during the T2 state of a TCORA write cycle. TCORA is initialized to H'FF.

- Time Constant Register B_0 (TCORB_0) - Number of bits: 8 bits, Address: H'FFFFCE

Bit	Bit Name	Set Value	R/W	Descriptions
7 to 0	—	H'32	R/W	TCORB is an 8-bit readable/writable register. TCORB_0 and TCORB_ 1 comprise a single 16-bit register, so they can be accessed together by word access. TCORB is continually compared with the value in TCNT. When a match is detected, the corresponding compare-match flag B (CMFB) in TCSR is set to 1. However, comparison is disabled during the T2 state of a TCORB write cycle. TCORB is initialized to H'FF.

- Timer Counter_0 (TCNT_0) - Number of bits: 8 bits, Address: H'FFFFD0

Bit	Bit Name	Set Value	R/W	Descriptions
7 to 0	—	H'00	R/W	Each TCNT is an 8-bit readable/writable up-counter. TCNT_0 and TCNT_1 comprise a single 16-bit register, so they can be accessed together by word access. The clock source is selected by the CKS2 to CKS0 bits in TCR. TCNT can be cleared by a compare-match A signal or compare-match B signal. The method of clearing can be selected by the CCLR1 and CCLR0 bits in TCR. When TCNT overflows (changes from H'FF to H'00), the OVF bit in TCSR is set to 1. TCNT is initialized to H'00.

- Timer Control Register_0 (TCR_0) - Number of bits: 8 bits, Address: H'FFFFC8

Bit	Bit Name	Set Value	R/W	Descriptions
7	CMIEB	1	R/W	Compare-Match Interrupt Enable B Selects whether the CMFB interrupt request (CMIB) is enabled or disabled when the CMFB flag in TCSR is set to 1. 0: CMFB interrupt request (CMIB) is disabled 1: CMFB interrupt request (CMIB) is enabled
6	CMIEA	1	R/W	Compare-Match Interrupt Enable A Selects whether the CMFA interrupt request (CMIA) is enabled or disabled when the CMFA flag in TCSR is set to 1. 0: CMFA interrupt request (CMIA) is disabled 1: CMFA interrupt request (CMIA) is enabled
4	CCLR1	0	R/W	Counter Clear 1 and 0
3	CCLR0	1	R/W	Specify the clearing conditions of TCNT. 00: Counter clear is disabled 01: Counter clear is enabled on compare-match A 10: Counter clear is enabled on compare-match B 11: Setting prohibited
2	CKS2	0	R/W	Clock Select 2 to 0
1	CKS1	1	R/W	Select the clock input to TCNT and count condition, together with the ICKS1 and ICKS0 bits in STCR.
0	CKS0	0`	R/W	

(5) Flowchart

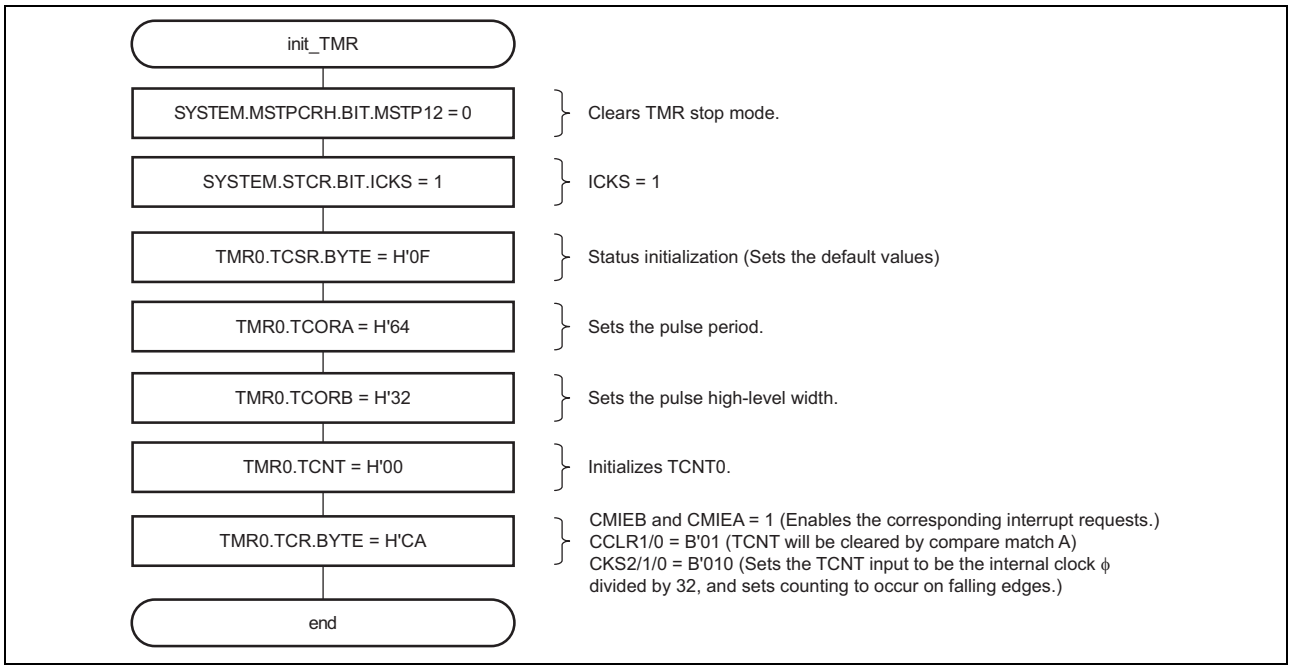

Figure 9 Flowchart (init_TMR)

5.2.5 INT_TMR_CMIA0 Function

(1) Function overview

The INT_TMR_CMIA0 function clears the CMFA flag and sets the PA0 pin output level to high.

(2) Arguments

None

(3) Returned value

None

(4) Description of internal I/O registers used

This function uses the internal registers shown below.

Note that the set values shown here are for use in this application note and are not initial values.

- Timer Control/Status Register_0 (TCSR_0) - Number of bits: 8 bits, Address: H'FFFFCA

Bit	Bit Name	Set Value	R/W	Descriptions
6	CMFA	0	R/(W)*	Compare-Match Flag A [Setting condition] When the values of TCNT_0 and TCORA_0 match [Clearing condition] Read CMFA when CMFA = 1, then write 0 in CMFA

Note: * Only 0 can be written to clear the flag.

- Port A Output Data Register (PAODR) - Number of bits: 8 bits, Address: H'FFFFAA

Bit	Bit Name	Set Value	R/W	Descriptions
0	PA0ODR	1	R/W	Stores the output data for the pin, which is used as a general-purpose output port.

(5) Flowchart

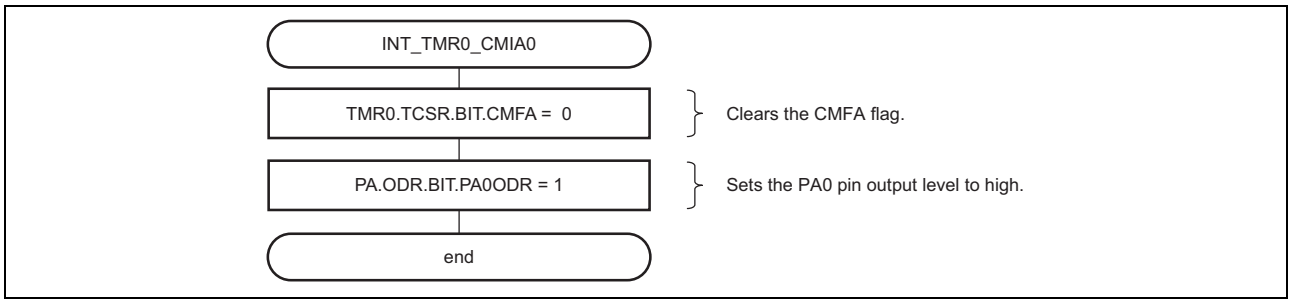

Figure 10 Flowchart (INT_TMR_CMIA0)

5.2.6 INT_TMR_CMIB0 Function

(1) Function overview

The INT_TMR_CMIB0 function clears the CMFB flag and sets the PA0 pin output level to low.

(2) Arguments

None

(3) Returned value

None

(4) Description of internal I/O registers used

This function uses the internal registers shown below.

Note that the set values shown here are for use in this application note and are not initial values.

- Timer Control/Status Register_0 (TCSR_0) - Number of bits: 8 bits, Address: H'FFFFCA

Bit	Bit Name	Set Value	R/W	Descriptions
7	CMFB	0	R/(W)*	Compare-Match Flag B [Setting condition] When the values of TCNT_0 and TCORB_0 match [Clearing condition] Read CMFB when CMFB = 1, then write 0 in CMFB

Note: * Only 0 can be written to clear the flag.

- Port A Output Data Register (PAODR) - Number of bits: 8 bits, Address: H'FFFFAA

Bit	Bit Name	Set Value	R/W	Descriptions
0	PA0ODR	0	R/W	Stores the output data for the pin, which is used as a general-purpose output port.

(5) Flowchart

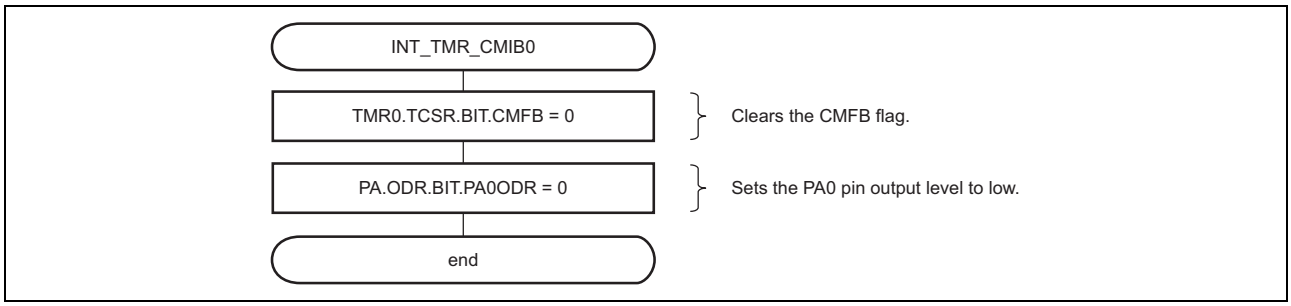

Figure 11 Flowchart (INT_TMR_CMIB0)

6. Reference Documents

- Hardware Manual
  H8S/2472, H8S/2463, H8S/2462 Group Hardware Manual
  (The latest version can be downloaded from the Renesas Technology Web site.)
- Development Environment Manual
  H8S/300, H8/300 Series C/C++ Compiler Package User's Manual
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