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H8S/2400 Series

Pulse Generation Example Using a 16-Bit Free-Running Timer (FRT)

Introduction

This Application Note presents a 16-bit free-running timer (FRT) based pulse generation sample application.

A continuous pulse signal with a fixed period can be generated by using the FRT compare match A and compare match B functions and I/O ports.

Target Devices

- H8S/2472, H8S/2463, H8S/2462 Group

Preface

This program can be used with other H8S Family MCUs that have the same internal I/O registers as the devices on which operation has been confirmed. Check the latest version of the manual for any additions and modifications to functions.

Careful evaluation is recommended before using this application note.

Contents

1. Specifications

This application note presents a program that uses the compare match A and B interrupts and port A0 (PA0) to generate a 10 kHz, 50% duty pulse signal.

Figure 1 presents an overview of the operation presented in this application note. The detailed specifications are as follows.

- The pulse period (100 μs) is set in the FRT output compare register A (OCRA) and the duty of 50% (50 μs) is set in output compare register B (OCRB).
- Compare match A is set as the clear condition for the free-running counter (FRC).
- The PA0 pin is set to the high-level output state in compare match A interrupt handling.
- The PA0 pin is set to the low-level output state in compare match B interrupt handling.

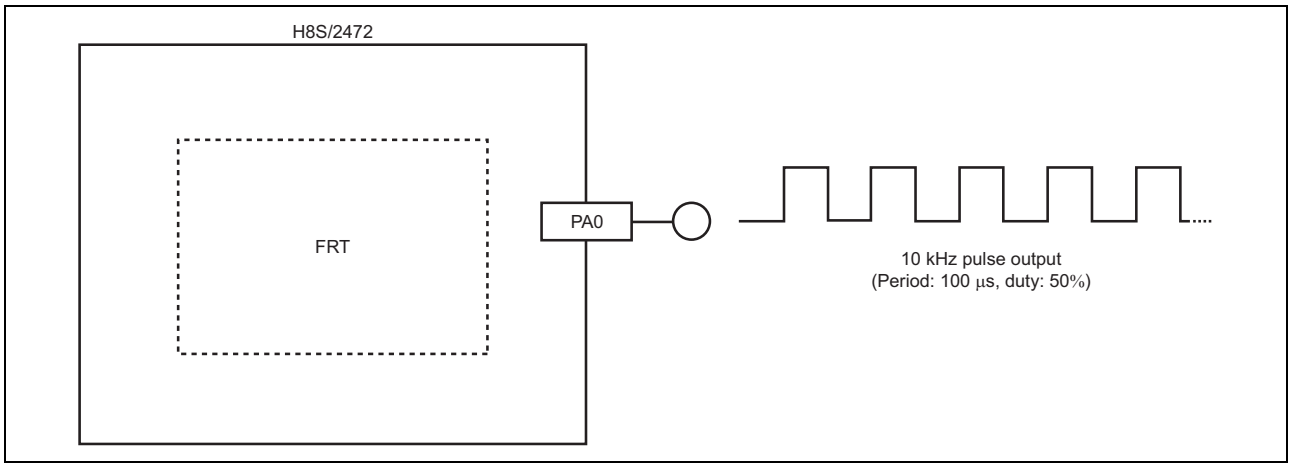

Figure 1 Operational Overview

2. Applicable Conditions

Table 1 Applicable Conditions

Item	Description
Operating frequency	Input clock: 8 MHz System clock (ϕ): 32 MHz (8.0 MHz multiplied by 4)
Operating voltage	3.3V
Operating mode	Mode 2 ($\overline{MD2}$ = 1, MD1 = 1)
Integrated Development environment	High-performance Embedded Workshop HEW Version 4.04.01.001
Evaluation board	Renesas Technology R0K402472D000BR
C/C++ compiler	Renesas Technology H8S, H8/300 C/C++ Compiler (V.6.02.01.000)
Compile options	-cpu=2600A:24 -optimize=0
Optimizing linkage editor	Renesas Technology Optimizing Linkage Editor (V.9.04.01.000)
Linker options	-start = PResetPRG,PIntPRG/0400, P,C$DSEC,C$BSEC,D/0800, B,R/0FF0800, S/0FF9600

3. Functions Used

3.1 FRC Count Timing

Figure 2 shows the FRC increment timing with an internal clock source.

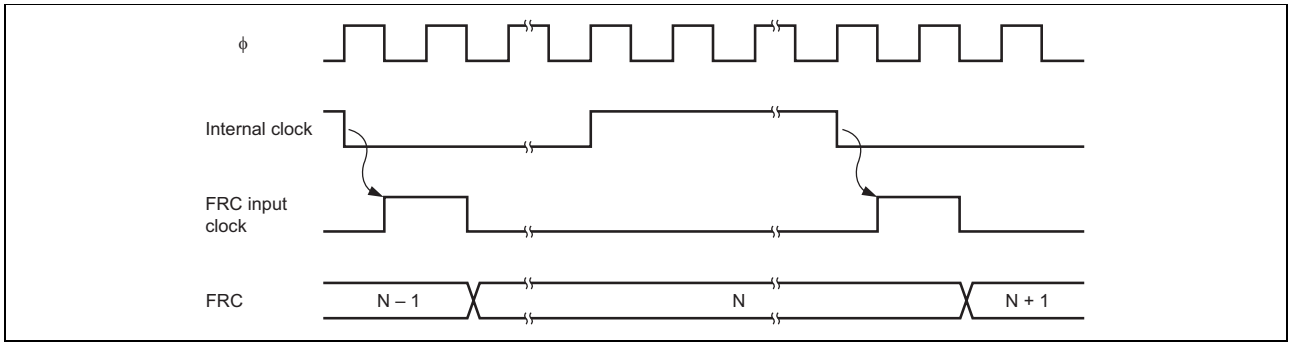

Figure 2 Increment Timing with Internal Clock Source

3.2 Output Compare Output Timing

A compare-match signal occurs at the last state when the FRC and OCR values match (at the timing when the FRC updates the counter value). Figure 3 shows the timing of this operation for compare-match A.

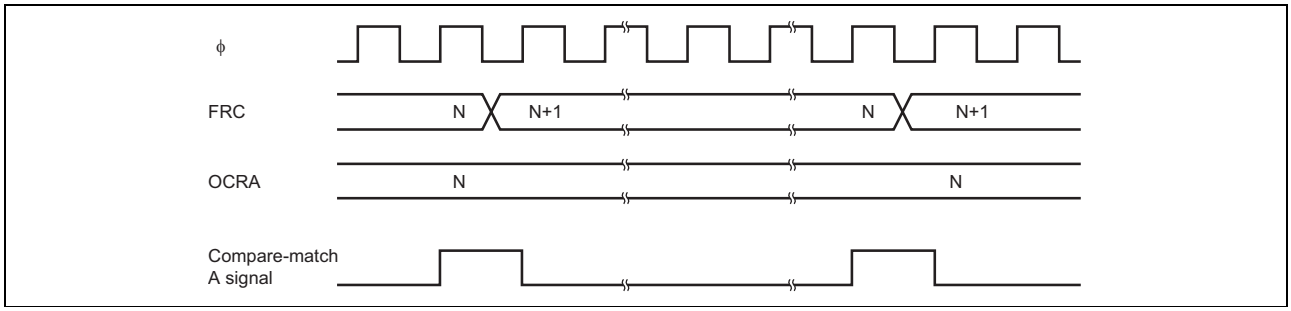

Figure 3 Timing of Output Compare A Output

3.3 FRC Clear Timing

FRC can be cleared when compare-match A occurs. Figure 4 shows the timing of this operation.

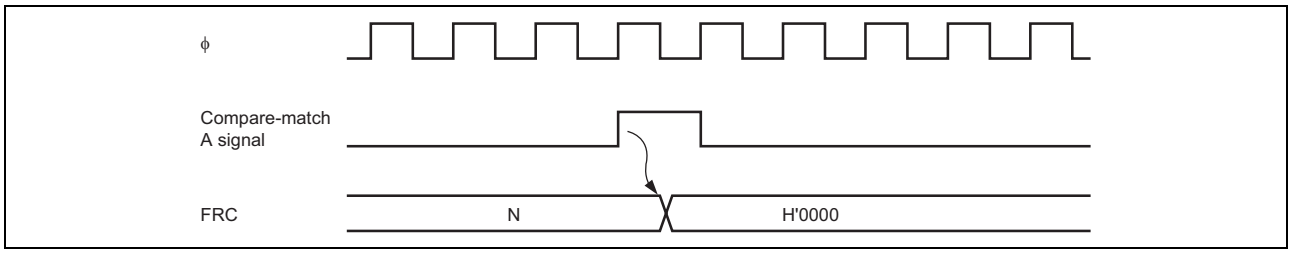

Figure 4 Clearing of FRC by Compare-Match A Signal

3.4 Timing of Output Compare Flag (OCF) Setting

The output compare flag, OCFA or OCFB, is set to 1 by a compare-match signal generated when the FRC value matches the OCRA or OCRB value. This compare-match signal is generated at the last state in which the two values match, just before FRC increments to a new value. When the FRC and OCRA or OCRB value match, the compare-match signal is not generated until the next cycle of the clock source. Figure 5 shows the timing of setting the OCFA or OCFB flag.

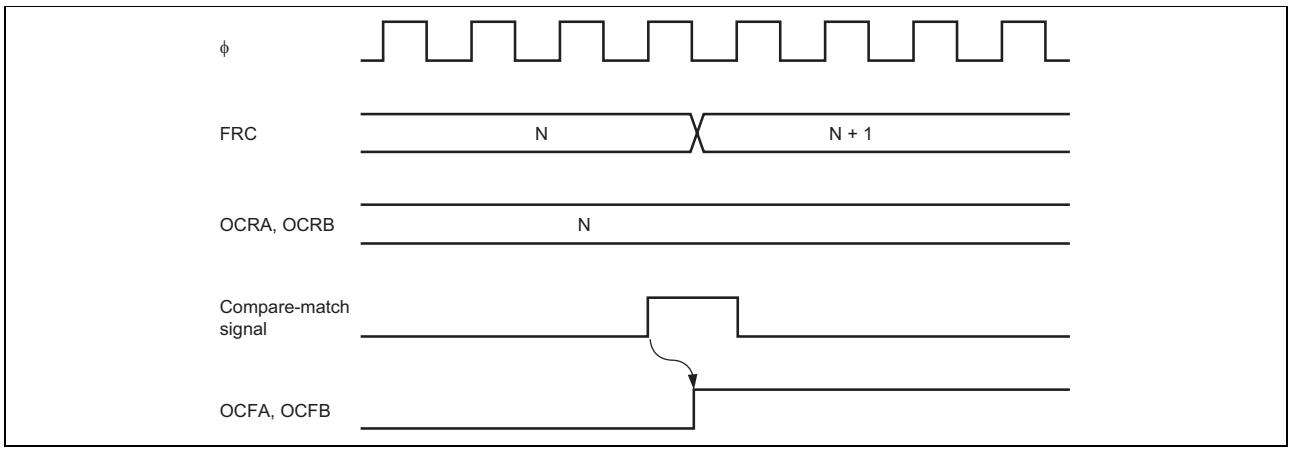

Figure 5 Timing of Output Compare Flag (OCFA or OCFB) Setting

4. Operation

Figure 6 shows the FRT-based pulse generation function described in this application note.

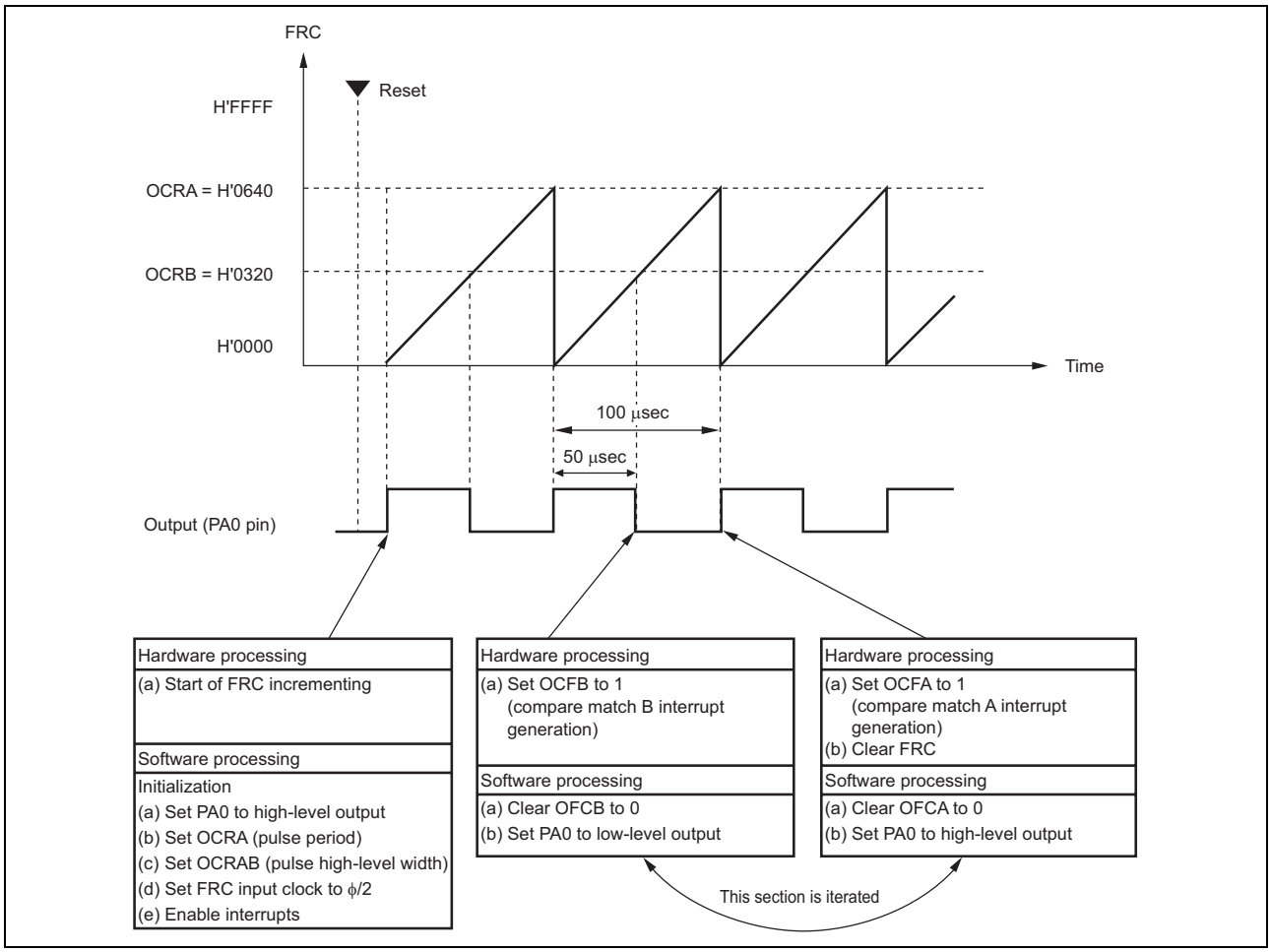

Figure 6 FRT Pulse Signal Generation

5. Software

5.1 Functions

Table 2 Functions

Function Name	Description
PowerON_Reset	• Initialization function Initializes the stack pointer (SP), sets interrupt mask bits, sets up uninitialized and initialized data, and calls the main function.
main	• Main function Calls the init_CPU and init_FRT functions.
init_CPU	• I/O register initialization function Initializes each of the registers.
init_FRT	• FRT initialization function Sets up FRT operation and starts that operation.
INT_FRT_OCIA	• Output compare interrupt A function Sets the PA0 pin output level to high (pulse period management)
INT_FRT_OCIB	• Output compare interrupt B function Sets the PA0 pin output level to low (duty management)

5.1.1 PowerON_Reset Function

(1) Function overview

The PowerON_Reset function initializes the stack pointer (SP), prepares the embedded functions and standard library functions, sets the interrupt mask bits, and sets up the uninitialized and initialized data. Then it calls the main function.

(2) Arguments

None

(3) Returned value

None

(4) Description of internal I/O registers used

None

(5) Flowchart

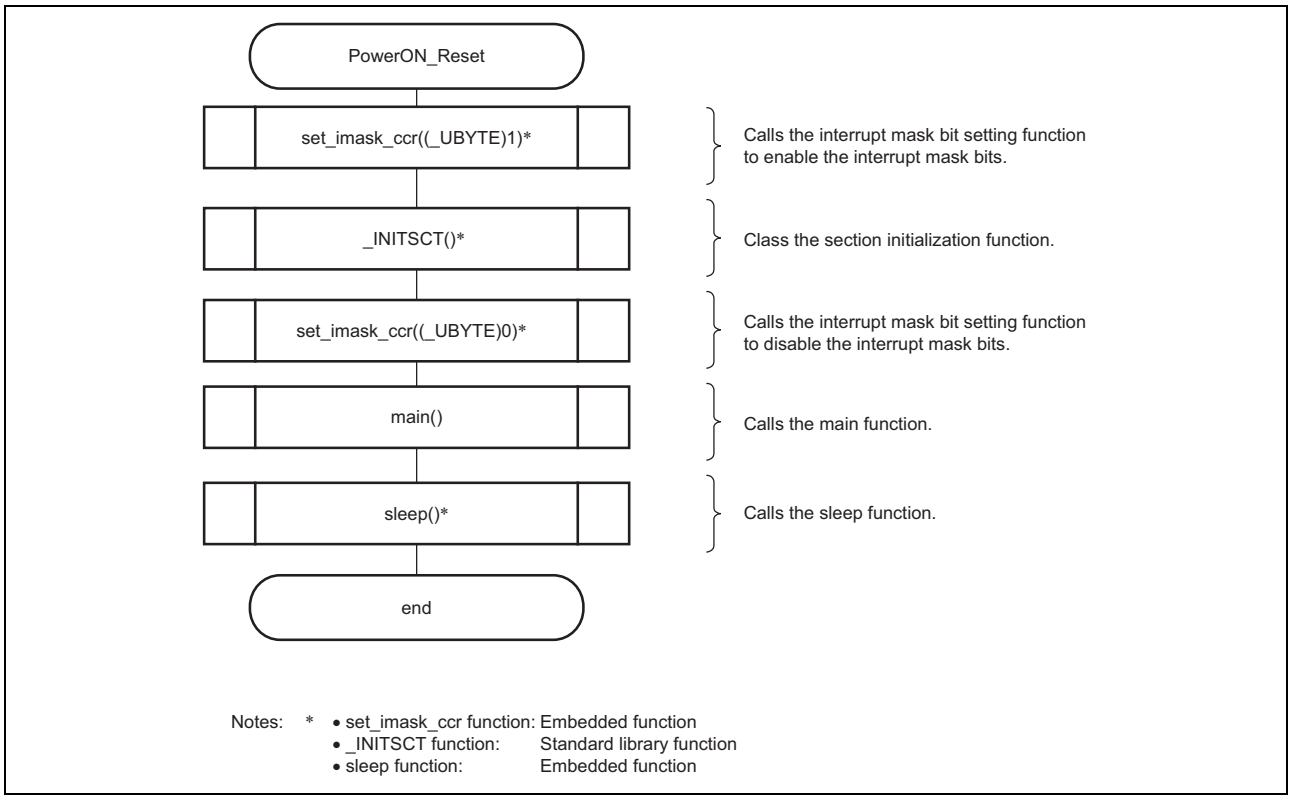

Figure 7 Flowchart (PowerON_Reset)

5.1.2 main Function

(1) Function overview

The main function calls the init_CPU and init_FRT functions.

(2) Arguments

None

(3) Returned value

None

(4) Description of internal I/O registers used

None

(5) Flowchart

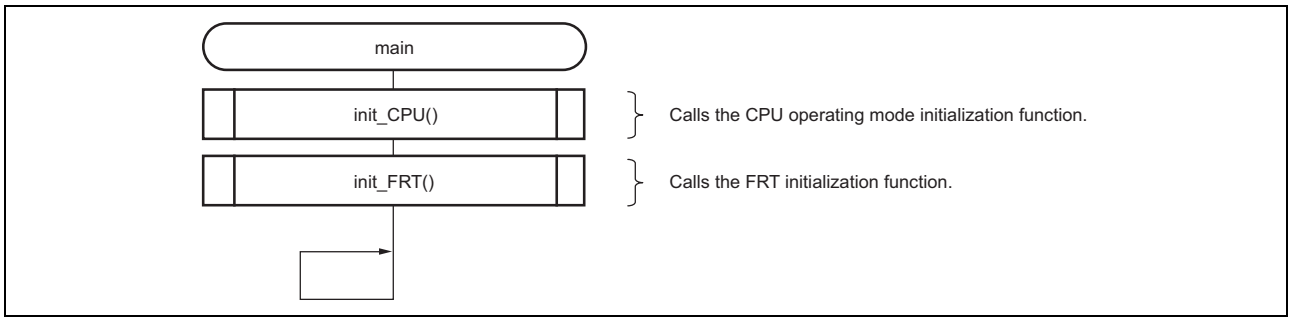

Figure 8 Flowchart (main)

5.1.3 init_CPU Function

(1) Function overview

The init_CPU function initializes the system cock settings and the pulse output port (PA0).

(2) Arguments

None

(3) Returned value

None

(4) Description of internal I/O registers used

This function uses the internal registers shown below.

Note that the set values shown here are for use in this application note and are not initial values.

- Standby Control Register (SBYCR) - Number of bits: 8, Address: H'FFFF84

Bit	Bit Name	Set Value	R/W	Descriptions
2	SCK2	0	R/W	System Clock Select 2 to 0
1	SCK1	0	R/W	Select a clock for the bus master in high-speed mode or medium-speed mode.
0	SCK0	0	R/W	000: High-speed mode (Initial value) 001: Medium-speed clock: ϕ/2 010: Medium-speed clock: ϕ/4 011: Medium-speed clock: ϕ/8 100: Medium-speed clock: ϕ/16 101: Medium-speed clock: ϕ/32 11x: Must not be set.

Legend:
x: Don't care

- Mode Control Register (MDCR) - Number of bits: 8, Address: H'FFFFC5

Bit	Bit Name	Set Value	R/W	Descriptions
7	EXPE	0	R/W	Extended Mode Enable Specifies extended mode. 0: Single-chip mode 1: Extended mode

- Port A Output Data Register (PAODR) - Number of bits: 8, Address: H'FFFFAA

Bit	Bit Name	Set Value	R/W	Descriptions
0	PA0ODR	1	R/W	PAODR stores output data for the port A pins that are used as the general output port.

- Port A Data Direction Register (PADDR) - Number of bits: 8, Address: H'FFFFAB

Bit	Bit Name	Set Value	R/W	Descriptions
0	PA0DDR	1	W	When set to 1, the corresponding pins function as output port pins; when cleared to 0, function as input port pins. As the address of this register is the same as that of Port A Input Data Register (PAPIN), reading from this register indicates the state of port A.

(5) Flowchart

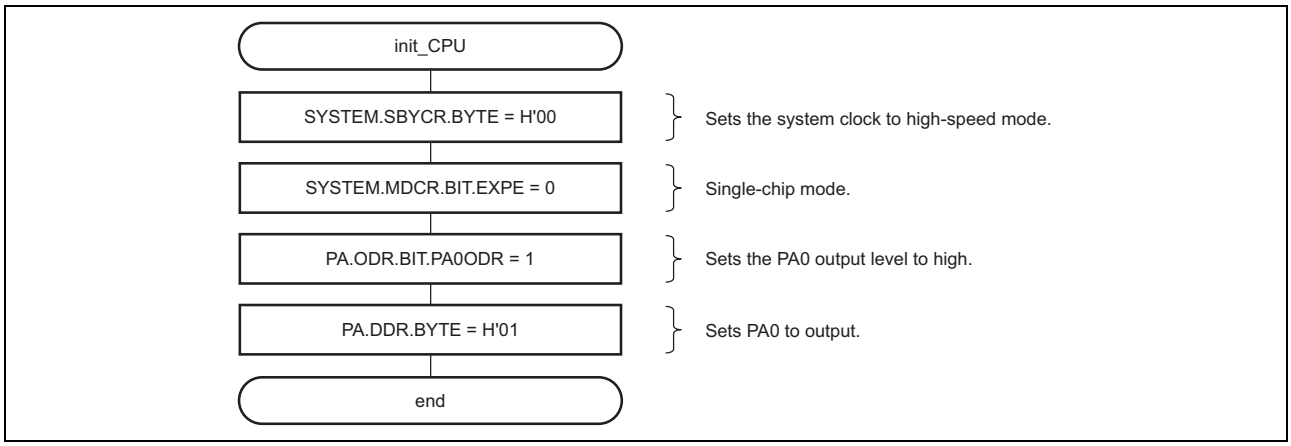

Figure 9 Flowchart (init_CPU)

5.1.4 init_FRT Function

(1) Function overview

The init_FRT function Initializes the FRT.

(2) Arguments

None

(3) Returned value

None

(4) Description of internal I/O registers used

This function uses the internal registers shown below.

Note that the set values shown here are for use in this application note and are not initial values.

- Module Stop Control Register H (MSTPCRH) - Number of bits: 8 bits, Address: H'FFFF86

Bit	Bit Name	Set Value	R/W	Descriptions
5	MSTP13	0	R/W	16-bit free-running timer (FRT) 1: The module switches to module stop mode at the point the bus cycle completes. 0: Module stop mode is cleared and operation restarts at the point the bus cycle completes.

- Timer Control/Status Register (TCSR) - Number of bits: 8 bits, Address: H'FFFF91

Bit	Bit Name	Set Value	R/W	Descriptions
3	OCFA	0	R/(W)*	Output Compare Flag A Indicates that the FRC value matches the OCRA value. [Setting condition] When FRC = OCRA [Clearing condition] Read OCFA when OCFA = 1, then write 0 to OCFA
2	OCFB	0	R/(W)*	Output Compare Flag B Indicates that the FRC value matches the OCRB value. [Setting condition] When FRC = OCRB [Clearing condition] Read OCFB when OCFB = 1, then write 0 to OCFB
1	OVF	0	R/(W)*	Overflow Flag Indicates that the FRC has overflowed. [Setting condition] When FRC overflows (changes from H'FFFF to H'0000) [Clearing condition] Read OVF when OVF = 1, then write 0 to OVF
0	CCLRA	1	R/W	Counter Clear A Selects whether the FRC is to be cleared on compare-match A (when the FRC and OCRA values match). 0: FRC clearing is disabled 1: FRC is cleared on compare-match A

Note: * Only 0 can be written to clear the flag.

- Timer Control Register (TCR) - Number of bits: 8 bits, Address: H'FFFF96

Bit	Bit Name	Set Value	R/W	Descriptions
1	CKS1	0	R/W	Clock Select 1 and 0
0	CKS0	0	R/W	Select clock source for FRC. 00: ϕ/2 internal clock source 01: ϕ/8 internal clock source 10: ϕ/32 internal clock source 11: Reserved

- Timer Output Compare Control Register (TOCR) - Number of bits: 8 bits, Address: H'FFFF97

Bit	Bit Name	Set Value	R/W	Descriptions
4	OCRS	0/1	R/W	Output Compare Register Select OCRA and OCRB share the same address. When this address is accessed, the OCRS bit selects which register is accessed. The operation of OCRA or OCRB is not affected. 0: OCRA is selected 1: OCRB is selected

- Output Compare Register A (OCRA) - Number of bits: 16 bits, Address: H'FFFF94

Bit	Bit Name	Set Value	R/W	Descriptions
15 to 0	—	H'0640	R/W	OCRA is a 16-bit read/write register. The value in OCRA is continuously compared to the FRC value. When the two values match (a compare match), the OCFA flag in TCSR is set to 1. OCRA should always be accessed in 16-bit units: it cannot be accessed in 8-bit units.

Note: OCRA and OCRAB have the same address. The OCRS bit in TOCR is used for switching between these registers.

- Output Compare Register B (OCRB) - Number of bits: 16 bits, Address: H'FFFF94

Bit	Bit Name	Set Value	R/W	Descriptions
15 to 0	—	H'0320	R/W	OCRB is a 16-bit read/write register. The value in OCRB is continuously compared to the FRC value. When the two values match (a compare match), the OCFB flag in TCSR is set to 1. OCRB should always be accessed in 16-bit units: it cannot be accessed in 8-bit units.

Note: OCRA and OCRAB have the same address. The OCRS bit in TOCR is used for switching between these registers.

- Free-Running Counter (FRC) - Number of bits: 16 bits, Address: H'FFFF92

Bit	Bit Name	Set Value	R/W	Descriptions
15 to 0	—	H'0000	R/W	FRC is a 16-bit read/write increment-only counter. The input clock is selected by the CKS1 and CKS0 bits in TCR. FRC can be cleared by compare match A. When FRC overflows from H'FFFF to H'0000, the OVF flag in TCR is set to 1. FRC should always be accessed in 16-bit units: it cannot be accessed in 8-bit units. FRC is initialized to H'0000.

- Timer Interrupt Enable Register (TIER) - Number of bits: 8 bits, Address: H'FFFF90

Bit	Bit Name	Set Value	R/W	Descriptions
3	OCIAE	1	R/W	Output Compare Interrupt A Enable Selects whether to enable output compare interrupt A request (OCIA) when output compare flag A (OCFA) in TCSR is set to 1. 0: OCIA requested by OCFA is disabled 1: OCIA requested by OCFA is enabled
2	OCIBE	1	R/W	Output Compare Interrupt B Enable Selects whether to enable output compare interrupt B request (OCIB) when output compare flag B (OCFB) in TCSR is set to 1. 0: OCIB requested by OCFB is disabled 1: OCIB requested by OCFB is enabled

(5) Flowchart

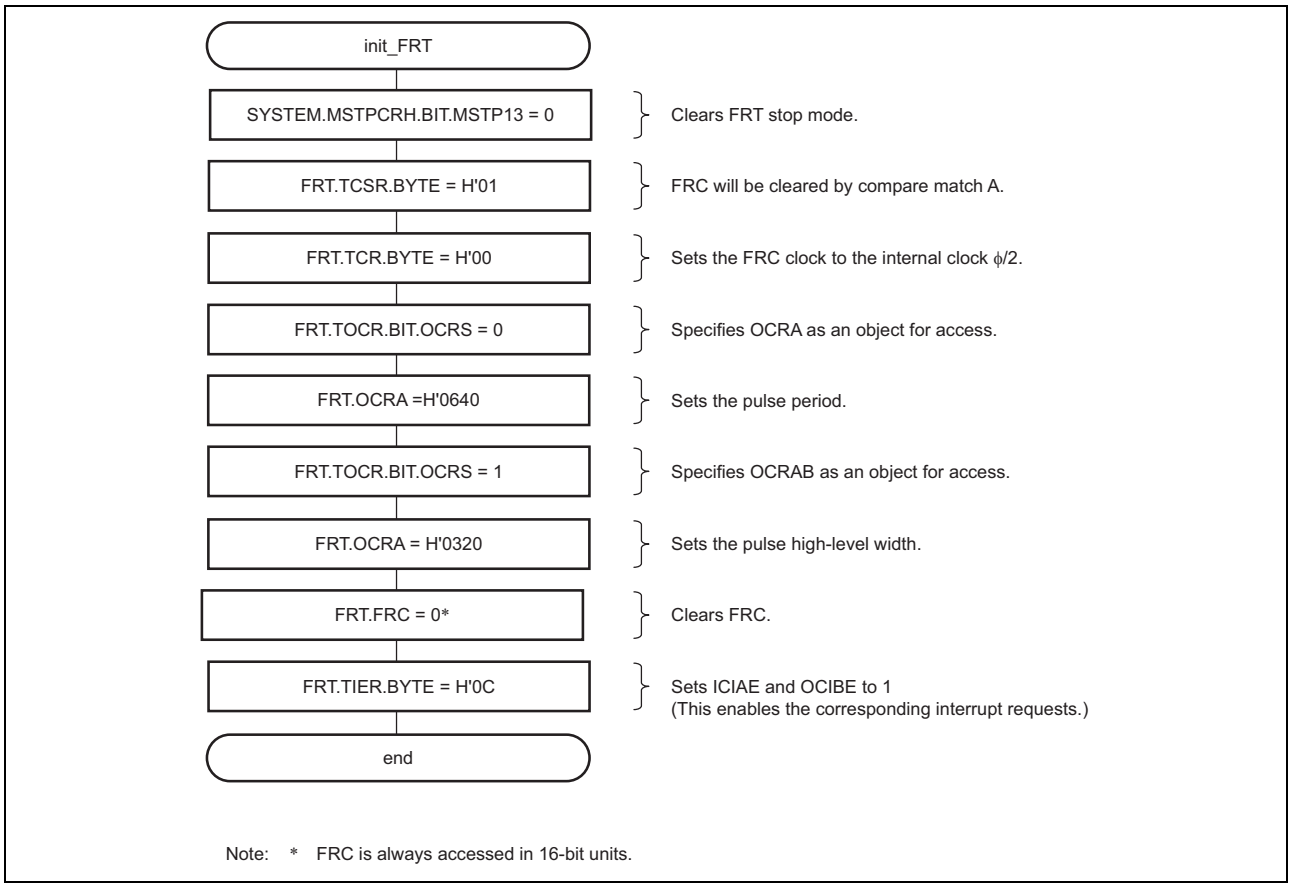

Figure 10 Flowchart (init_FRC)

5.1.5 INT_FRT_OCIA Function

(1) Function overview

The INT_FRT_OCIA function clears the OCFA flag and sets the PA0 pin output level to high.

(2) Arguments

None

(3) Returned value

None

(4) Description of internal I/O registers used

This function uses the internal registers shown below.

Note that the set values shown here are for use in this application note and are not initial values.

- Timer Control/Status Register (TCSR) - Number of bits: 8 bits, Address: H'FFFF91

Bit	Bit Name	Set Value	R/W	Descriptions
3	OCFA	0	R/(W)*	Output Compare Flag A Indicates that the FRC value matches the OCRA value. [Setting condition] When FRC = OCRA [Clearing condition] Read OCFA when OCFA = 1, then write 0 to OCFA

Note: * Only 0 can be written to clear the flag.

- Port A Output Data Register (PAODR) - Number of bits: 8 bits, Address: H'FFFFAA

Bit	Bit Name	Set Value	R/W	Descriptions
0	PA0ODR	1	R/W	Stores the output data for the pin, which is used as a general-purpose output port.

(5) Flowchart

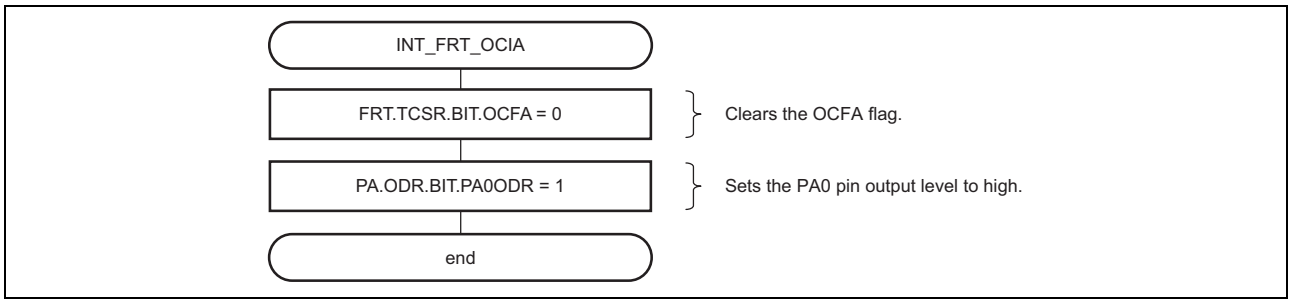

Figure 11 Flowchart (INT_FRT_OCIA)

5.1.6 INT_FRT_OCIB Function

(1) Function overview

The INT_FRT_OCIB function clears the OCFB flag and sets the PA0 pin output level to low.

(2) Arguments

None

(3) Returned value

None

(4) Description of internal I/O registers used

This function uses the internal registers shown below.

Note that the set values shown here are for use in this application note and are not initial values.

- Timer Control/Status Register (TCSR) - Number of bits: 8 bits, Address: H'FFFF91

Bit	Bit Name	Set Value	R/W	Descriptions
2	OCFB	0	R/(W)*	Output Compare Flag B Indicates that the FRC value matches the OCRB value. [Setting condition] When FRC = OCRB [Clearing condition] Read OCFB when OCFB = 1, then write 0 to OCFB

Note: * Only 0 can be written to clear the flag.

- Port A Output Data Register (PAODR) - Number of bits: 8 bits, Address: H'FFFFAA

Bit	Bit Name	Set Value	R/W	Descriptions
0	PA0ODR	0	R/W	Stores the output data for the pin, which is used as a general-purpose output port.

(5)Flowchart

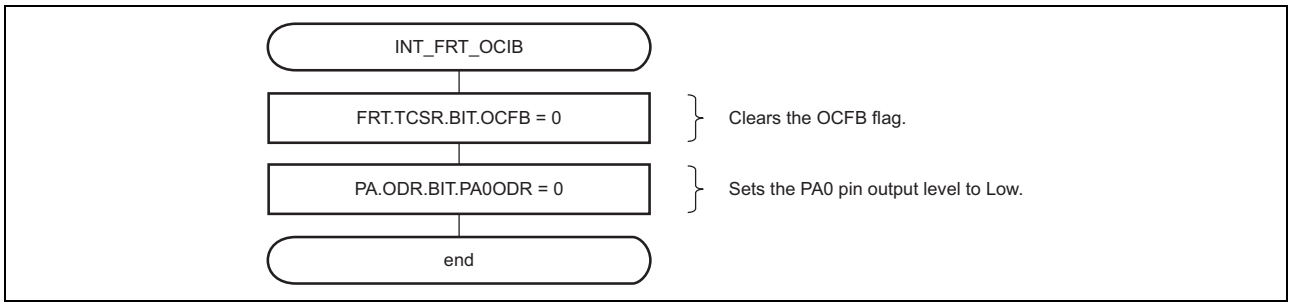

Figure 12 Flowchart (INT_FRT_OCIB)

6. Reference Documents

- Hardware Manual
  H8S/2472, H8S/2463, H8S/2462 Group Hardware Manual
  (The latest version can be downloaded from the Renesas Technology Web site.)
- Development Environment Manual
  H8S/300, H8/300 Series C/C++ Compiler Package User's Manual
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