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H8S/2400 Series

CRC Operation Circuit

Introduction

This application note covers using the CRC operation circuit to generate 2-byte CRC codes for 256-byte data blocks and using the generated CRC codes to perform error checking on data blocks.

By using the CRC operation circuit, the reliability of high-speed data transfer can be enhanced.

Target Devices

- H8S/2472, H8S/2463, H8S/2462 Group

Preface

This program can be used with other H8S Family MCUs that have the same internal I/O registers as the devices on which operation has been confirmed. Check the latest version of the manual for any additions and modifications to functions.

Careful evaluation is recommended before using this application note.

Contents

1. Specifications

The specifications of this application note cover using the CRC operation circuit to generate 2-byte CRC codes and using the CRC codes to perform error checking on data blocks.

The detailed specifications for the operations described in this application note are listed below.

- The polynomial expression used to generate the CRC is $X^{16} + X^{12} + X^5 + 1$.
- Each CRC calculation is performed on a block consisting of 256 bytes of data.
- The block consists of 256 bytes of sequential data as follows: H'00, H'01, H'02, …, H'FD, H'FE, H'FF.
- The CRC code is generated for LSB-first communication.
- This application note covers the CRC calculation processing only.

Figure 1 shows an overview of the operations described in this application note.

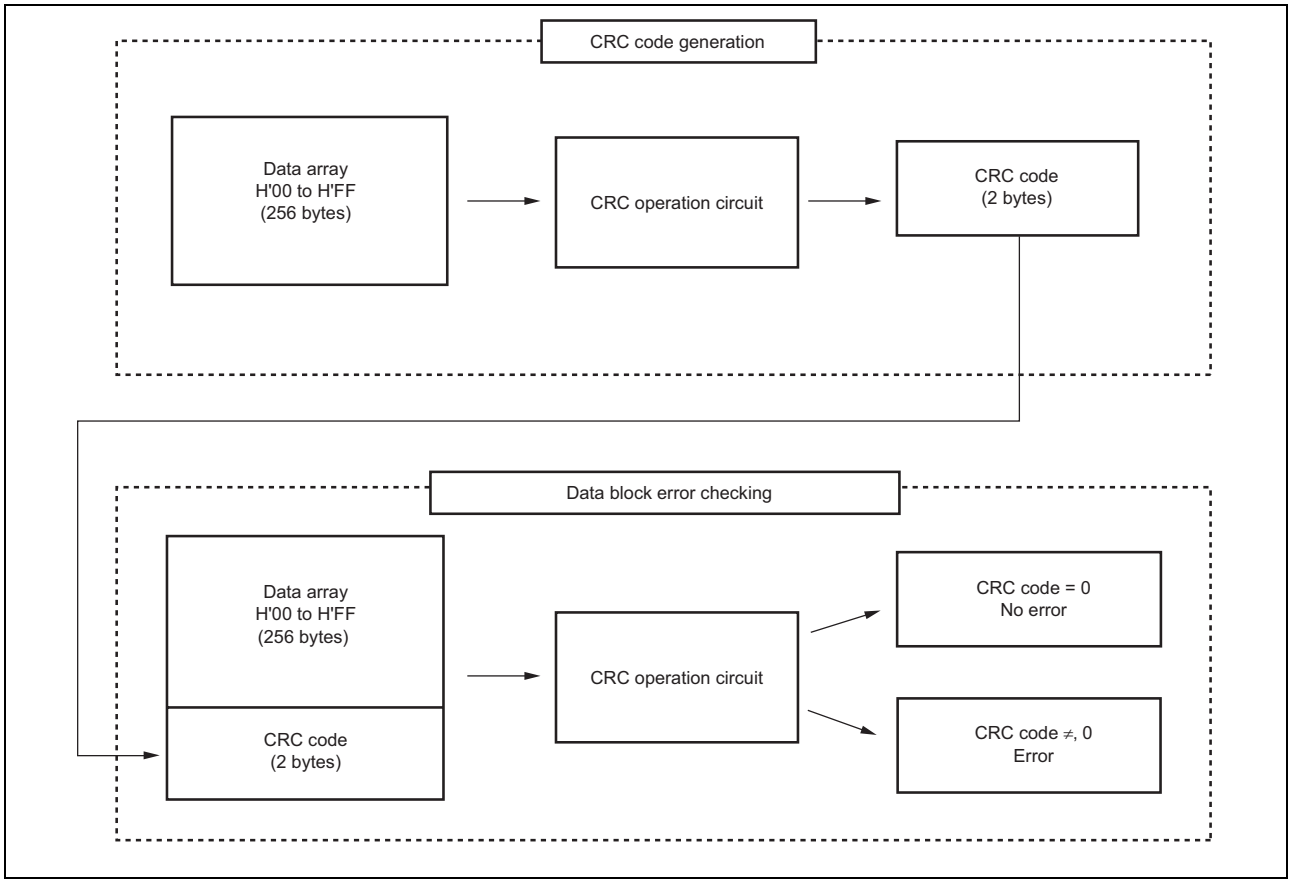

Figure 1 Operation Overview

2. Applicable Conditions

Table 1 Applicable Conditions

Item	Description
Operating frequency	Input clock: 8.0 MHz System clock (ϕ): 32 MHz (8.0 MHz multiplied by 4*)
Operating voltage	3.3V
Operating mode	Mode 2 ($\overline{MD2}$ = 1, MD1 = 1)
Evaluation board	Renesas Technology R0K402472D000BR
Integrated development environment	High-performance Embedded Workshop (HEW) Ver.4.04.01.001
C/C++ compiler	Renesas Technology H8S,H8/300 C/C++ Compiler (V.6.02.00)
Compile options	-cpu=2600A:24, -optimize = 1
Optimizing linkage editor	Renesas Technology Optimizing Linkage Editor (V9.03.00)
Linker options	start = PResetPRG,PIntPRG/0400, P,C,C$DSEC,C$BSEC,D/0800, B,R/0FF0800, S/0FFEE00

Note: * The PLL multiplier circuit multiplies the externally input clock by 4.

3. Functions Used

The CRC operation circuit can be used to detect errors in data blocks in order to assure the reliability of data transfer, such as high-speed transmission and reception operations.

The features of the CRC operation circuit are listed below.

- CRC code generated for any desired data length in an 8-bit unit
- CRC operation executed on eight bits in parallel
- One of three generating polynomials selectable
- CRC code generation for LSB-first or MSB-first communication selectable

Figure 2 is a block diagram of the CRC operation circuit.

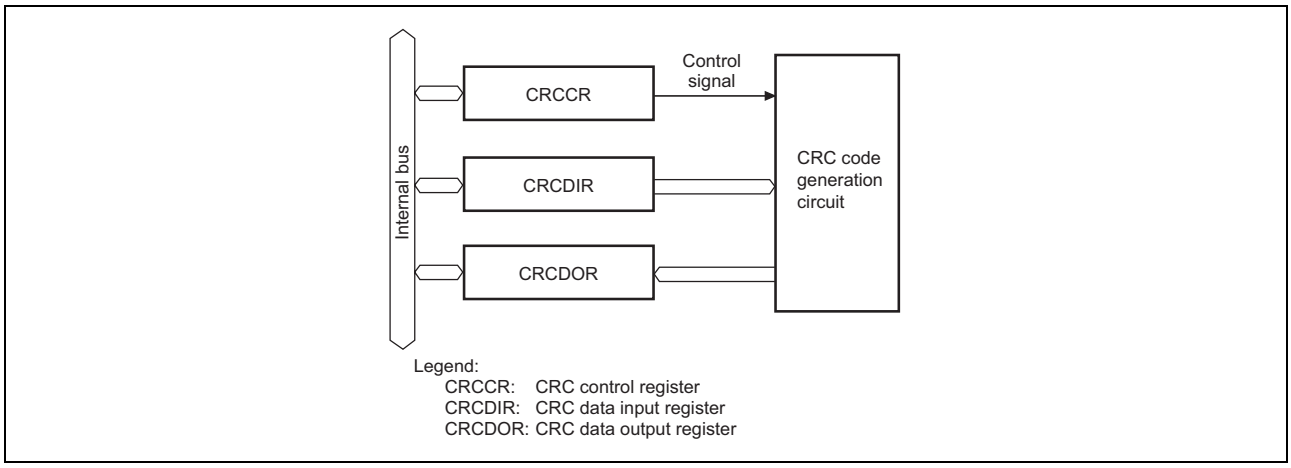

Figure 2 Block Diagram of CRC Operation Circuit

3.1 Note on CRC Operation Circuit

Note that the sequence to transmit the CRC code differs between LSB-first transmission and MSB-first transmission.

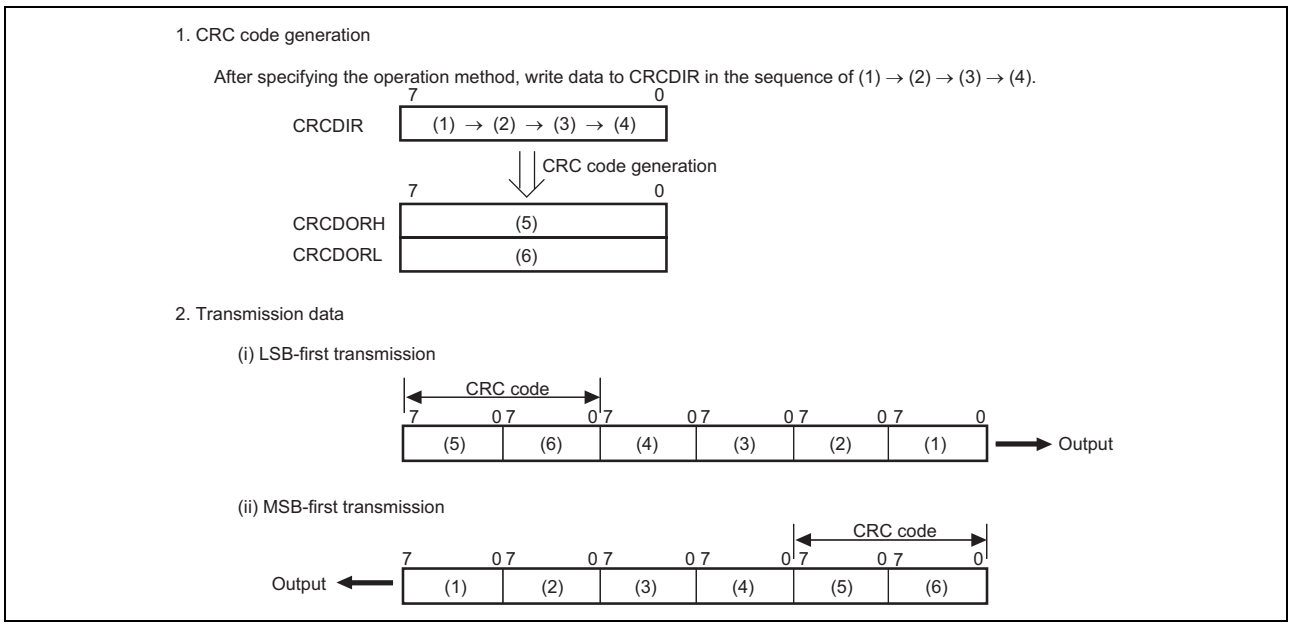

Figure 3 LSB-First and MSB-First Transmit Data

4. Operation

In the example shown below, a CRC code for LSB-first communication is generated for the hexadecimal data H'F0 using the polynomial expression $X^{16} + X^{12} + X^5 + 1$ and with bits G1 and G0 in CRCCR set to B'11.

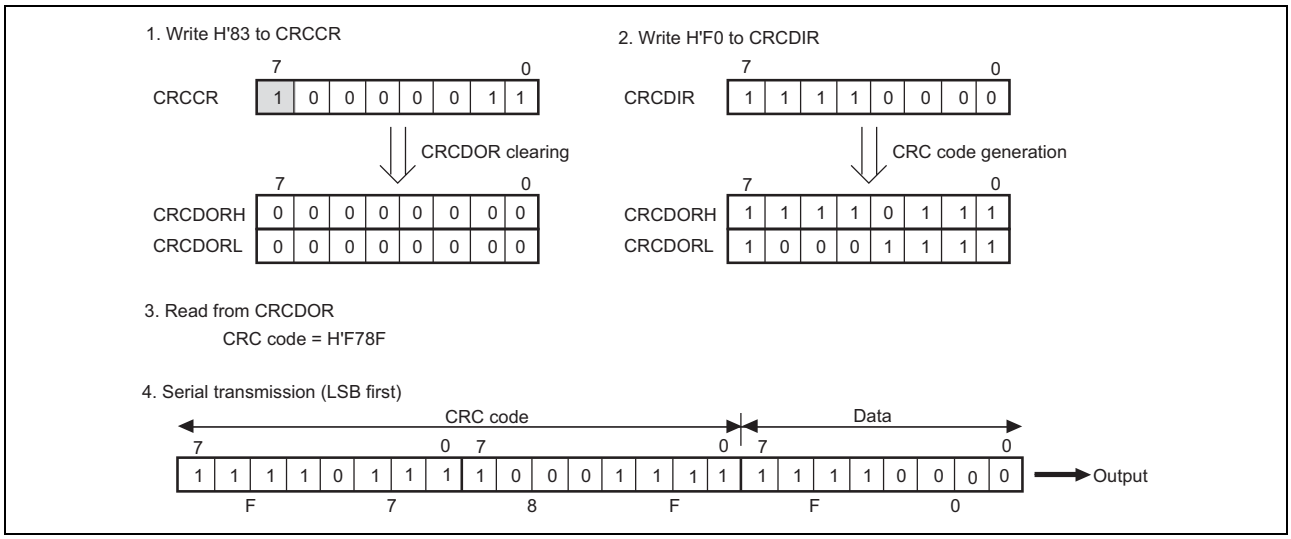

Figure 4 LSB-First Data Transmission

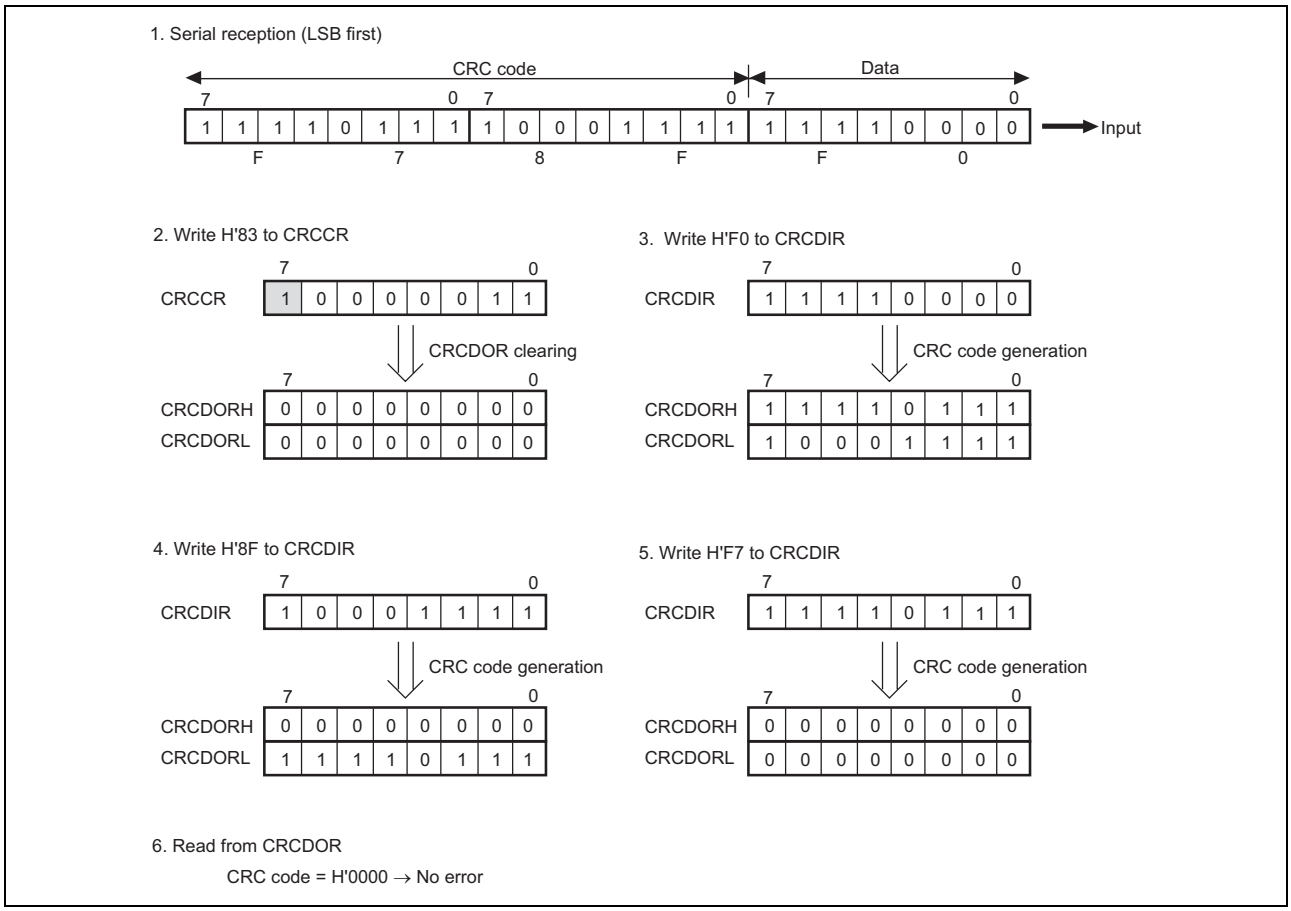

Figure 5 LSB-First Data Reception

5. Functions

5.1 Symbolic Constants

Table 3 List of Symbolic Constants

Constant Name	Set Value	Description	Used by Functions
MAX_CRC_DATA_CNT	256	Maximum number of data bytes for CRC calculation	init crc_code_generation mistake_detection

5.2 Unions

Table 4 List of Unions

Type	Union Name	Type	Variable Name	Type	Variable Name	No. of Bits	Description	Used by Function
union	uCODE	unsigned int	WORD	—	—	16	Word access variable	init crc_code_generation mistake_detection
		struct	BIT	unsigned char	H	8	CRC code upper bits	
				unsigned char	L	8	CRC code lower bits	

5.3 RAM Variables

Table 6 List of RAM Variables

Type	Variable Name	Set Value	Description	Used by Functions
union uCODE	crc_code	0	CRC code	init crc_code_generation mistake_detection
const unsigned char	crc_data [MAX_CRC_DATA_CNT]	0x00, 0x01, 0x02,…, …, 0xFD, 0xFE, 0xFF	Data for CRC calculation	init crc_code_generation mistake_detection

5.4 List of Functions

Table 7 List of Functions

Function Name	Description
PowerON_Reset	• Initial settings function Initializes status pointer (SP), sets interrupt mask bits, sets uninitialized/initialized data, calls main function.
main	• Main function Performs initialization, generates CRC code, detects errors.
init	• I/O register initialization function Initializes registers.
crc_code_generation	• CRC code generation function Generates a CRC code in LSB-first format.
mistake_detection	• Error detection function Detects errors in the data block.

5.5 Functions

5.5.1 PowerON_Reset Function

(1) Functional Overview

The PowerON_Reset function initializes the status pointer (SP) and uses embedded functions and standard library functions to set interrupt mask bits and set uninitialized/initialized data. Then it calls the main function.

(2) Arguments

None

(3) Returned values

None

(4) Description of internal I/O registers used

None

(5) Flowchart

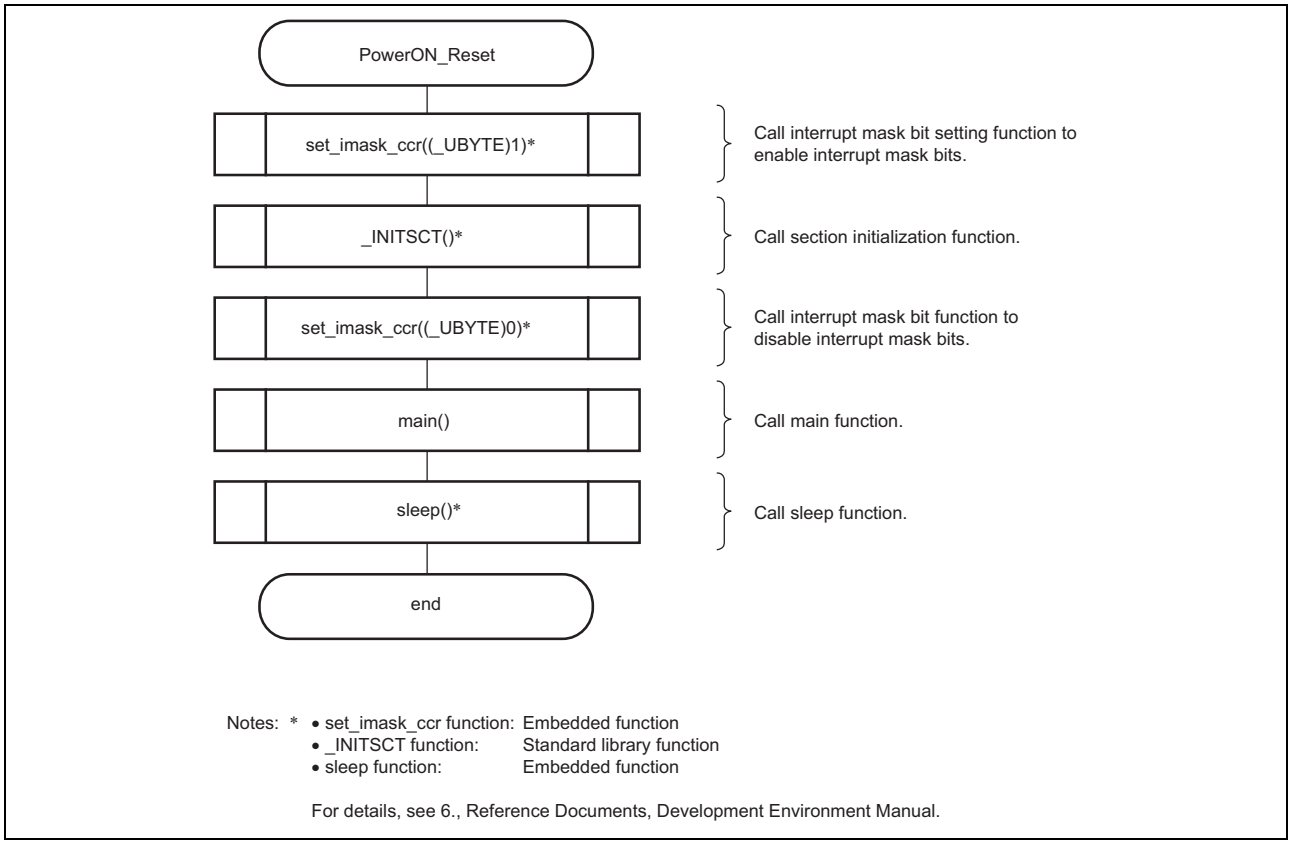

Figure 6 Flowchart (PowerON_Reset)

5.5.2 main Function

(1) Functional Overview

The main function initializes the registers, generates a CRC code, and performs error detection.

(2) Arguments

None

(3) Returned values

None

(4) Description of internal I/O registers used

None

(5) Flowchart

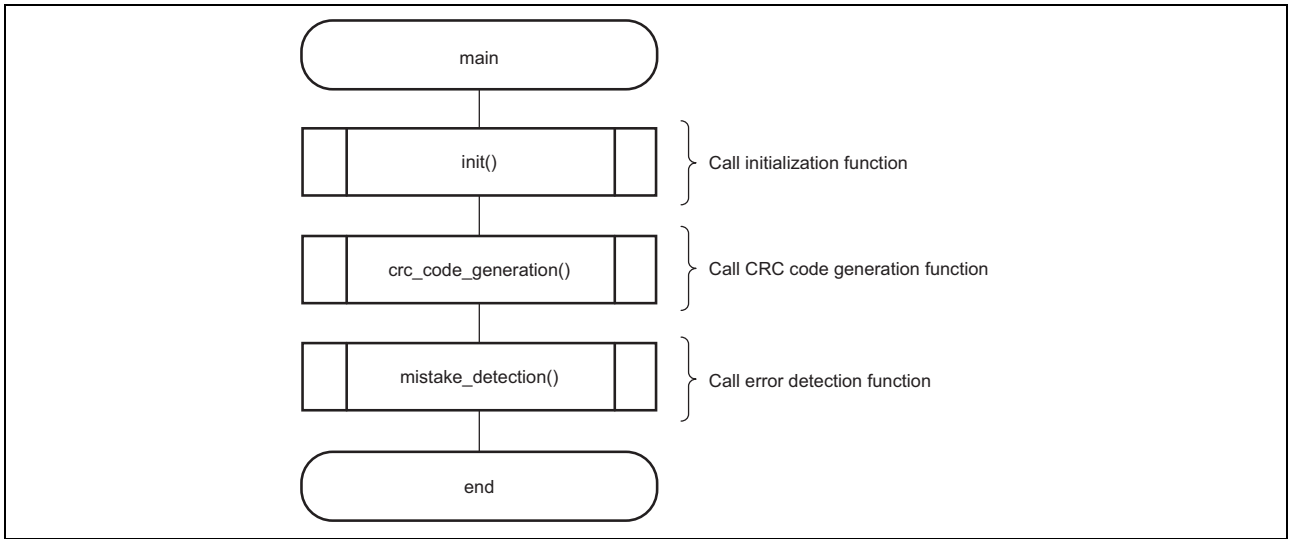

Figure 7 Main Flowchart (main)

5.5.3 init Function

(1) Functional Overview

The init function initializes the registers.

(2) Arguments

None

(3) Returned values

None

(4) Description of internal I/O registers used

The internal I/O registers used by this function are shown below. Note that the setting values shown are those used for this sample task and differ from the initial values.

- Mode Control Register (MDCR) - Number of bits: 8, Address: H'FFFFC5

Bit	Bit Name	Set Value	R/W	Descriptions
2	MDS2	—	R	Mode Select 2 and 1
1	MDS1	—	R	These bits indicate the input levels at mode pins ($\overline{MD2}$ and MD1) (the current operating mode). Bits MDS2 and MDS1 correspond to $\overline{MD2}$ and MD1, respectively. MDS2 and MDS1 are read-only bits and they cannot be written to. The mode pin ($\overline{MD2}$ and MD1) input levels are latched into these bits when MDCR is read. These latches are canceled by a reset.

- Standby Control Register (SBYCR) - Number of bits: 8, Address: H'FFFF84

Bit	Bit Name	Set Value	R/W	Descriptions
2	SCK2	0	R/W	System Clock Select 2 to 0
1	SCK1	0	R/W	Select a clock for the bus master in high-speed mode or medium-speed mode.
0	SCK0	0	R/W	000: High-speed mode

- SUBMSTPBL causes on-chip peripheral modules to shift to module stop mode in module units. Each module can be set to module stop mode by setting the corresponding bit to 1.
- Module Stop Control Register L (MSTPCRL) - Number of bits: 8, Address: H'FFFF87

Bit	Bit Name	Set Value	R/W	Descriptions
1	MSTP1	0	R/W	CRC operation circuit

- CRC Control Register (CRCCR) - Number of bits: 8, Address: H'FFFED4

Bit	Bit Name	Set Value	R/W	Descriptions
7	DORCLR	0	W	CRCDOR Clear Setting this bit to 1 clears CRCDOR to H'0000.
2	LMS	0	R/W	CRC Operation Switch Selects CRC code generation for LSB-first or MSB-first communication. 0: Performs CRC operation for LSB-first communication. The lower byte (bits 7 to 0) is first transmitted when CRCDOR contents (CRC code) are divided into two bytes to be transmitted in two parts.
1	G1	1	R/W	CRC Generating Polynomial Select
0	G0	1	R/W	These bits select the polynomial. 11: $X^{16} + X^{12} + X^5 + 1$

(5) Flowchart

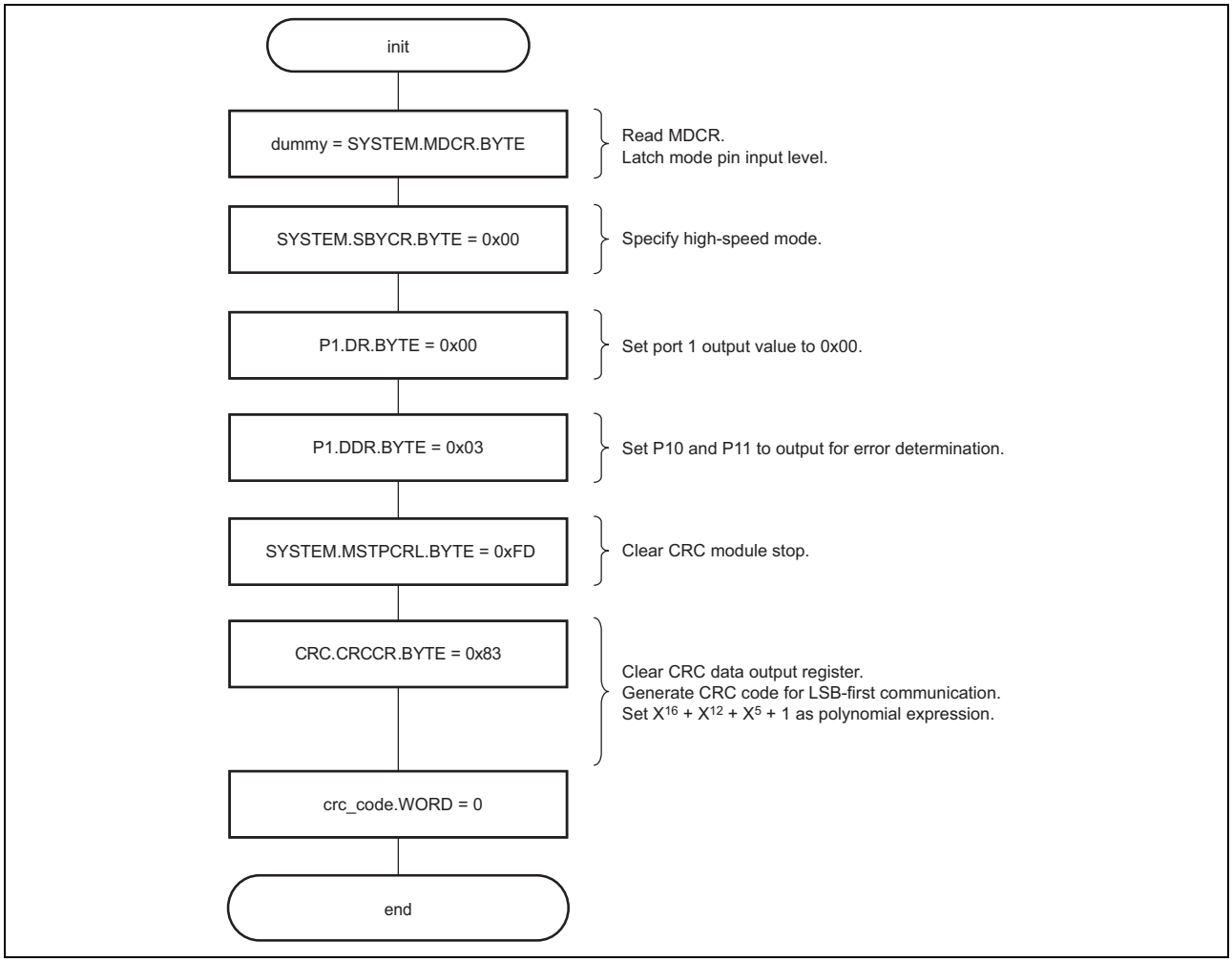

Figure 8 Initialization Flowchart (init)

5.5.4 crc_code_generation Function

(1) Functional Overview

The crc_code_generation function generates a CRC code in LSB-first format using the CRC operation circuit.

(2) Arguments

None

(3) Returned values

None

(4) Description of internal I/O registers used

The internal I/O registers used by this function are shown below. Note that the setting values shown are those used for this sample task and differ from the initial values.

- CRC Control Register (CRCCR) - Number of bits: 8, Address: H'FFFED4

Bit	Bit Name	Set Value	R/W	Descriptions
7	DORCLR	0	W	CRCDOR Clear Setting this bit to 1 clears CRCDOR to H'0000.

- CRC Data Input Register (CRCDIR) - Number of bits: 8, Address: H'FFFED5
  CRCDIR is an 8-bit readable/writable register, to which the bytes to be CRC-operated are written. The result is obtained in CRCDOR.

- CRC Data Output Register (CRCDOR) - Number of bits: 16, Address: H'FFFED6
  CRCDOR is a 16-bit readable/writable register that contains the result of CRC operation when the bytes to be CRC-operated are written to CRCDIR after CRCDOR is cleared. When the CRC operation result is additionally written to the bytes to which CRC operation is to be performed, the CRC operation result will be H'0000 if the data contains no CRC error. When bits 1 and 0 in CRCCR are set to G1 = 0 and G0 = 1, respectively, the lower byte of this register contains the result.

(5) Flowchart

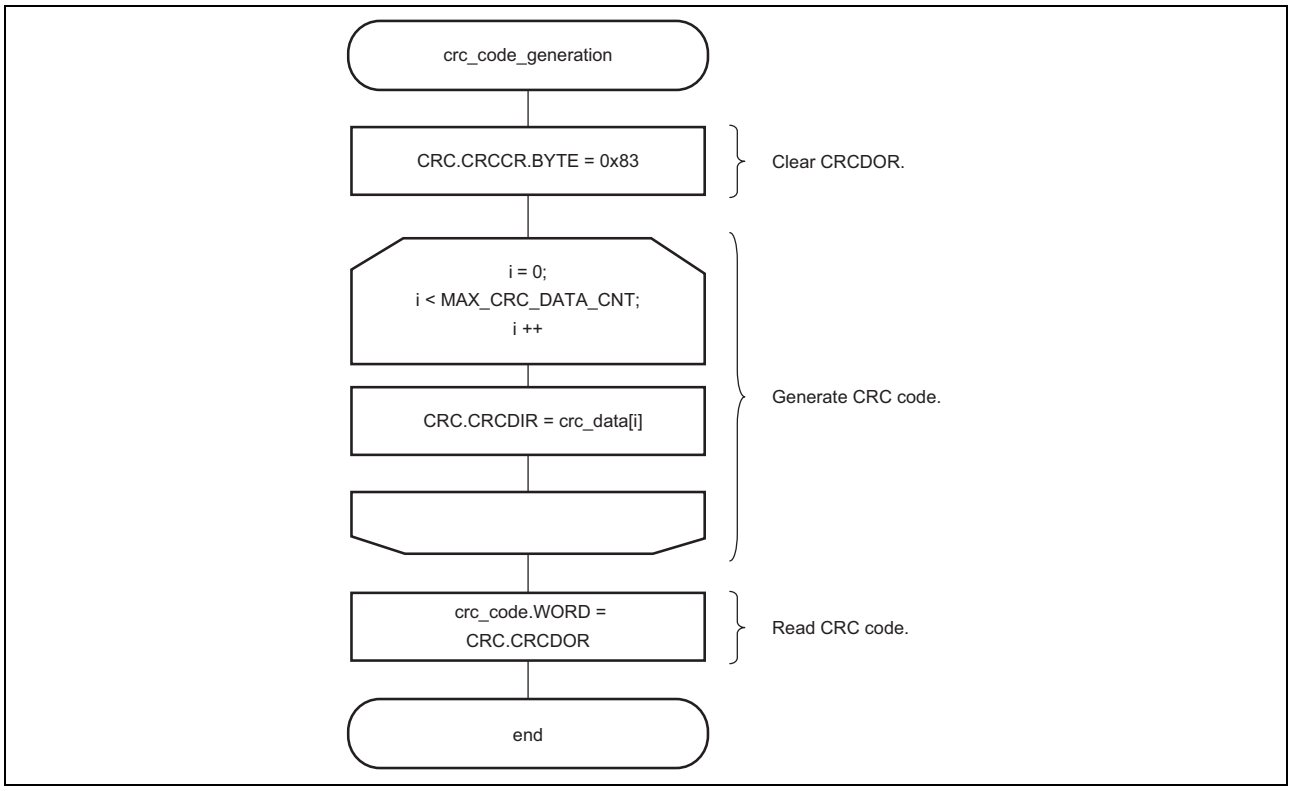

Figure 9 CRC Code Generation Flowchart (crc_code_generation)

5.5.5 mistake_detection Function

(1) Functional Overview

The mistake_detection function detects errors in the data block using the CRC operation circuit.

(2) Arguments

None

(3) Returned values

None

(4) Description of internal I/O registers used

The internal I/O registers used by this function are shown below. Note that the setting values shown are those used for this sample task and differ from the initial values.

- CRC Control Register (CRCCR) - Number of bits: 8, Address: H'FFFED4

Bit	Bit Name	Set Value	R/W	Descriptions
7	DORCLR	0	W	CRCDOR Clear Setting this bit to 1 clears CRCDOR to H'0000.

- CRC Data Input Register (CRCDIR) - Number of bits: 8, Address: H'FFFED5
  CRCDIR is an 8-bit readable/writable register, to which the bytes to be CRC-operated are written. The result is obtained in CRCDOR.

- CRC Data Output Register (CRCDOR) - Number of bits: 16, Address: H'FFFED6
  CRCDOR is a 16-bit readable/writable register that contains the result of CRC operation when the bytes to be CRC-operated are written to CRCDIR after CRCDOR is cleared. When the CRC operation result is additionally written to the bytes to which CRC operation is to be performed, the CRC operation result will be H'0000 if the data contains no CRC error. When bits 1 and 0 in CRCCR are set to G1 = 0 and G0 = 1, respectively, the lower byte of this register contains the result.

(5) Flowchart

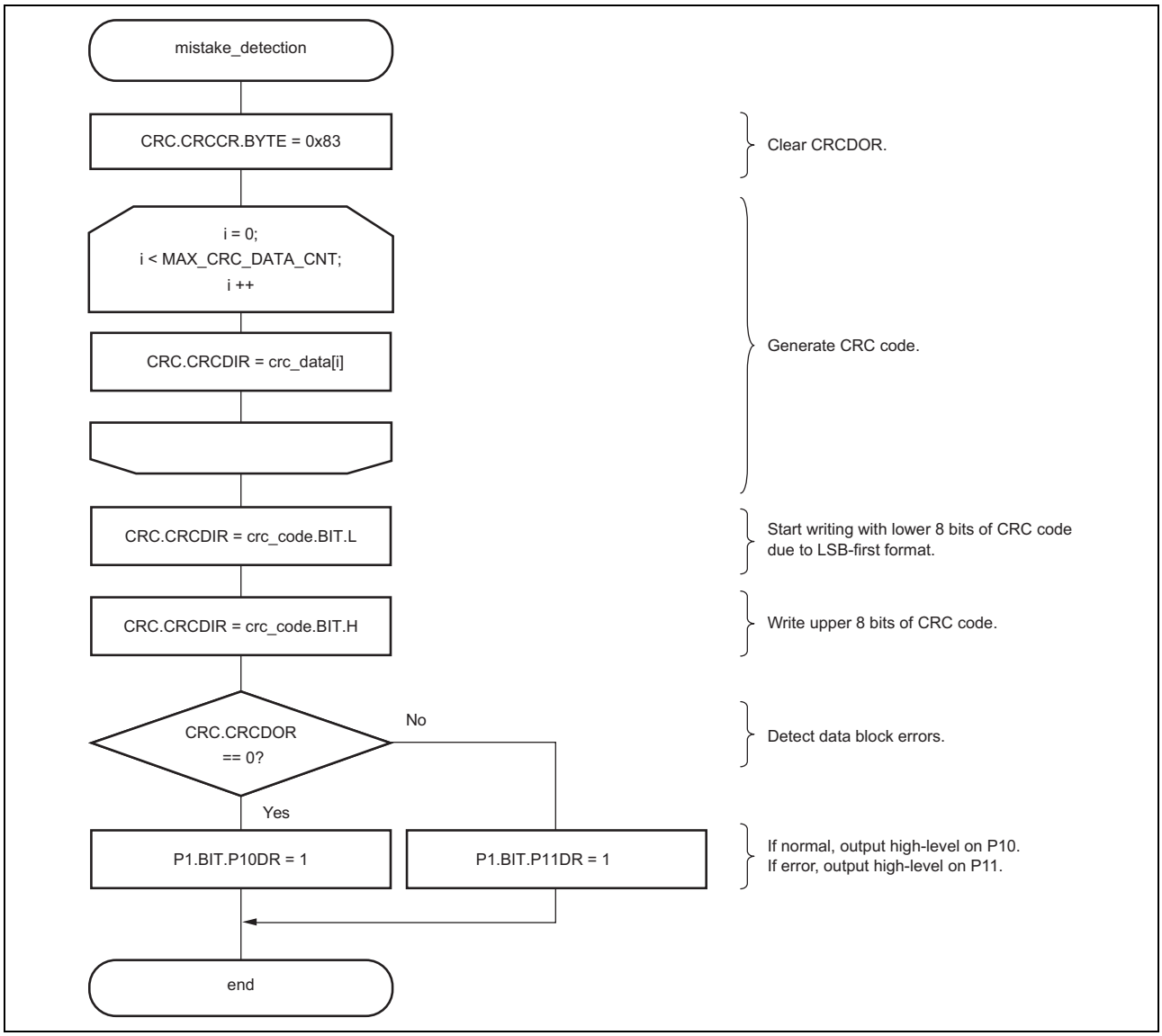

Figure 10 Error Detection Flowchart (mistake_detection)

6. Reference Documents

- Hardware Manual
  H8S/2472, H8S/2463, H8S/2462 Group Hardware Manual
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- Development Environment Manual
  H8S/300, H8/300 Series C/C++ Compiler Package User's Manual
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