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April 1st, 2010
Renesas Electronics Corporation

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H8S / 2200 Series

Output of Externally Triggered Pulses with Seven-Phases

Introduction

Seven pulse signals synchronized by the falling edge of an external signal are output with individual timing. The delay times from the falling edge of the external signal and pulse widths can be varied.

Target Device

H8S/2239

Contents

1. Specifications

(1) Seven pulse signals synchronized by the falling edge of an external signal are output with individual timing, as is shown in figure 1.
(2) The delay times from the falling edge of the external signal and pulse widths can be varied within these ranges:
200 ns ≤ delay time < cycle of the external signal – pulse width; and
50 ns ≤ pulse width < cycle of the external signal – delay time.
(3) In operation at 20 MHz, the period of the external signal can be set to any desired value between 250 ns and 3.27 ms.

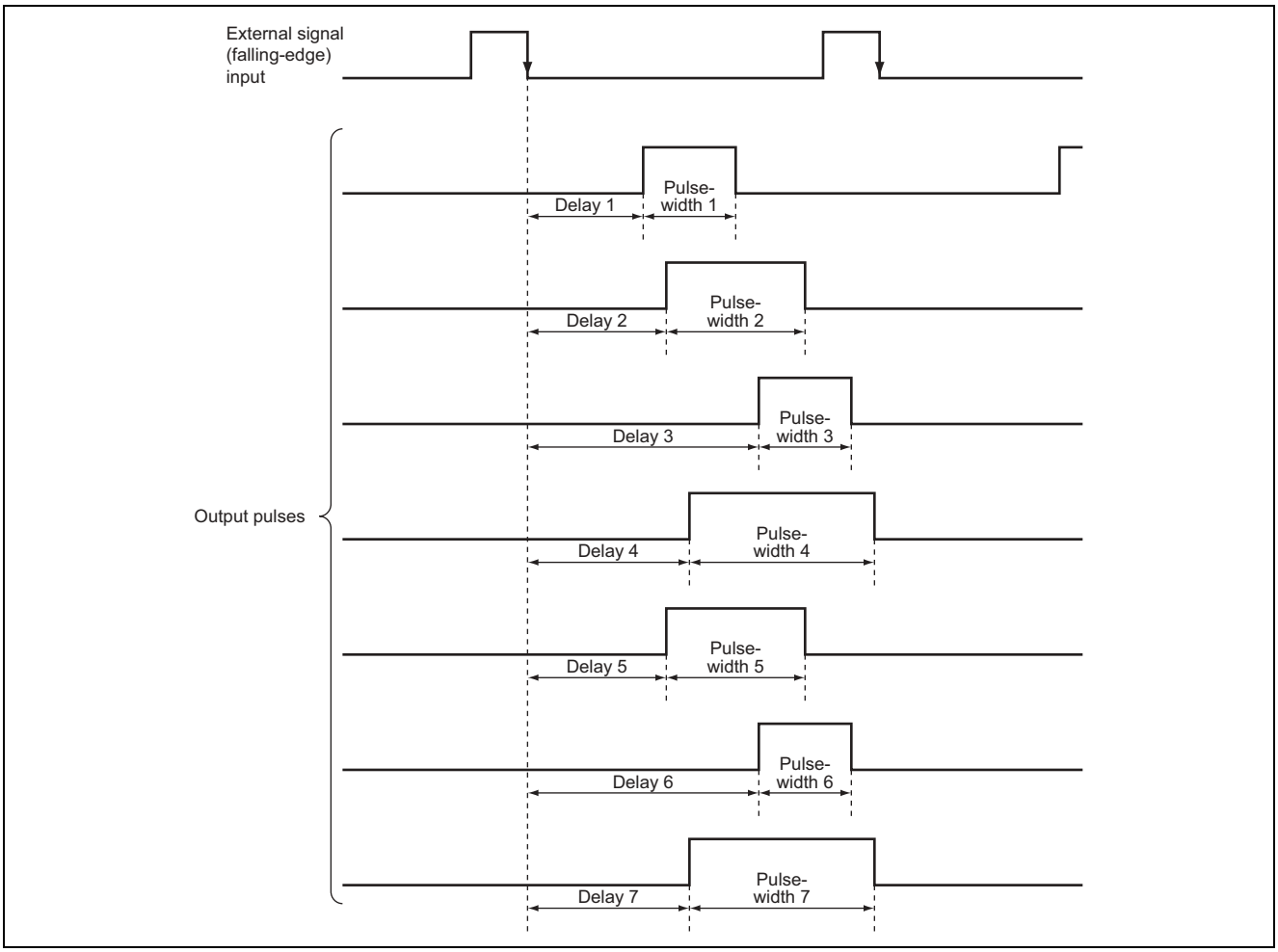


Figure 1 Example of Synchronized Pulse Output

2. Description of Module Usage

(1) In this sample task, multiple timer counters are simultaneously reset by an external signal and produce seven pulse signals with individual phases.

(a) Figure 2 is a block diagram of how the TPU is used in this sample task. Seven pulse signals, each with its own phase, are output in synchronization with an external signal by using the following TPU functions.

- Clearing the timer counter on detecting the falling edge of a pulse
- Simultaneous clearing of multiple timer-counters (synchronized operation)
- Generating a PWM output by using TGRA and TGRB, and TGAC and TGRD, as pairs (PWM mode 1)

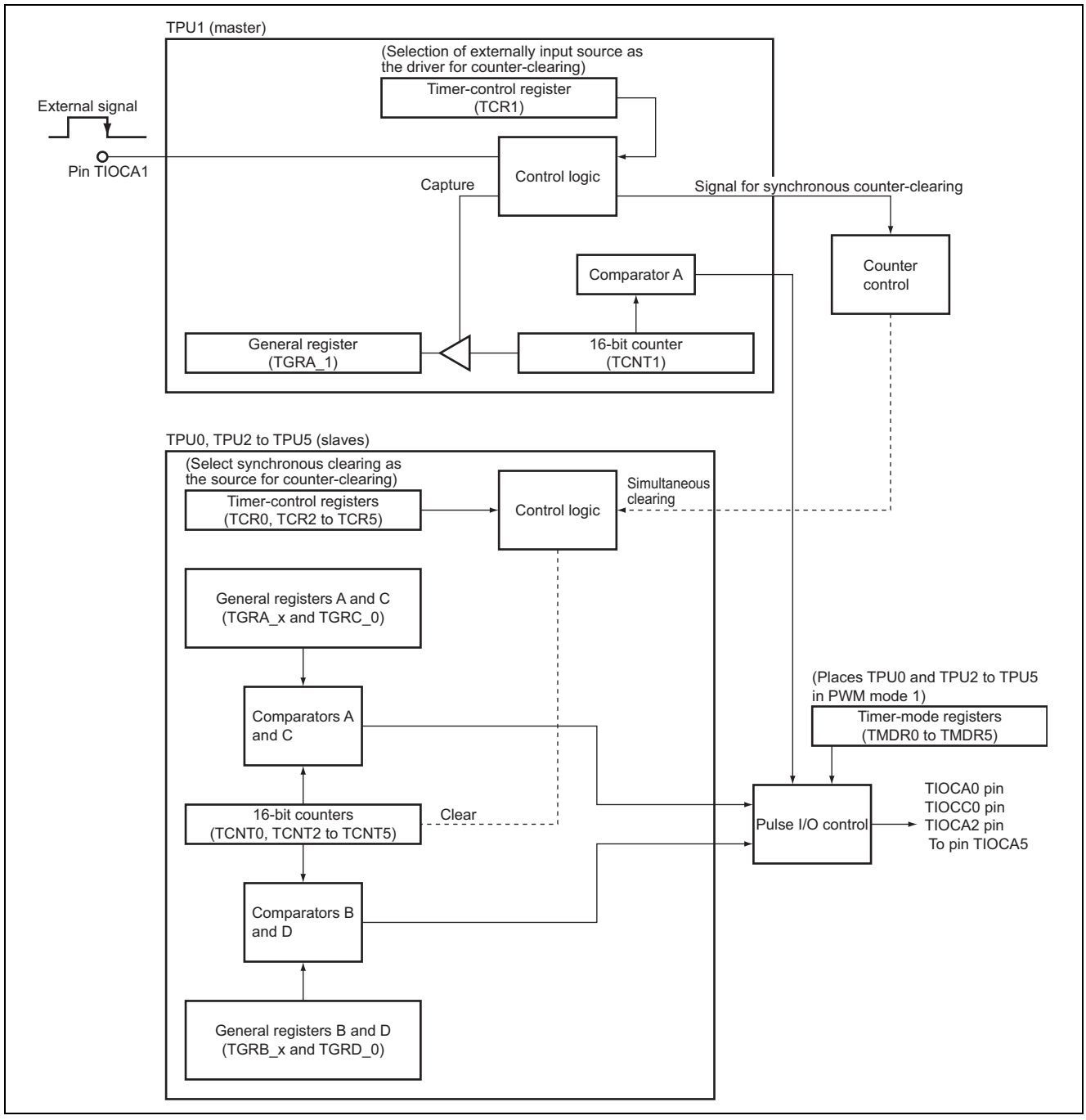


Figure 2 Block Diagram of 7-Phase Pulse Output in Synchronization with an External Trigger

(2) Usage of functions in this sample task is described in table 1. Output of seven pulse trains with seven phases is achieved by using the functions as described in the table.

Table 1 Assignments of Functions

Element	Description
TMDR0 to TMDR5	Selects PWM mode 1 as the operating mode for TPU0 and TPU2 to TPU5
TCR0 to TCR5	Selects the source for clearing of the timer counter
TIOCA1	Inputs the trigger signals
Pins TIOCA0, TIOCC0, and TIOCA2 to TIOCA5	Outputs the PWM waveforms
TGRA_0, TGRC_0, and TGRA_2 to TGRA_5	Timing with which the output level is driven high (delay time)
TGRB_0, TGRD_0, and TGRB_2 to TGRB_5	Timing with which the output level is driven low (pulse width)

3. Principles of Operation

The principle of operation for seven-phase pulse output in synchronization with the external signal is shown in figure 3. As is shown in the figure, the PWM pulses are output through a combination of hardware and software processing.

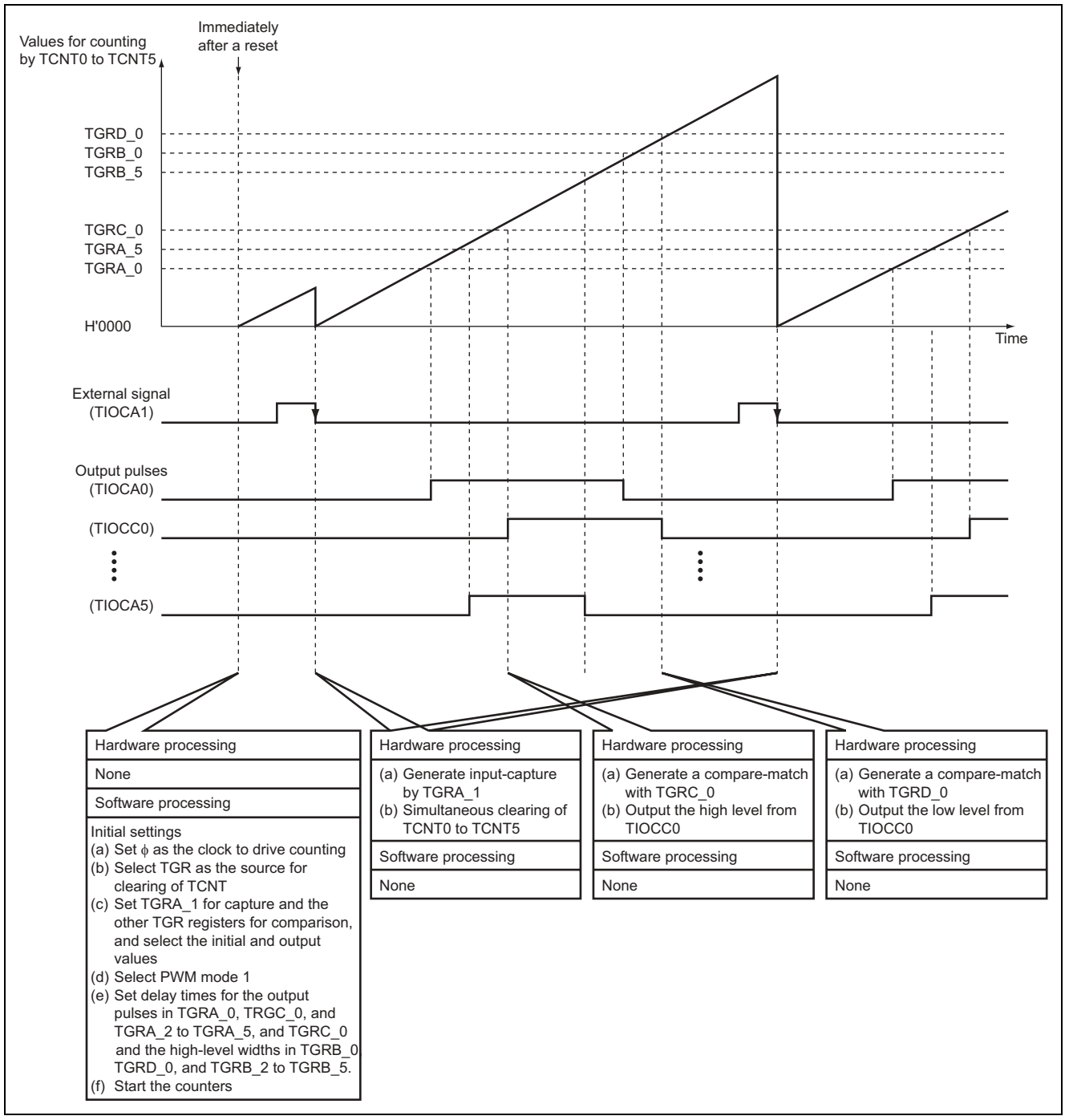


Figure 3 Principle of Operation for Pulse Output

4. Description of Software

(1) Function

Function	Label	Description
Main routine	cntrsmn	Selects simultaneous clearing of TPU0 to TPU5 and sets PWM output

(2) Arguments

Label	Description	Data Length	Used in	I/O
set_wid[0] to set_wid[6]	Timer-counter values that determine the pulse width. The pulse width is obtained by the following expression. Pulse width (ns) = timer-counter value × ϕ period (50 ns in operation at 20 MHz) × frequency divisor of input clock on each channel	unsigned short	Main routine	Input
set_dly[0] to set_dly[6]	Set the timer-counter value that determines the delay time from the falling edge of the externally input pulse until the corresponding output pulse. The delay time is obtained by the following expression. Delay time (ns) = timer-counter value × ϕ period (50 ns in operation at 20 MHz) × frequency divisor of input clock on each channel	unsigned short	Main routine	Input

(3) Internal Registers

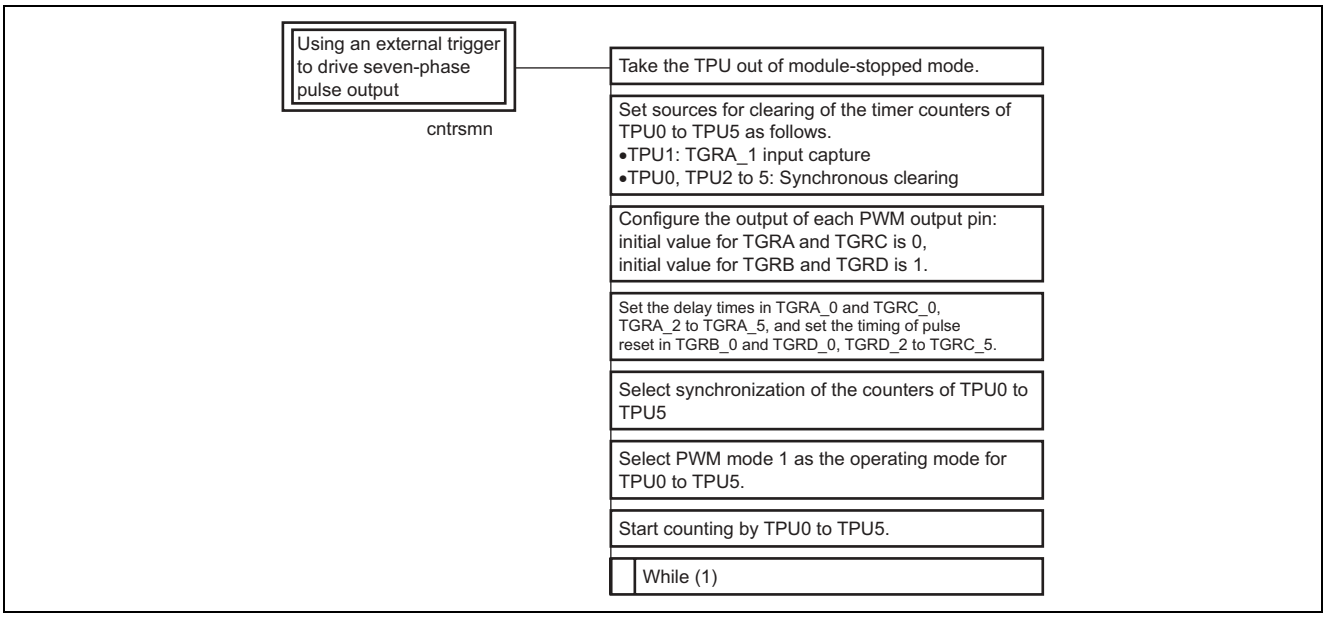
Register	Description	Used in
TSTR	Starts and stops counting by the timer counters of TPU0 to TPU5	Main routine
TSYR	Selects synchronous operation for the timer counters of TPU0 to TPU5	Main routine
TCR0	Sets input-capture to TGR0A as the source for clearing of the timer counters	Main routine
TCR1 to TCR5	Sets synchronous clearing as the source for clearing of all timer counters	Main routine
TIOR0 to TIOR5	Configures the output on each of the PWM output pins. TGRA, TGRC: Initial value = 0; TGRB, TGRD: Initial value = 1.	Main routine
TMDR0 to TMDR5	Selects PWM mode 1	Main routine
TGRA_0 and TGRC_0, TGRA_2 to TGRA_5	Timer-counter values that determine the delay time to the output pulse from each falling edge of the external input pulse	Main routine
TGRA_0 and TGRC_0, TGRA_2 to TGRA_5	Timer-counter values that determine the pulse width on the PWM output pin	Main routine
MSTPCR	Clears the TPU module-stopped mode.	Main routine

(4) RAM Usage

In this sample task, no RAM is used other than that for argument storage.

5. PAD

(1) Main routine



Revision Record

Rev.	Date	Description	
		Page	Summary
1.00	Mar.16.04	—	First edition issued

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