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April 1st, 2010
Renesas Electronics Corporation

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H8S/2200 Series

A/D Conversion by Timer Trigger

Introduction

The A/D converter and DMAC by a conversion start trigger is started from the TPU, A/D conversion of the audio signals is performed and the signals to the RAM are transferred through the DMAC.

Target Device

H8S/2215

Contents

1. Specifications

1. As shown in figure 1, this sample task starts up the A/D converter and DMAC by a conversion start trigger from the TPU, performs A/D conversion of an audio signal, and transfers it to the RAM from the DMAC.
2. The transfer RAM areas are H'600000 to H'60FFFF respectively.
3. The A/D converter starts up by a TGRA compare match of the TPU.
4. The H8S/2215 runs at 16-MHz internal operating frequency.

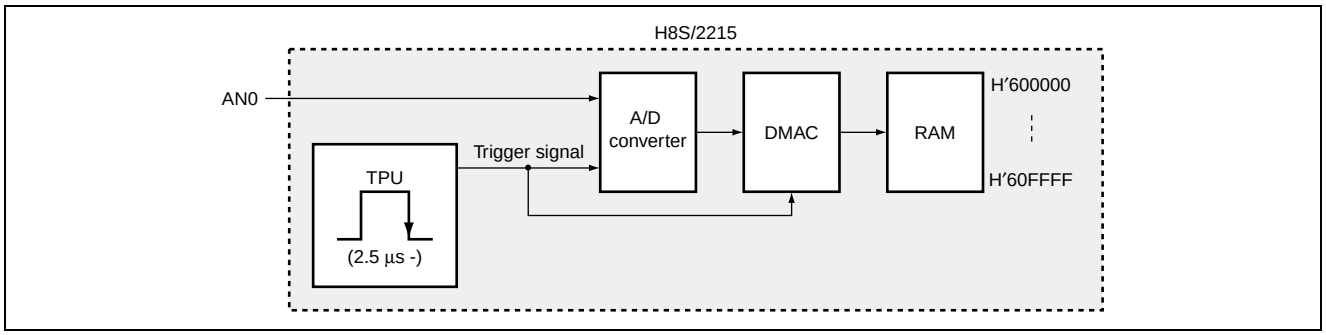


Figure 1 Block Diagram of A/D Conversion by Timer Trigger

2. Description of Functions

1. The block diagram of the DMAC, A/D converter, and TPU to be used by this sample task is shown in figure 2.
   This sample task uses the following DMAC function to transfer A/D conversion results to the RAM:
   A. Function that starts DMAC operation by a compare match A interrupt from the TPU
   This sample task uses the following A/D functions to perform sampling:
   A. Function that starts conversion by a trigger from TPU
   B. Function that performs sampling of input voltages of AN0
   This sample task uses the following TPU function to perform sampling:
   A. Function that can generates a conversion start trigger to the A/D converter

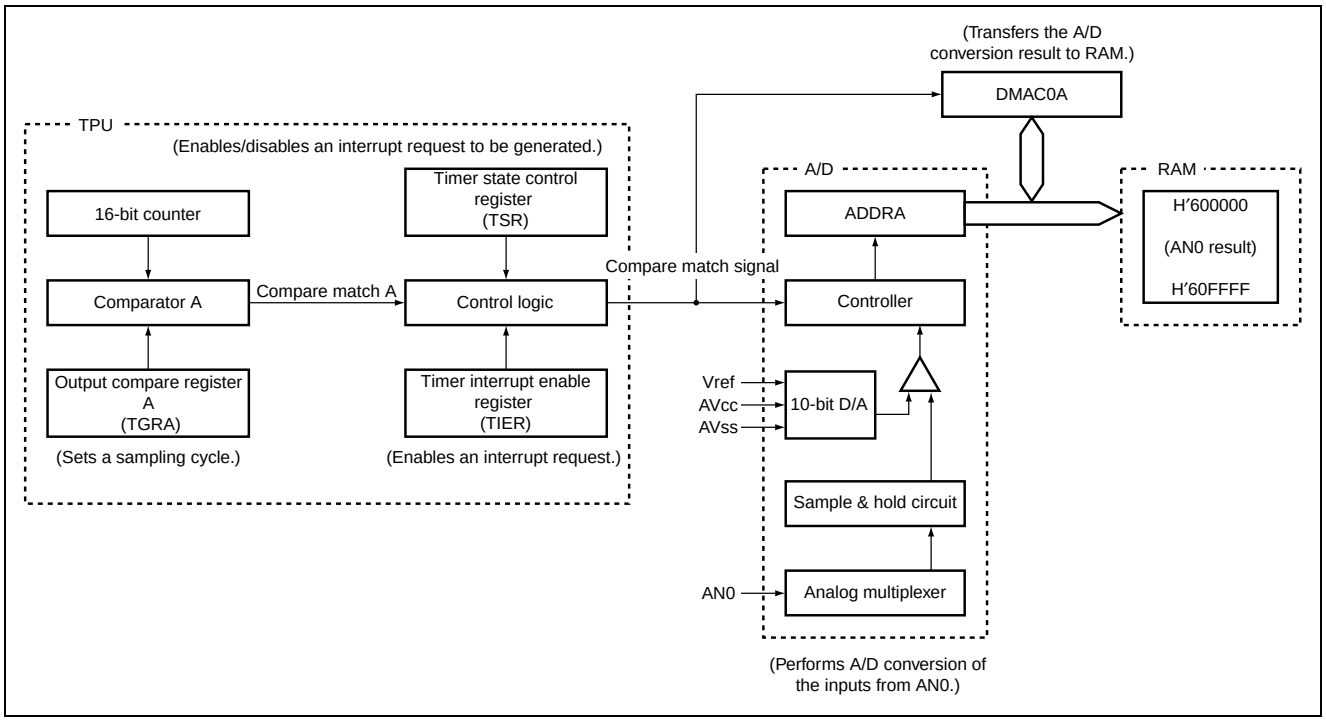


Figure 2 Block Diagram of A/D Conversion by Timer Trigger

2. Function allocation of this sample task is shown in table 1. This sample task allocates H8S/2215 functions as shown in table 1 to transfer A/D conversion results to the RAM.

Table 1 Assignment of Functions

Elements		Description
A/D	AN0	Analog signal input pin
	ADDRA	Stores A/D conversion results.
DMAC	DMABCR	Controls operation of each channel.
	DMACR	Sets the transfer mode to the sequential mode.
	MAR	Sets the transfer destination addresses.
	IOAR	Sets the transfer source addresses.
	ETCR	Sets the transfer count.
TPU	TGR	Sets the cycle.
	TCR	Selects the clock, counter clear source, etc.
	TIOR	Sets TGR as the output compare register.

3. Principles of Operation

The principles of operations used are shown in figure 3. This sample task performs H8S/2215 hardware processing as shown in figure 3 to store A/D conversion results in RAM.

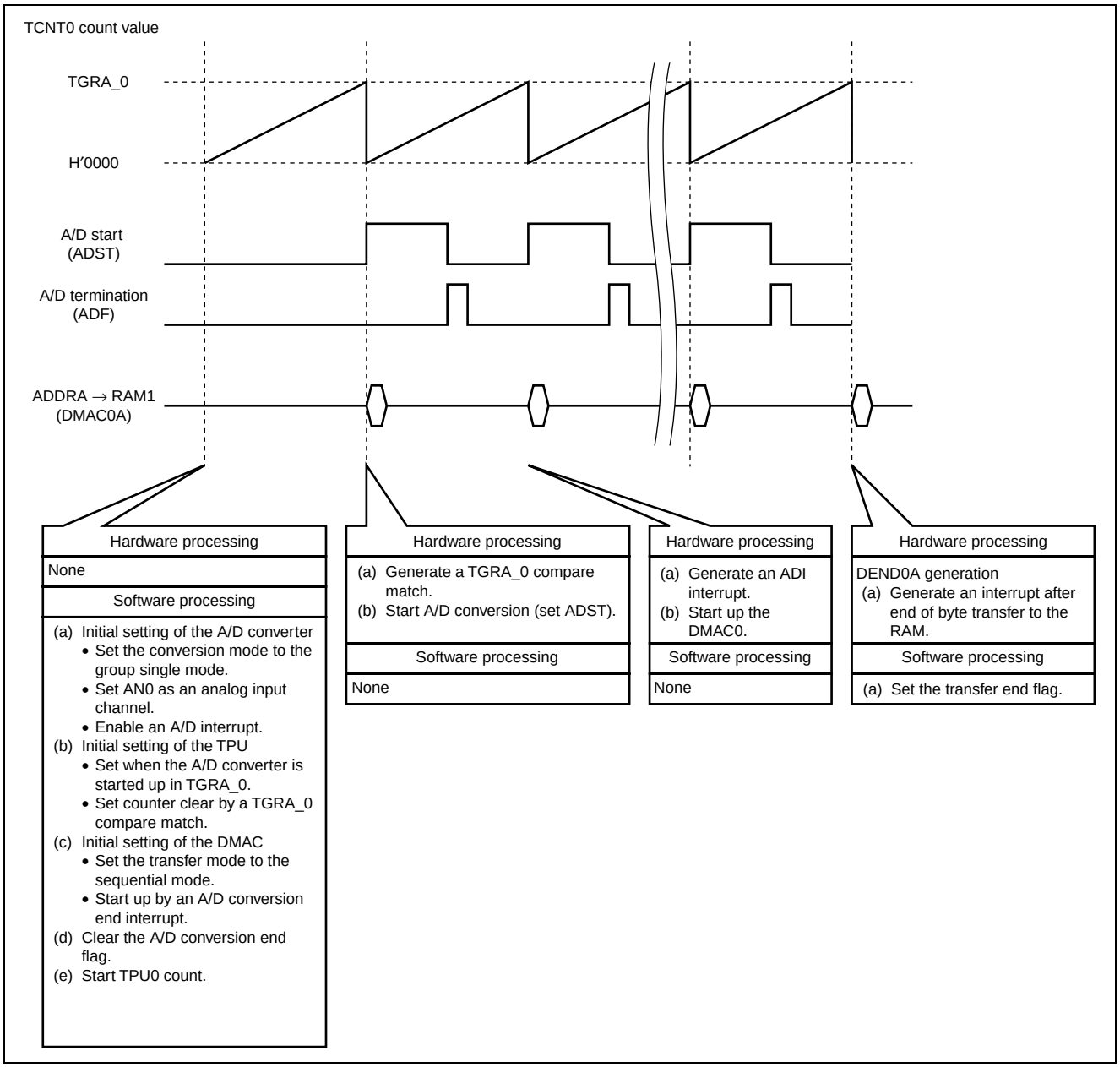


Figure 3 Principles of Operations Used of A/D Conversion by Timer Trigger

4. Description of Software

1. Description of Modules

Module Name	Label Name	Function
Main routine	tpuadmn	Performs initial setting of the TPU, DMAC, and A/D sets the RAM to be used.
A/D conversion end	adend	Sets the A/D conversion end flag.

2. Description of Arguments

Label Name	Function	Data Length	Used in	I/O
ad_end	Indicates end of data transfer from H'A00000 to H'A0FFFF. 1: Data transfer ended 0: Data transfer in progress	unsigned char	Main routine A/D conver-sion end	Input Output
ad_data	Stores A/D conversion results of AN0, starting from addata0 by DMA transfer in the one byte units. Transfers the conversion results to the RAM as follows: Upper bit AD9 AD8 AD7 AD6 AD5 AD4 AD3 AD2	unsigned char	Main routine	Input
sum_cyc	Sets the timer value equivalent to the sampling cycle of A/D conversion. Cycle (ns) = timer counter value × ϕ cycle (62.5 ns during 16-MHz operation)	unsigned short	Main routine	Input

3. Description of Internal Registers Used

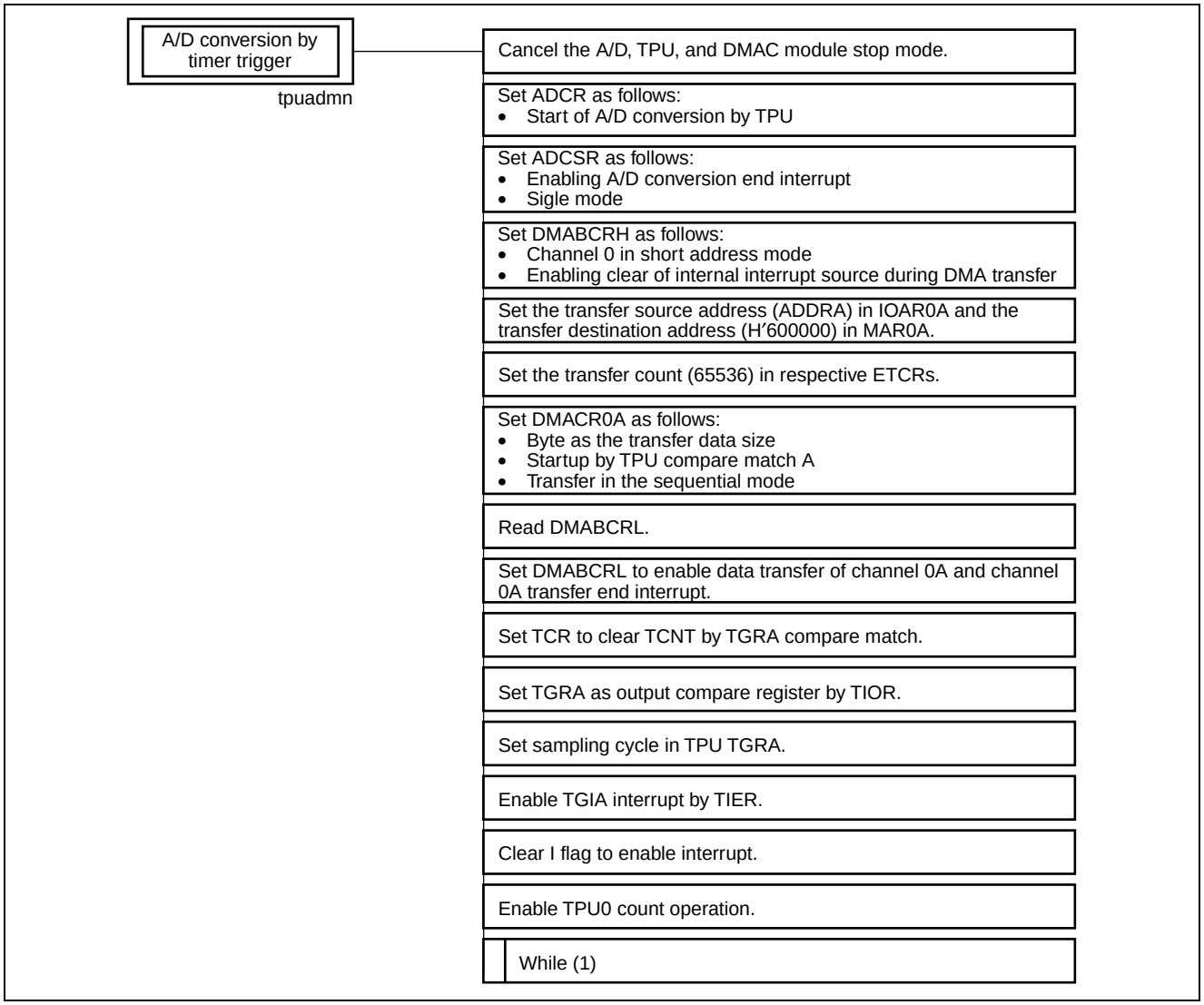
Implemented Function	Register Name	Function
TPU	TGRA	Sets the sampling cycle of A/D conversion.
	TIER	Enables a TGIEA interrupt.
	TCR	Sets TPU0 as follows: • Counter clear at detection of a TGRA compare match • Count by internal clock ϕ
	TIOR	Sets TGRA as the output compare register and inhibits pin output.
	TSTR	Enables TCNT0 count operation.
DMAC	DMABCR	Controls operation of each channel.
	DMACR0A	Sets the DMAC0A as follows: • Byte size transfer • Sequential mode • Enabling clear of the internal interrupt source during DMA transfer • Enabling data transfer and transfer end interrupt
	IOAR0	Sets the transfer source addresses.
	MAR0	Sets the transfer destination addresses.
	ETCR0	Sets the transfer count (H'0000).
A/D	ADCR	Sets ADCR as follows: • Start of A/D conversion by the TPU0
	ADCSR	Sets ADCSR as follows: • Enabling an A/D conversion end interrupt • Single mode • AN0 as input channels
MSTPCR		Cancels the module stop mode.

4. RAM Usage

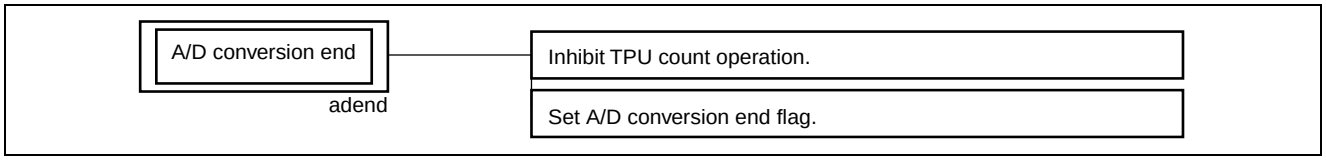
This sample task uses only arguments.

5. PAD

1. Main Routine



2. A/D Conversion End



Revision Record

Rev.	Date	Description	
		Page	Summary
1.00	Mar.16.04	—	First edition issued

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