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H8S Family

Two-Phase Excitation Control of a Stepping Motor

Introduction

This application note discusses how to implement two-phase excitation control of a two-phase stepping motor by using the TPU, PPG, and DTC functions of the H8S/2377.

Target Device

H8S/2377

Contents

1. Specifications

- A two-phase stepping motor is controlled using the TPU, PPG, and DTC functions incorporated in the H8S/2377.
- The stepping motor is controlled through two-phase excitation and repeats the following sequence: forward rotation → stop → reverse rotation → stop.
- Speed-up and slow-down processing is performed without software intervention.
- To protect the driver, a shoot-through current prevention period is set.

Figure 1 shows the connections for two-phase stepping motor control.

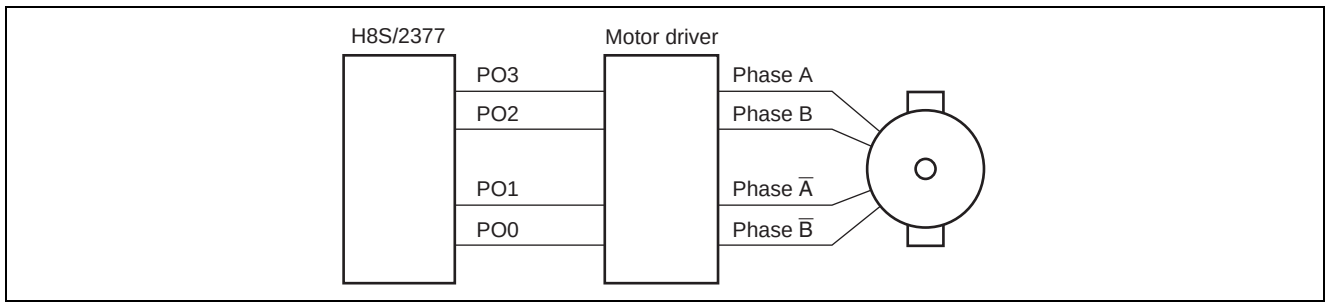


Figure 1 Connections for Two-Phase Stepping Motor Control

2. Applicable Conditions

Table 1 Applicable Conditions

Item	Contents
Operating frequency	Input clock: 19.6608 MHz System clock: 19.6608 MHz Peripheral module clock: 19.6608 MHz External bus clock: 19.6608 MHz
Operating mode	Mode 4 (MD2 = 1, MD1 = 0, MD0 = 0)
Development tool	HEW Version 3.01.02
C/C++ compiler	H8S, H8/300 SERIES C/C++ Compiler Version 6.00.02 (from Renesas Technology Corp.)
Compile option	-cpu = 2000a:24, -code = machinecode, -optimize = 1, -regparam = 3 -speed = (register, shift, struct, expression)

Table 2 Section Settings

Address	Section Name	Description
H'000000	CV1	Reset vector
H'0000A0	CV2	TPU TGI0A interrupt vector
H'000450	DDTCV	DTC transfer request vector
H'001000	P	Program area
	C	Data table storage
H'FF7000	B	RAM area

3. Description of Functions

3.1 Motor Specifications

This sample task uses a permanent magnet-type stepping motor (KP6P8-701 produced by Japan Servo Co., Ltd.). Table 3 summarizes the standard specifications of the KP6P8-701.

Table 3 Standard Specifications of KP6P8-701

Item	Specification
Model	KP6P8-701
Number of phases	2
Step angle [degree/step]	7.5
Voltage [V]	12
Current [A/phase]	0.33
Winding resistance [Ω/phase]	36
Inductance [mH/phase]	28
Maximum static torque [mN•m]	78.4
Detent torque [mN•m]	1.3
Rotor inertia [g•cm^2]	23.7

3.2 Description of Functions

The H8S/2377's functions used to control the stepping motor are described below. Figure 2 is a block diagram of the functions used in this sample task.

- DTC
  - Activated by compare-match A of the TPU.
  - Transfers an output pattern in the output pattern table to the NDR register of the PPG. After the transfer of an output pattern, the DTC transfers the pulse period data in the period data table to the TGRB register of the TPU by chain transfer.
- TPU
  - Compare-match A: Activates the DTC and PPG.
  - Compare-match B: Clears the timer counter and activates the PPG.
- PPG
  - In this sample task, outputs 4 bits of pulse signals that include shoot-through current prevention period (non-overlap time).
  - Compare-match B: Outputs pulse signals of high-to-low transition and suspends output of low-to-high transition.
  - Compare-match A: Outputs the low-to-high pulse signals that are suspended on compare-match B above. (This output is delayed by the time set by TGRA.)

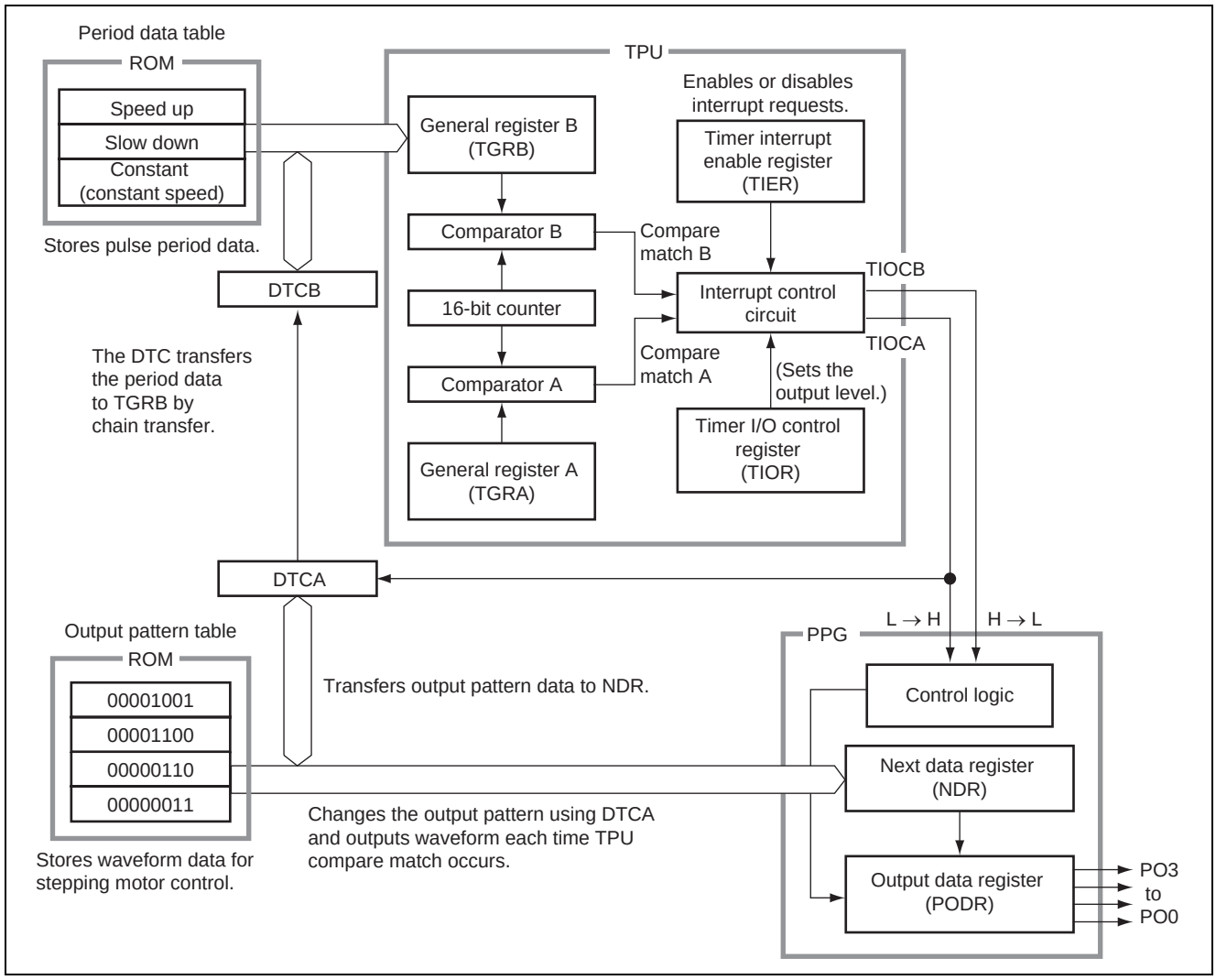


Figure 2 H8S/2377's Functions Used in This Application

3.3 DTC Vector Table

Figure 3 shows an example of DTC vector table and memory allocation. The DTC register information is stored from address H'FFBC00 in this order: MRA, SAR, MRB, DAR, CRA, and CRB. In the DTC vector table, the lower 2 bytes (H'BC00) of the start address of register information is set.

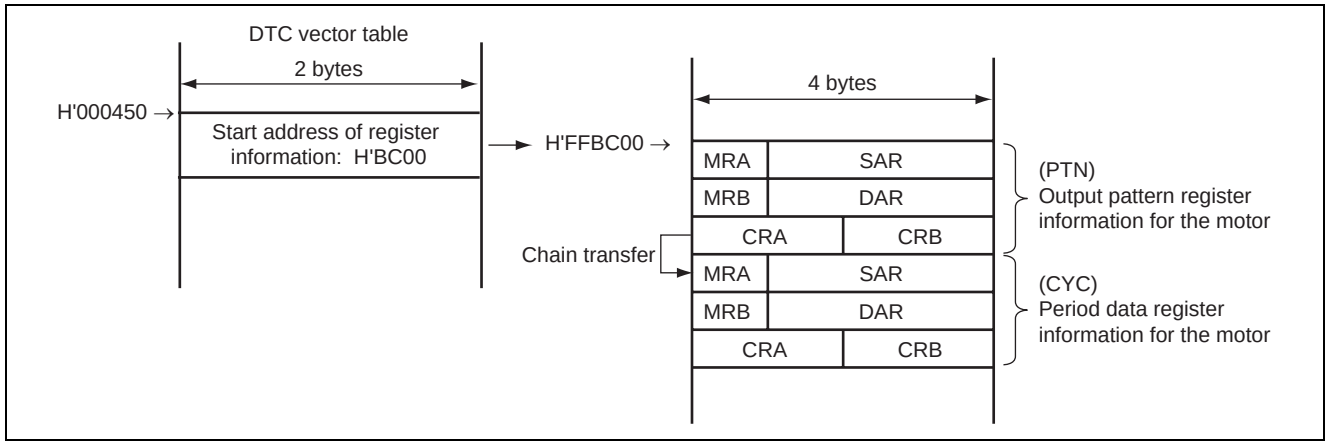


Figure 3 Example of DTC Vector Table and Memory Allocation

4. Description of Operation

4.1 Stepping Motor Operation

Figure 4 shows an example of two-phase stepping motor operation through two-phase excitation where the step angle of the motor is 7.5 degrees/step. The operation is summarized below.

- When the output pulse is high, the corresponding phase is excited, as shown in figure 4.
- Firstly, phases A and $\overline{B}$ are excited and the rotor is positioned between phases $\overline{B}$ and A.
- Next, phases A and B are excited simultaneously and the rotor is positioned between phases A and B. Subsequently, two adjacent phases are excited in the following sequence to cause the rotor to rotate: phases $\overline{B}$ and A $\rightarrow$ phases A and B $\rightarrow$ phases B and $\overline{A}$ $\rightarrow$ phases $\overline{A}$ and $\overline{B}$.
- Reverse rotation of the stepping motor is achieved by exciting the phases in the reverse sequence: phases $\overline{A}$ and $\overline{B}$ $\rightarrow$ phases B and $\overline{A}$ $\rightarrow$ phases A and B $\rightarrow$ phases $\overline{B}$ and A.
- The stepping motor is stopped by holding the phase excitation for a specified period at the last phase of forward or reverse rotation.

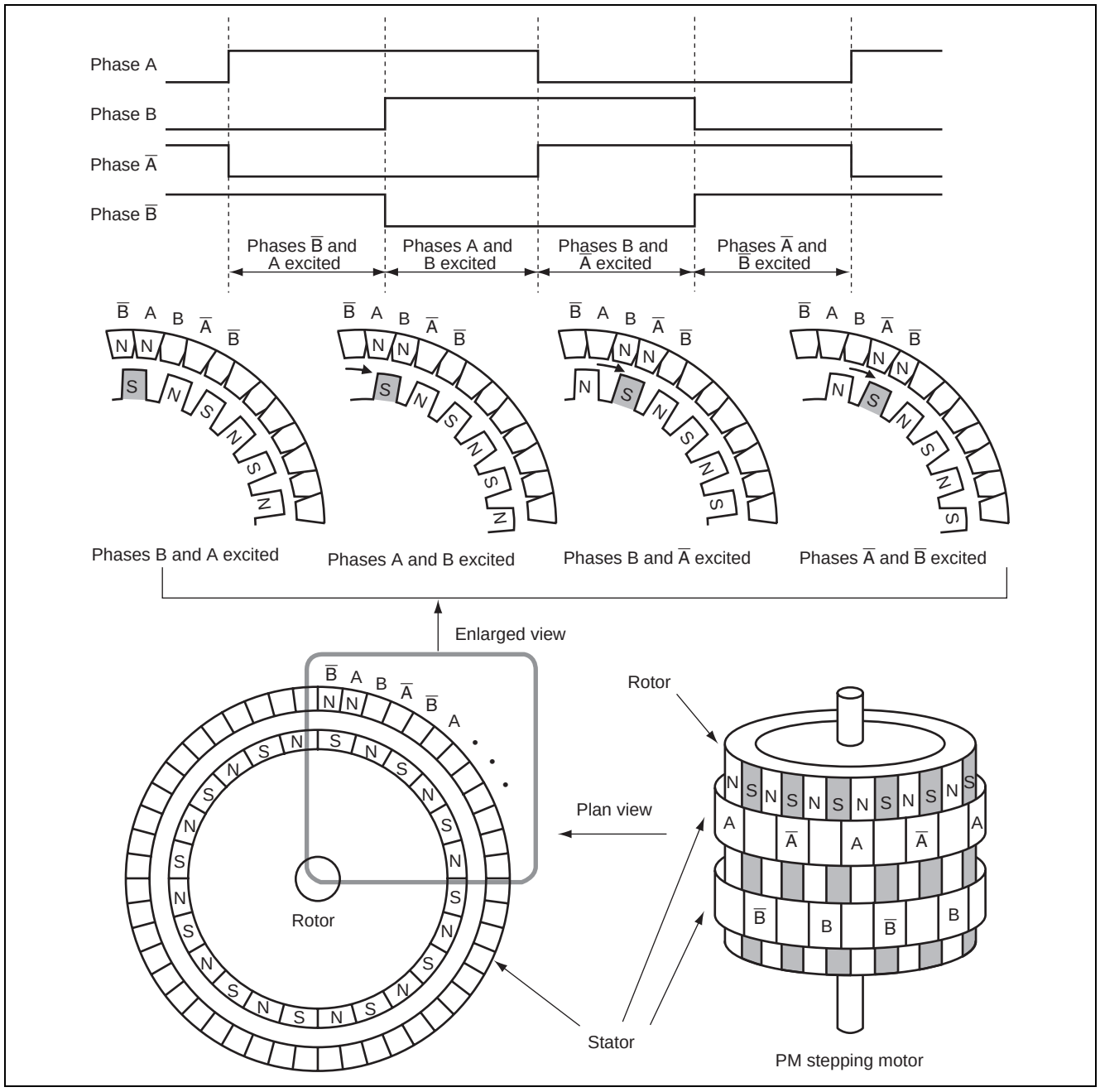


Figure 4 Example of Stepping Motor Operation

4.2 Non-Overlap Time

When the output pattern is switched, the shoot-through current prevention period n (non-overlap time) is inserted as shown in figure 5. The motor driver may be damaged by a turn-off delay that occurs when the excitation pattern is switched. Non-overlap time is inserted to prevent this problem.

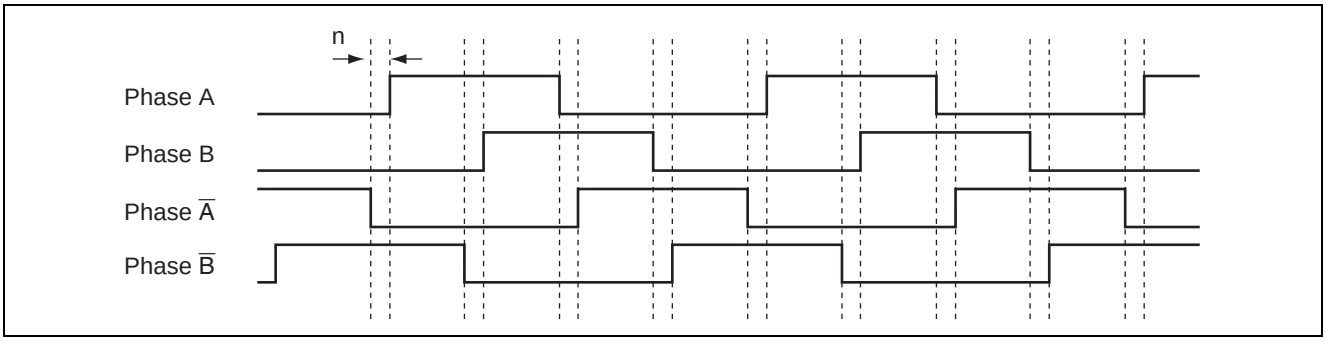


Figure 5 Example of Output with Non-Overlap Time

4.3 Speed-Up and Slow-Down Operation

Speed-up and slow-down operations effectively prevent motor from being out of step. In particular, if a train of short-period pulses is suddenly output, the motor may not be able to handle the load and does not rotate. Speed-up and slow-down operation control is applied to avoid this problem. The speed-up and slow-down operation sequence is described below.

- The pulse period is gradually shortened until the specified number of pulses has been output (Speed up).
- The specified number of pulses with a fixed pulse period is output (Constant speed).
- The pulse period is gradually extended until the specified number of pulses has been output (Slow down).

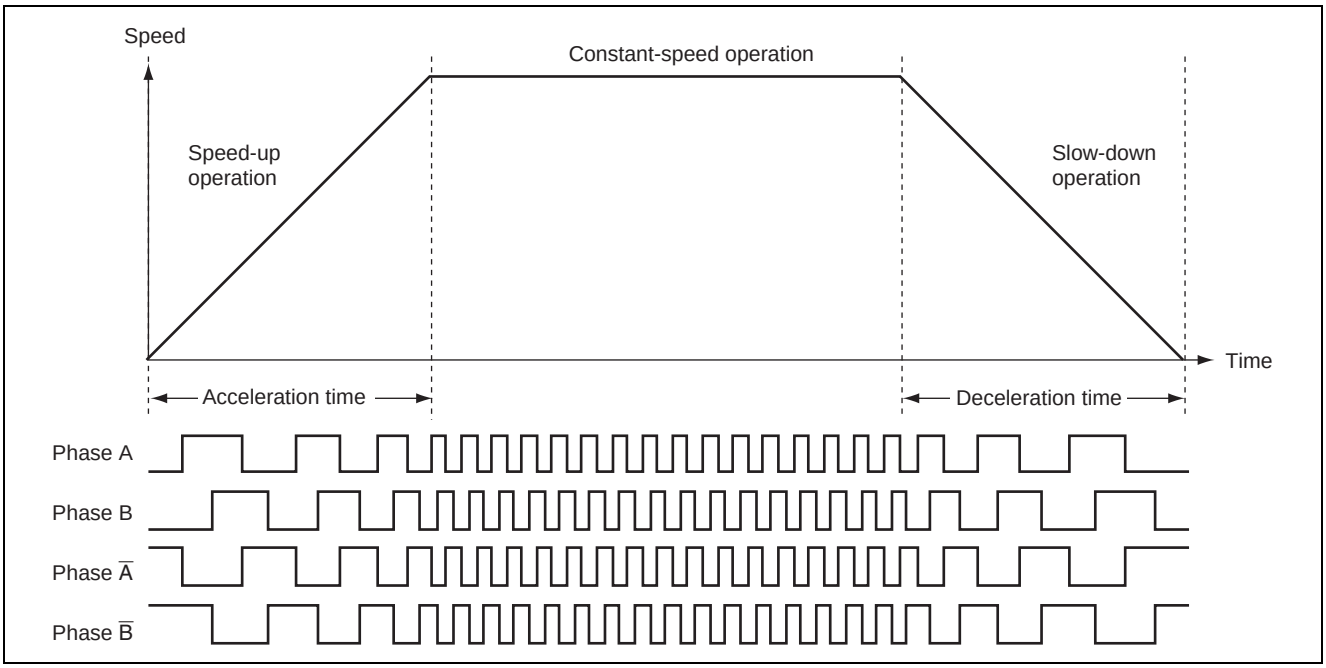


Figure 6 Speed-Up and Slow-Down Operations

4.4 Flow of Stepping Motor Control

Figure 7 shows the flowchart of stepping motor control.

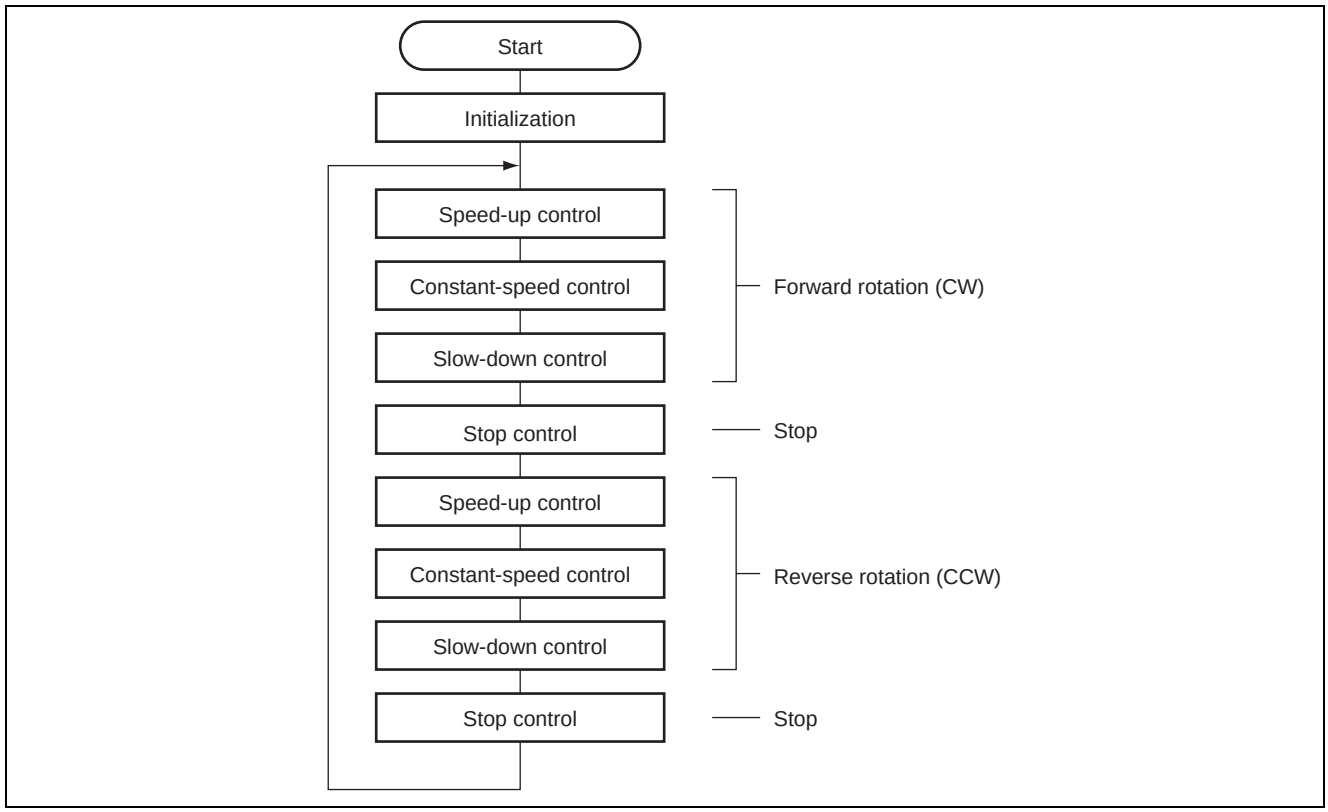


Figure 7 Flowchart of Stepping Motor Control

4.5 Example of Four-Phase Pulse Output

Figure 8 shows an example of four-phase output.

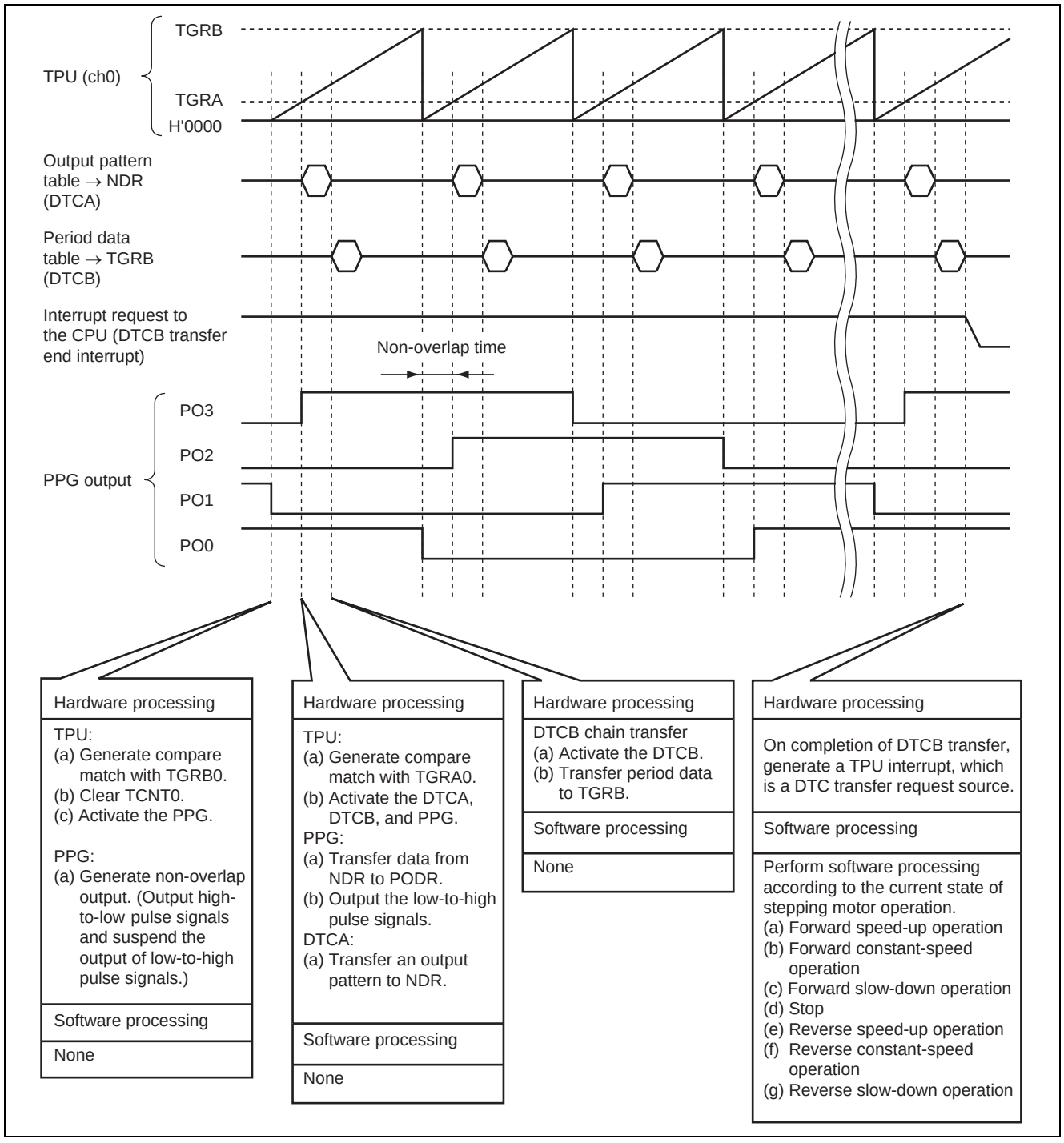


Figure 8 Timing of Stepping Motor Operation

5. Description of Software

5.1 List of Functions

Table 4 lists the functions used in this sample task. Figure 9 shows the function hierarchy in this sample task.

Table 4 List of Functions

Function Name	Functions
init	Initialization routine: Cancels module stop mode, sets clocks, and calls main function.
main	Main routine: Initializes the TPU, PPG, and DTC and makes settings for forward speed-up operation.
tgi0a_int	TPU interrupt processing: Controls motor operation in each stage.
fslowup0	Called after completion of reverse stop operation and changes the DTC transfer modes for forward speed-up operation.
fconst0	Called after completion of forward speed-up operation and switches the DTC transfer modes for forward constant-speed operation.
fslowdwn0	Called after completion of forward constant-speed operation and changes the DTC transfer modes for forward slow-down operation.
rslowup0	Called after completion of forward stop operation and changes the DTC transfer modes for reverse speed-up operation.
rconst0	Called after completion of reverse speed-up operation and changes the DTC transfer modes for reverse constant-speed operation.
rslowdwn0	Called after completion of reverse constant-speed operation and changes the DTC transfer modes for reverse slow-down operation.
frstop0	Called after completion of reverse slow-down operation and changes the DTC transfer modes for stop operation.

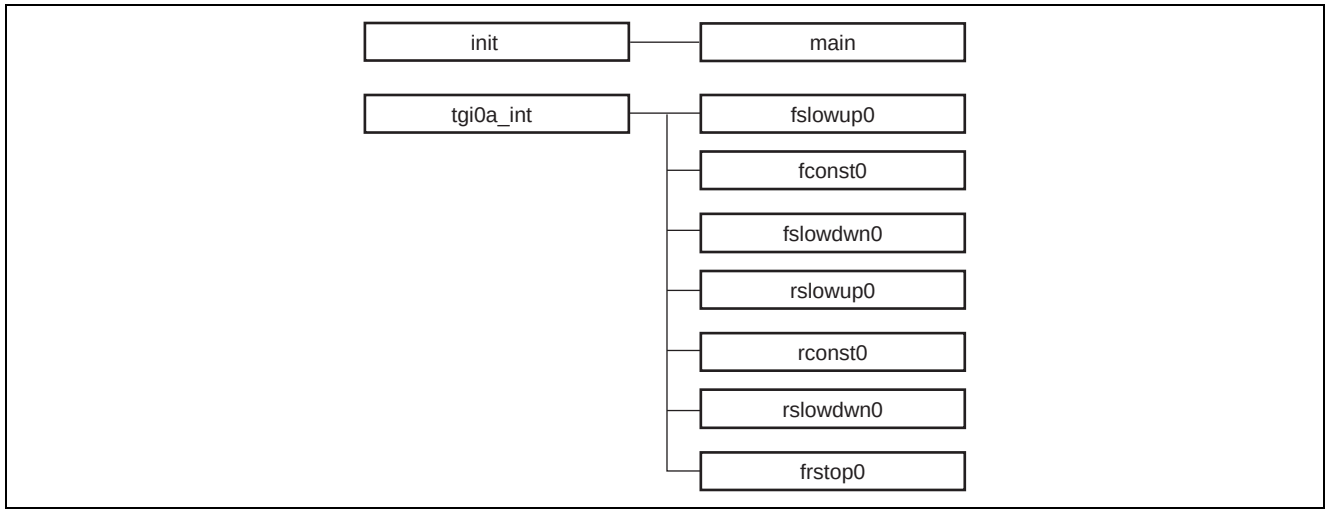


Figure 9 Hierarchy of Functions

5.2 Constants

Table 5 lists the constants used in this sample task.

Table 5 Description of Constants

Constant Name	Value	Description
UPTIME	49	Number of steps for speed-up and slow-down operations
CNSTTIME	481	Number of steps for constant-speed operation
STOPTIME	20	Number of steps for stop operation

5.3 Data Table Variables

- Output Pattern Table

  Data table of output patterns for stepping motor excitation.

```
pattbl[4] = {
   0xF6, .... Excites phase B̄ (PO0) and phase A (PO3)
   0xF3, .... Excites phase A (PO3) and phase B (PO2)
   0xF9, .... Excites phase B (PO2) and phase Ā (PO1)
   0xFC, .... Excites phase Ā (PO1) and phase B̄ (PO0)
};
```

- Period Data Table

```
uptbl[49] = {
    0x4E00, 0x4D00, 0x4C00, 0x4B00, 0x4A00, 0x4900, 0x4800, 0x4700, 0x4600, 0x4500,
    0x4400, 0x4300, 0x4200, 0x4100, 0x4000, 0x3F00, 0x3E00, 0x3D00, 0x3C00, 0x3B00,
    0x3A00, 0x3900, 0x3800, 0x3700, 0x3600, 0x3500, 0x3400, 0x3200, 0x3000, 0x2E00,
    0x2D00, 0x2C00, 0x2B00, 0x2A00, 0x2900, 0x2800, 0x2700, 0x2600, 0x2500, 0x2400,
    0x2300, 0x2200, 0x2100, 0x2000, 0x1F00, 0x1E00, 0x1D00, 0x1C00, 0x1B00,
};
```

5.4 Internal Registers

- System Clock Control Register (SCKCR) Address: H'FFFF3B

Bit	Bit Name	Setting	Function
2	SCK2	0	System clock select 2, 1, 0
1	SCK1	0	00: Division ratio is 1/1.
0	SCK0	0	

- Extension Module Stop Control Register H, L (EXMSTPCRH, EXMSTPCRL)
  Address: H'FFFF42, H'FFFF43

Bit	Bit Name	Setting	Function
4	MSTP20	0	I^2C bus interface 2_1 (IIC2_1) 0: Cancels module stop mode. 1: Sets module stop mode.
3	MSTP19	0	I^2C bus interface 2_0 (IIC2_0) 0: Cancels module stop mode. 1: Sets module stop mode.

- PLL Control Register (PLLCR) Address: H'FFFF45

Bit	Bit Name	Setting	Function
1	STC1	0	Frequency multiplication factor setting
0	STC0	0	00: Frequency multiplication factor of the PLL circuit is ×1.

- Module Stop Control Register H, L (MSTPCRH, MSTPCRL) Address: H'FFFF40, H'FFFF41

Bit	Bit Name	Setting	Function
15	ACSE	0	All-module-clocks-stop mode enable 0: Disables all-module-clocks-stop mode. 1: Enables all-module-clocks-stop mode.
14	MSTP14	0	EXDMA controller (EXDMA) 0: Cancels module stop mode. 1: Sets module stop mode.
13	MSTP13	0	DMA controller (DMAC) 0: Cancels module stop mode. 1: Sets module stop mode.
12	MSTP12	0	Data transfer controller (DTC) 0: Cancels module stop mode. 1: Sets module stop mode.
11	MSTP11	0	16-bit timer pulse unit (TPU) 0: Cancels module stop mode. 1: Sets module stop mode.
10	MSTP10	0	Programmable pulse generator (PPG) 0: Cancels module stop mode. 1: Sets module stop mode.
9	MSTP9	0	D/A converter (channels 0, 1) 0: Cancels module stop mode. 1: Sets module stop mode.
8	MSTP8	0	D/A converter (channels 2, 3) 0: Cancels module stop mode. 1: Sets module stop mode.
7	MSTP7	0	D/A converter (channels 4, 5) 0: Cancels module stop mode. 1: Sets module stop mode.
6	MSTP6	0	A/D converter 0: Cancels module stop mode. 1: Sets module stop mode.
5	MSTP5	0	Serial communication interface 4 (SCI_4) 0: Cancels module stop mode. 1: Sets module stop mode.
4	MSTP4	0	Serial communication interface 3 (SCI_3) 0: Cancels module stop mode. 1: Sets module stop mode.
3	MSTP3	0	Serial communication interface 2 (SCI_2) 0: Cancels module stop mode. 1: Sets module stop mode.
2	MSTP2	0	Serial communication interface 1 (SCI_1) 0: Cancels module stop mode. 1: Sets module stop mode.
1	MSTP1	0	Serial communication interface 0 (SCI_0) 0: Cancels module stop mode. 1: Sets module stop mode.
0	MSTP0	0	8-bit timer (TMR) 0: Cancels module stop mode. 1: Sets module stop mode.

- Port 2 Data direction Register (P2DDR) Address: H'FFFE21

Bit	Bit Name	Setting	Function
3	P23DDR	1	1111: P23 (PO3) to P20 (PO0) function as output port pins.
2	P22DDR	1	
1	P21DDR	1	
0	P20DDR	1	

- DTC Enable Register C (DTCERC) Address: H'FFFF2A

Bit	Bit Name	Setting	Function
13	DTCEC5	1	0: Disables DCT activation by TGI0A interrupt of the TPU_0. 1: Enables DCT activation by TGI0A interrupt of the TPU_0.

- PPG Output Control Register (PCR) Address: H'FFFF46

Bit	Bit Name	Setting	Function
1	G0CMS1	0	Group 0 compare match select 1, 0
0	G0CMS0	0	00: Output of pulse output group 0 is triggered by compare-match of TPU channel 0.

- PPG Output Mode Register (PMR) Address: H'FFFF47

Bit	Bit Name	Setting	Function
4	G0INV	1	Group 0 invert 0: Inverted output 1: Direct output
0	G0NOV	1	Group 0 non-overlap 0: Normal operation. 1: Non-overlap operation.

- Next Data Enable Register L (NDERL) Address: H'FFFF49

Bit	Bit Name	Setting	Function
7	NDER7	0	Next data enable 7 to 0 When a bit in this register is set to 1, data of the corresponding bit in NDRL is transferred to PODRL, triggered by the selected output trigger. Data transfer from NDRL to PODRL does not take place for the bits whose corresponding bits in this register are clear.
6	NDER6	0	
5	NDER5	0	
4	NDER4	0	
3	NDER3	1	
2	NDER2	1	
1	NDER1	1	
0	NDER0	1	

- Output Data Register L (PODRL) Address: H'FFFF4B

Bit	Bit Name	Setting	Function
7	POD7	0	Output data register 7 to 0
6	POD6	0	For the bits set to generate pulse outputs by NDERL, the values of the corresponding bits in NDRL are transferred to this register by the output trigger during PPG operation. While a bit in NDERL is set to 1, the CPU cannot write to the corresponding bit of this register. While a bit in NDERL is clear, the initial pulse output value can be set in the corresponding bit of this register.
5	POD5	0	
4	POD4	0	
3	POD3	1	
2	POD2	1	
1	POD1	0	
0	POD0	0	

- Next Data Register L (NDRL) Address: H'FFFF4F

Bit	Bit Name	Setting	Function
3	NDER3	1	Next data 3 to 0
2	NDER2	1	The contents of this register are transferred to the corresponding bits in the PODRL by the output trigger specified by PCR.
1	NDER1	0	
0	NDER0	0	

- Timer Start Register (TSTR) Address: H'FFFFC0

Bit	Bit Name	Setting	Function
0	CST0	1	Counter start 0 0: Stops counting by TCNT_0 of the TPU. 1: Starts counting by TCNT_0 of the TPU.

- Timer Control Register_0 (TCR_0) Address: H'FFFFB0

Bit	Bit Name	Setting	Function
7	CCLR2	0	Counter clear 2 to 0
6	CCLR1	1	010: Clear TCNT_0 on compare match or input capture by TGRB_0.
5	CCLR0	0	
4	CKEG1	0	Clock edge 1, 0
3	CKEG0	0	00: The counter counts the falling edges when an internal clock is input, or counts the rising edges when an external clock is input.
2	TPSC2	0	Timer prescaler 2 to 0
1	TPSC1	1	010: The counter clock source is the internal clock Pϕ/16.
0	TPSC0	0	

- Timer Interrupt Enable Register_0 (TIER_0) Address: H'FFFFD4

Bit	Bit Name	Setting	Function
0	TGIEA	1	TGR interrupt enable A 0: Disables interrupt request (TGIA) generation by the TGFA bit. 1: Enables interrupt request (TGIA) generation by the TGFA bit.

- Timer Status Register_0 (TSR_0) Address: H'FFFFD5

Bit	Bit Name	Setting	Function
1	TGFB	0	Input capture/output compare flag B Indicates the occurrence of TGRB input capture or compare match. 0: Input capture or compare match has not occurred. 1: Input capture or compare match has occurred.
0	TGFA	0	Input capture/output compare flag A Indicates the occurrence of TGRA input capture or compare match. 0: Input capture or compare match has not occurred. 1: Input capture or compare match has occurred.

- Timer General Register A_0 (TGRA_0) Address: H'FFFFD8
  - Function: A 16-bit register that is compared with the counter in output compare operation.
  - Setting value: H'00000064
- Timer General Register B_0 (TGRB_0) Address: H'FFFFDA
  - Function: A 16-bit register that is compared with the counter in output compare operation.
  - Setting value: H'0000FF00

5.5 RAM Usage

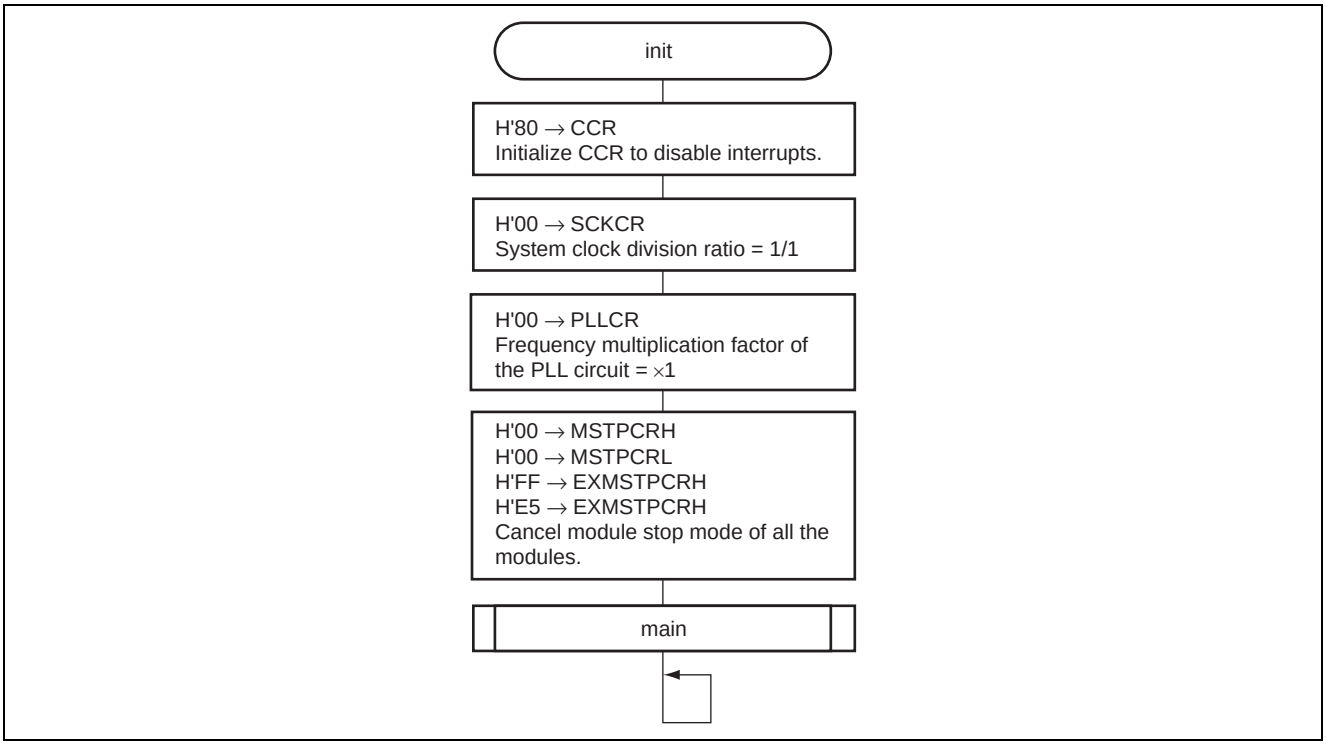
Table 6 describes the RAM usage in this sample task.

Table 6 Description of RAM

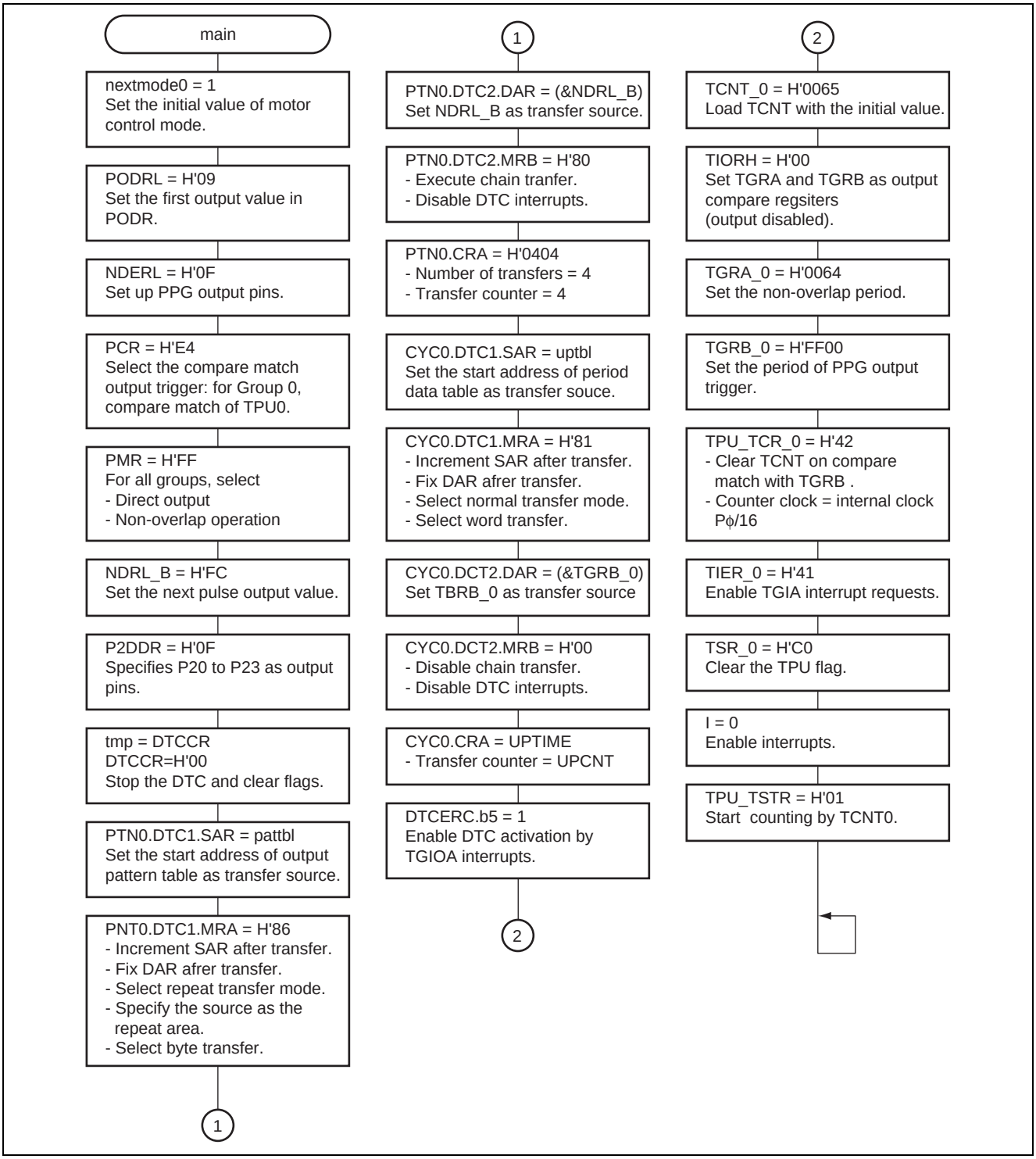
Type	Variable Name	Description
DTC_tag	PTN0	Output pattern register information for motor
DTC_tag	CYC0	Period data register information for motor
unsigned char	nextmode0	Sets stepping motor operating mode. 0: Forward speed-up control 1: Forward constant-speed control 2: Forward slow-down control 3: Stop control 4: Reverse speed-up control 5: Reverse constant-speed control 6: Reverse slow-down control 7: Stop control

6. Flowchart

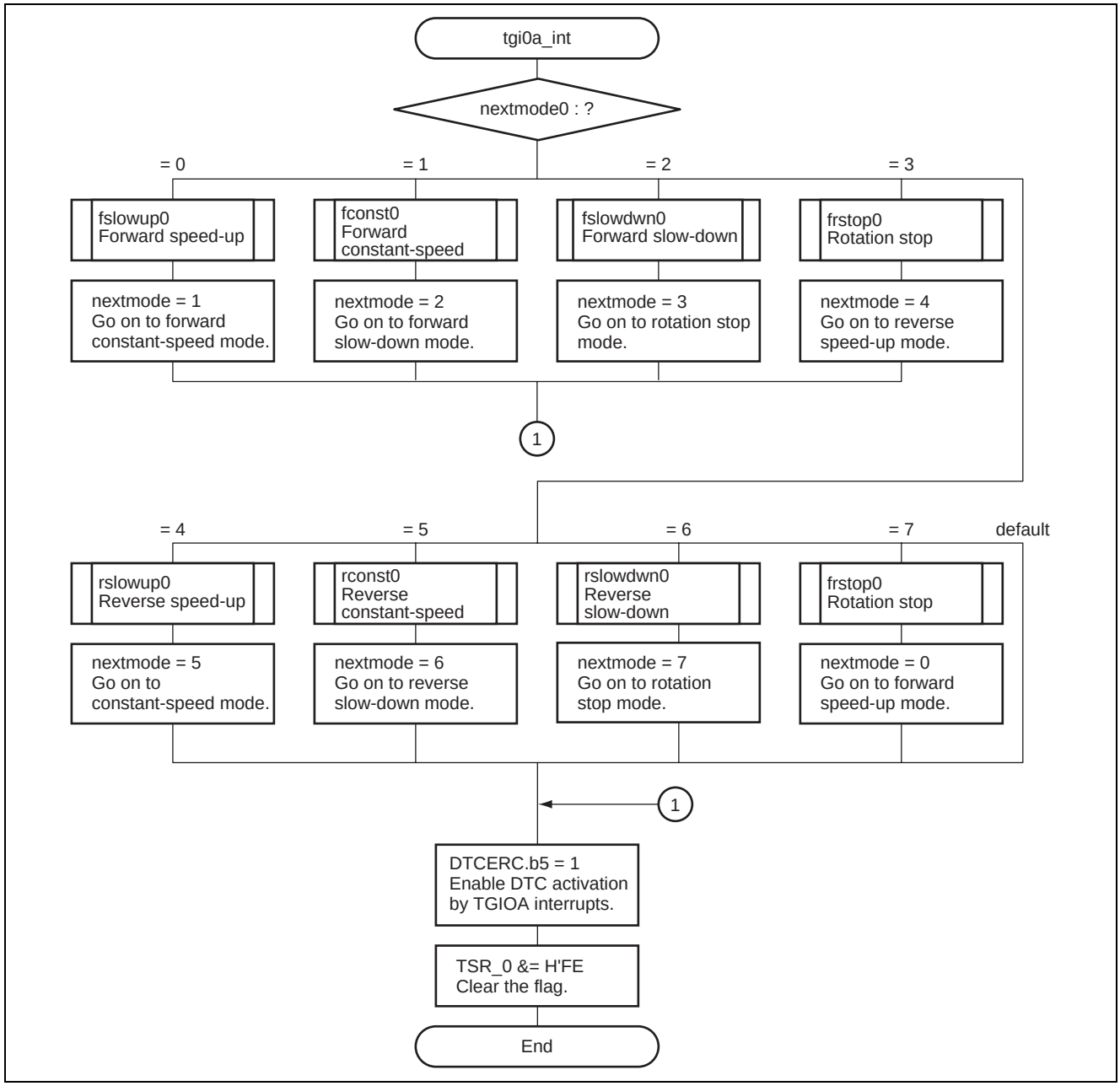
6.1 init Function



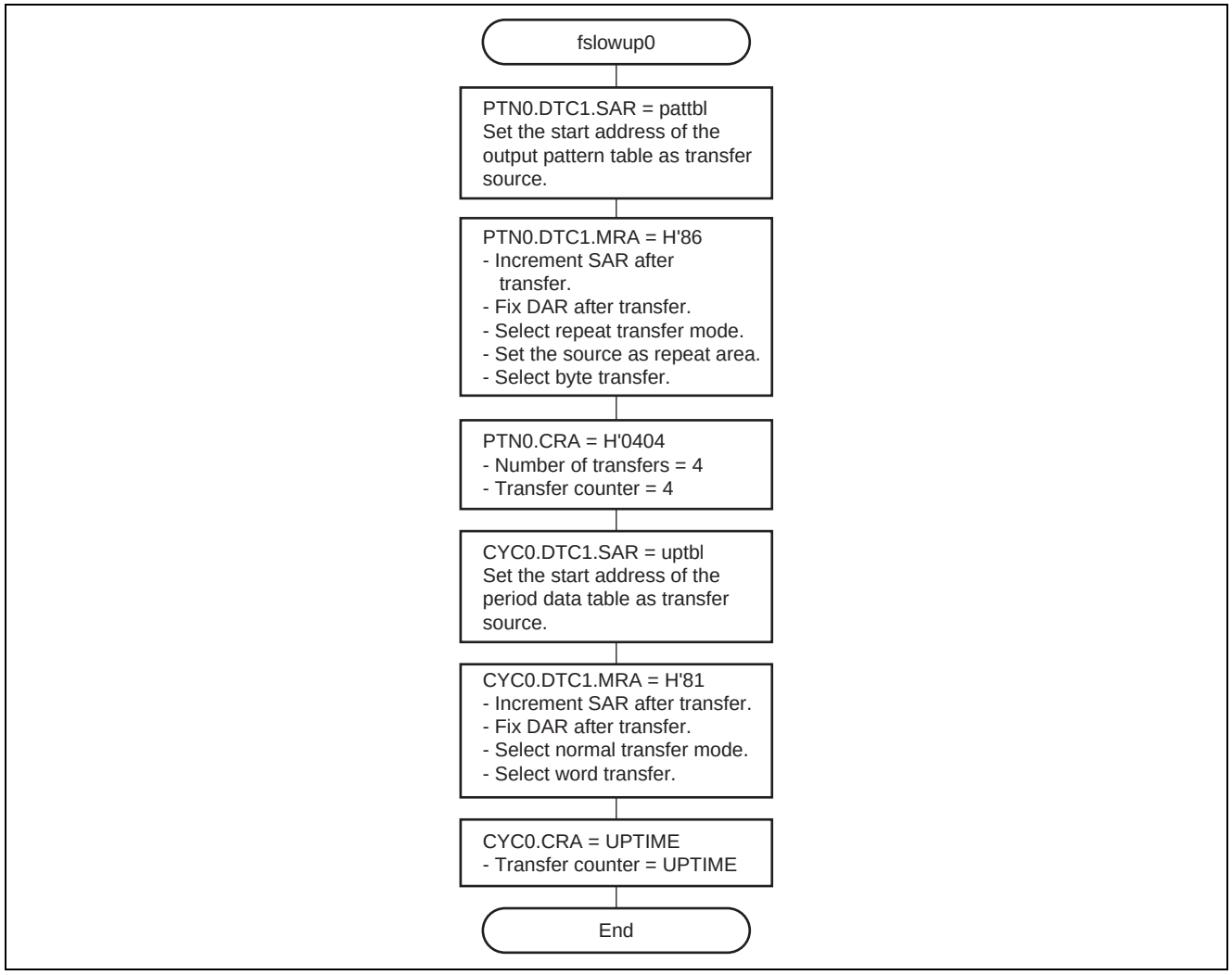
6.2 main Function



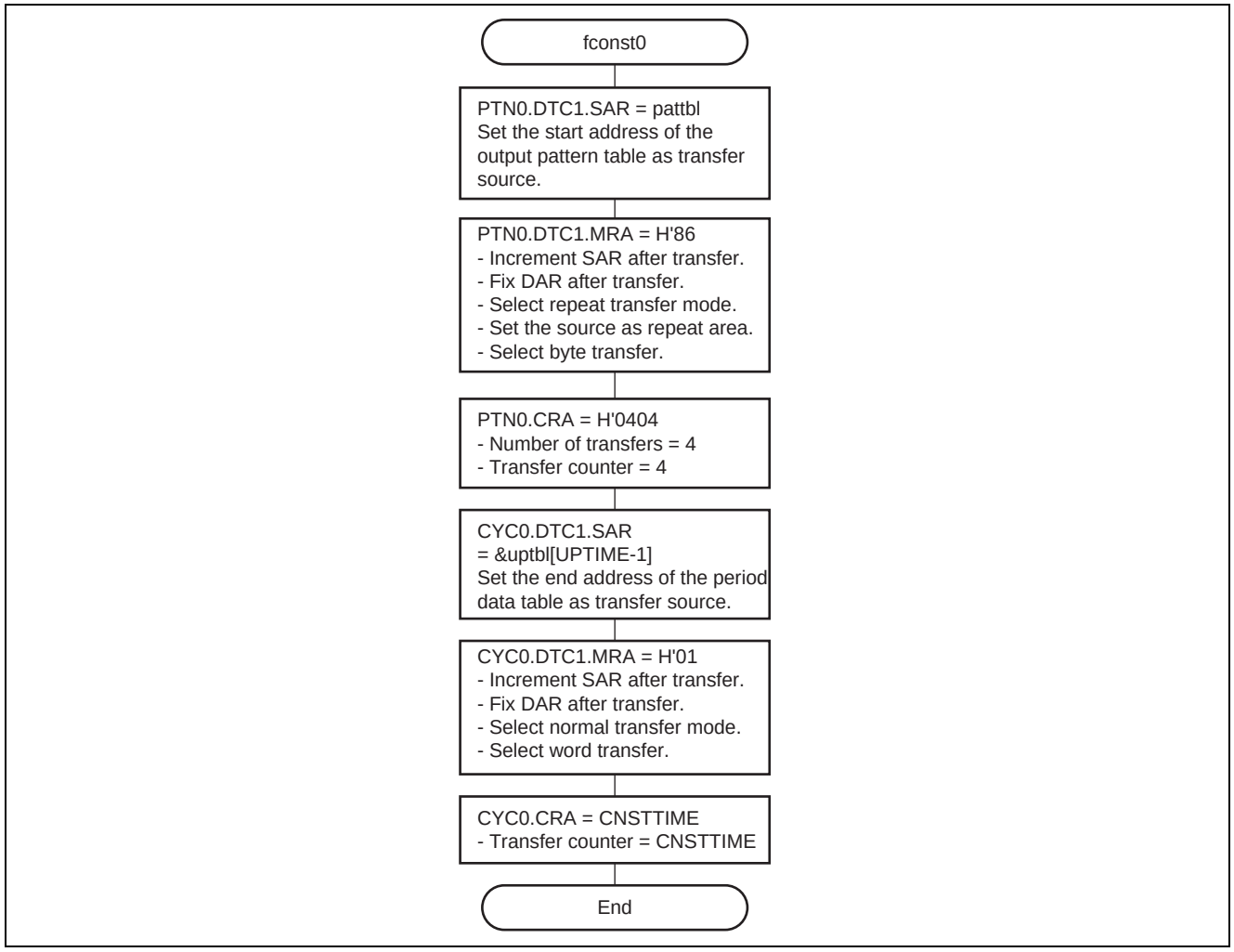
6.3 tgi0a_int Function



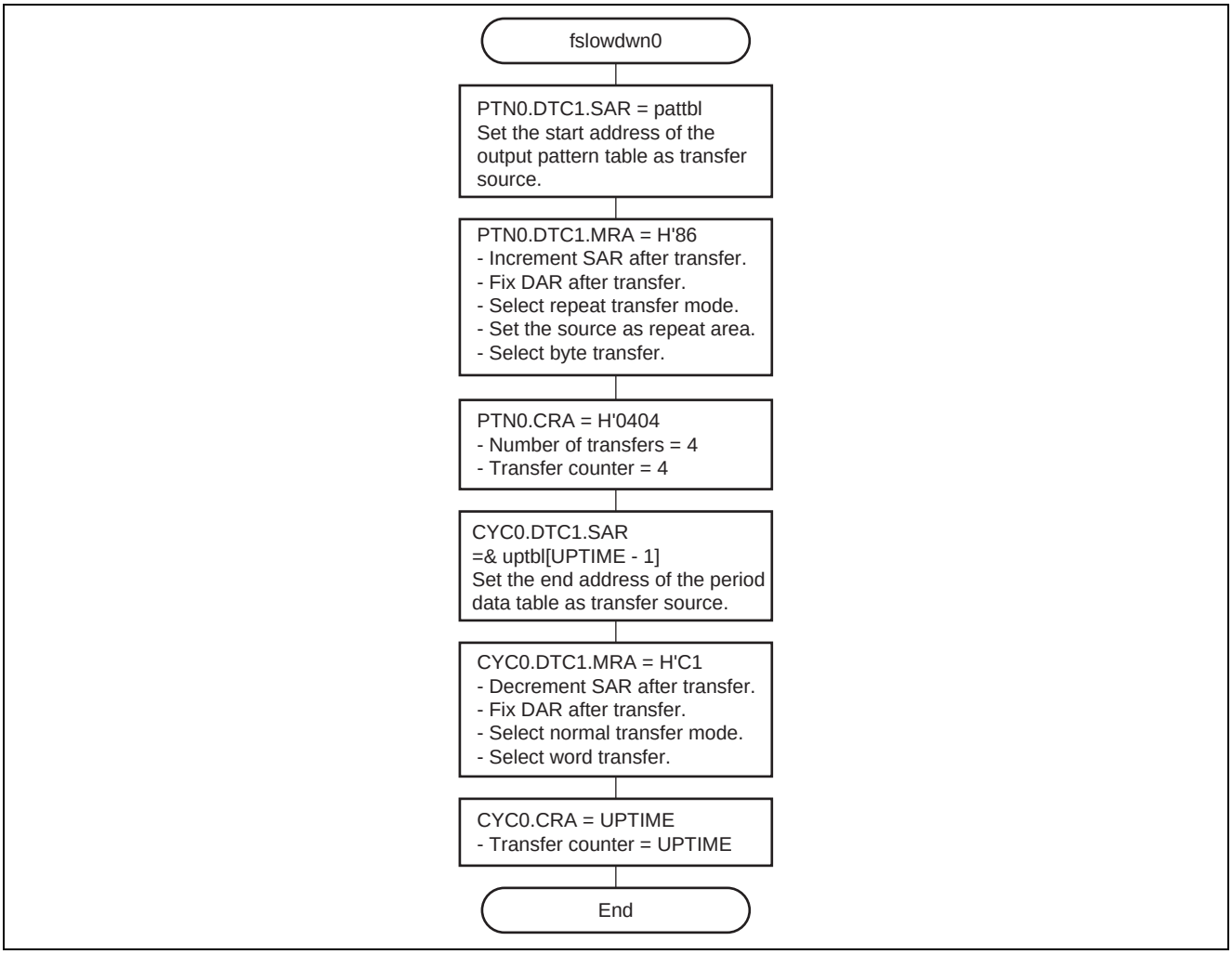
6.4 fslowup0 Function



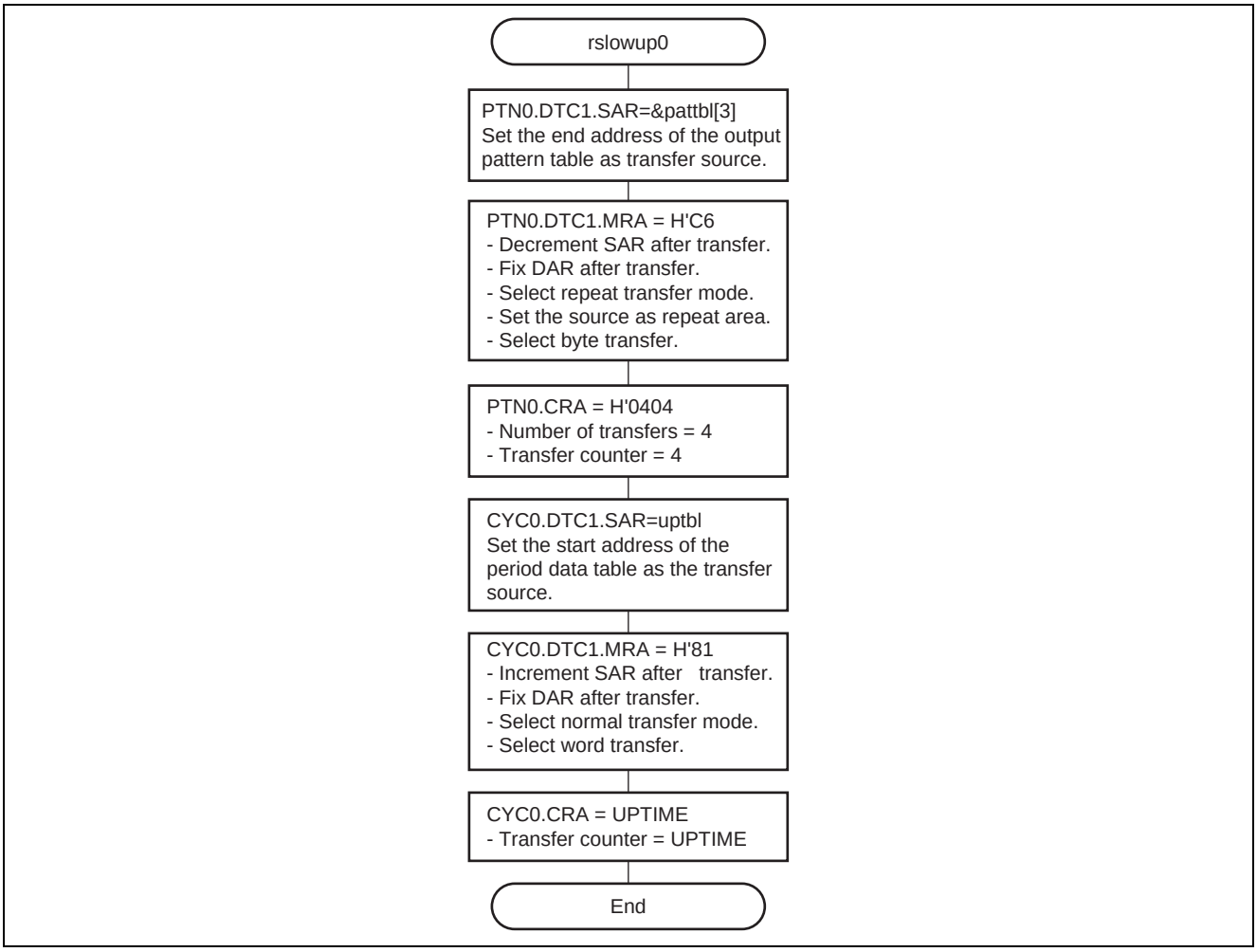
6.5 fconst0 Function



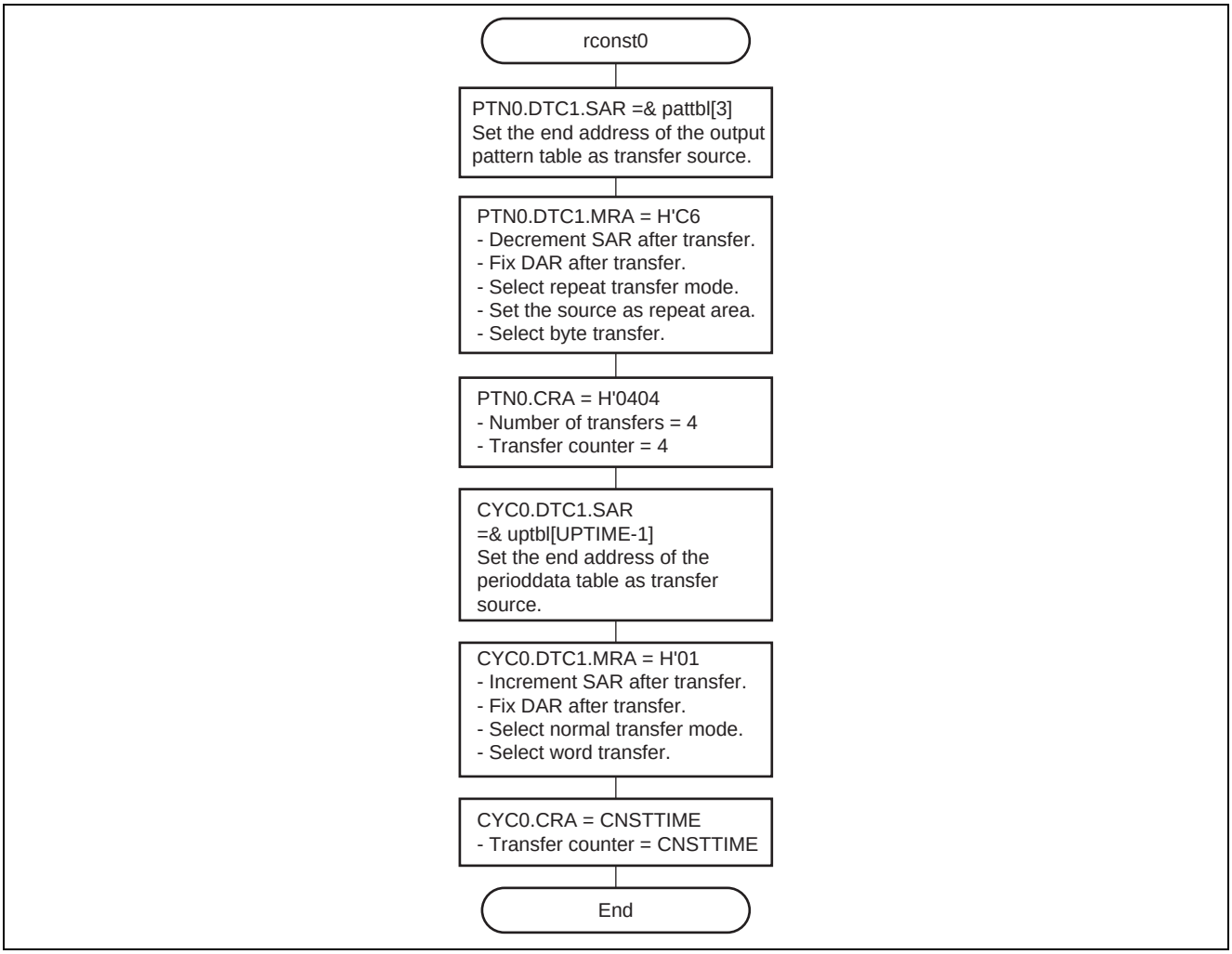
6.6 fslowdwn0 Function



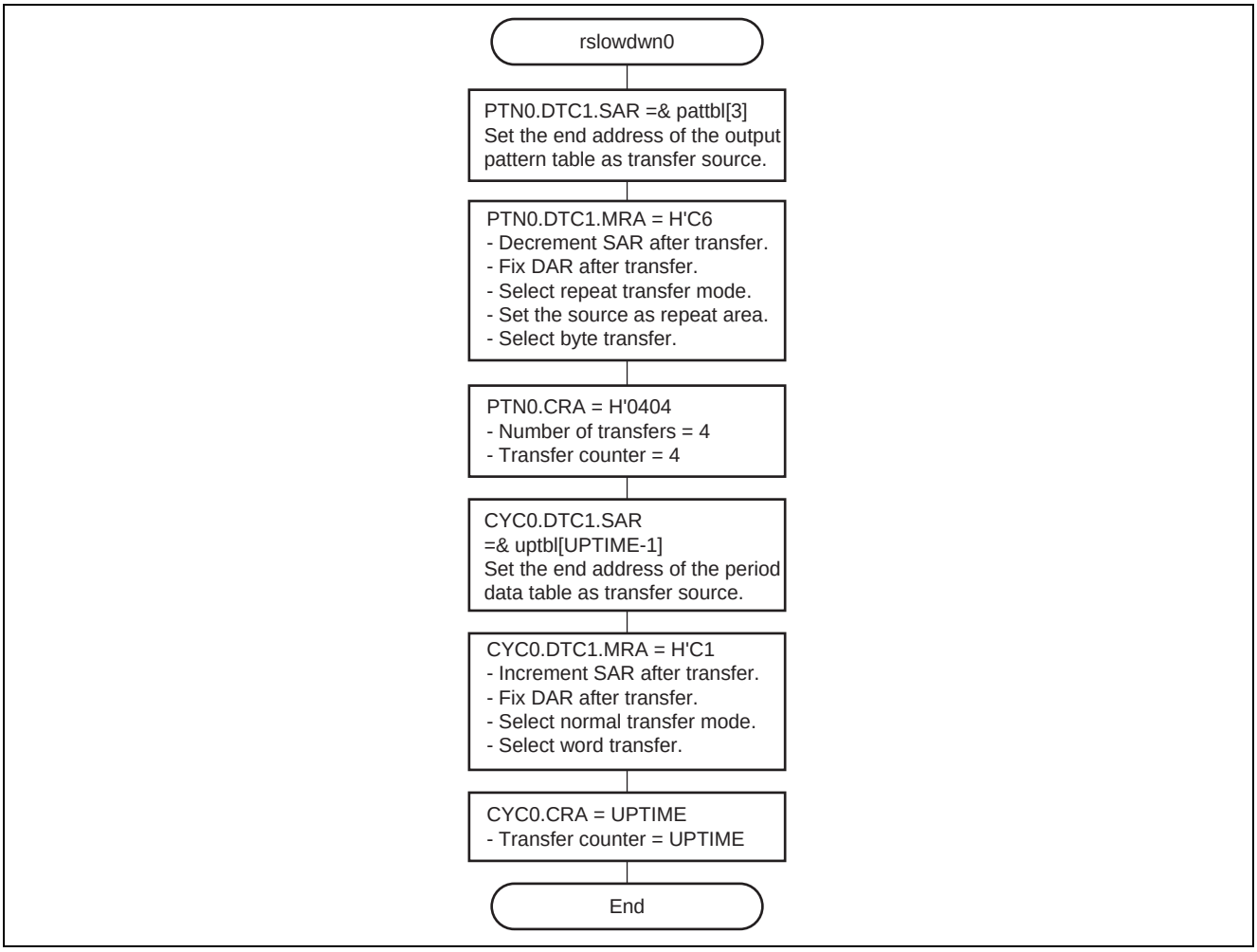
6.7 rslowup0 Function



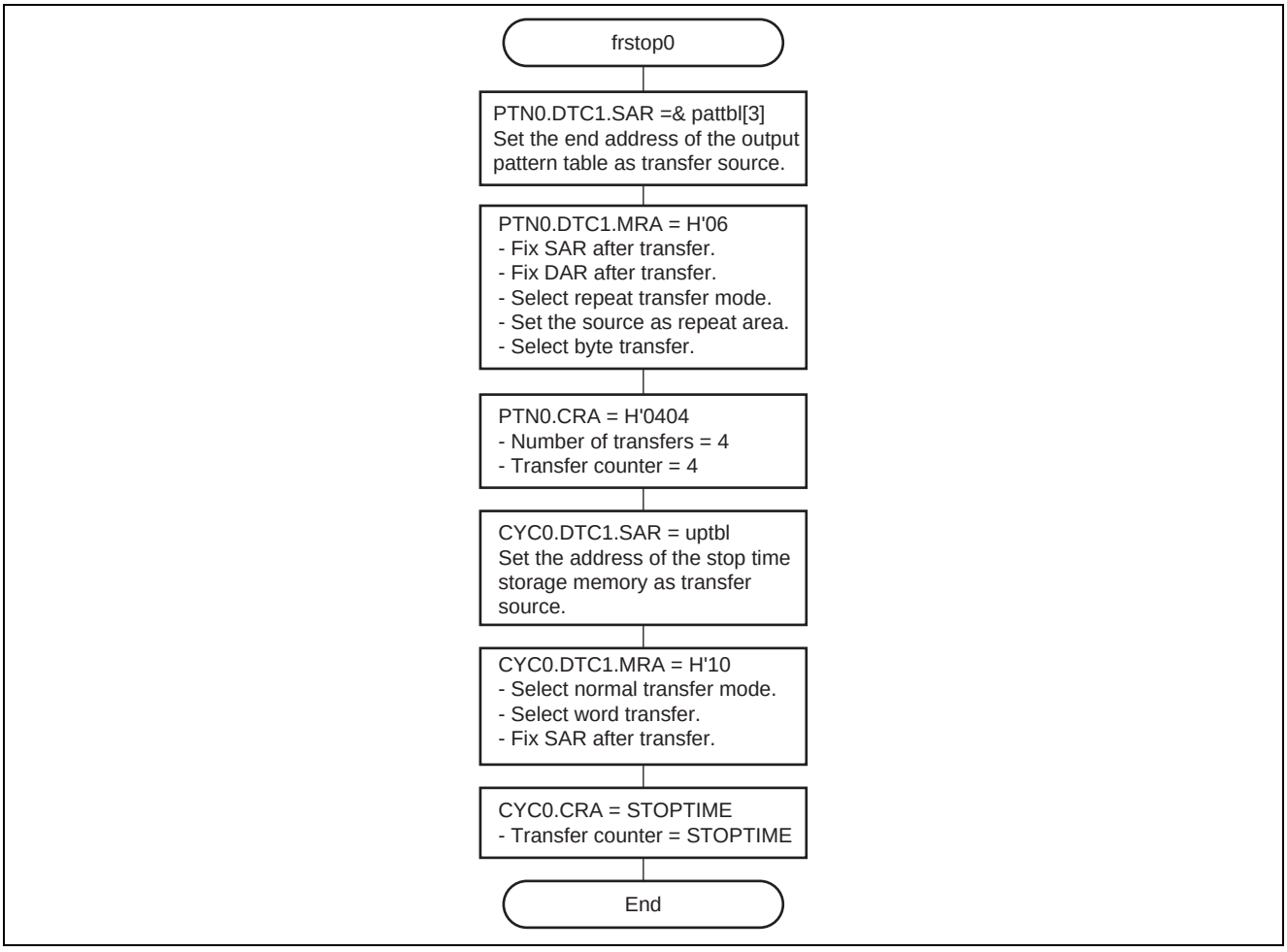
6.8 rconst0 Function



6.9 rslowdwn0 Function



6.10 frstop0 Function



Revision Record

		Description	
Rev.	Date	Page	Summary
1.00	Mar.09.05	—	First edition issued

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