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H8S Family

Outputting Four Groups of 4-Bit Signals

Introduction

Asynchronous pulses are output as four groups of 4-bit signals by using the programmable pulse generator (PPG) outputs.

Target Device

H8S/2377

Contents

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2. Applicable Conditions 3
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1. Specifications

- Asynchronous pulses are output as four groups of 4-bit signals by using the programmable pulse generator (PPG) outputs as shown in figure 1.
- The PPG is activated by compare match of the timer pulse unit (TPU).

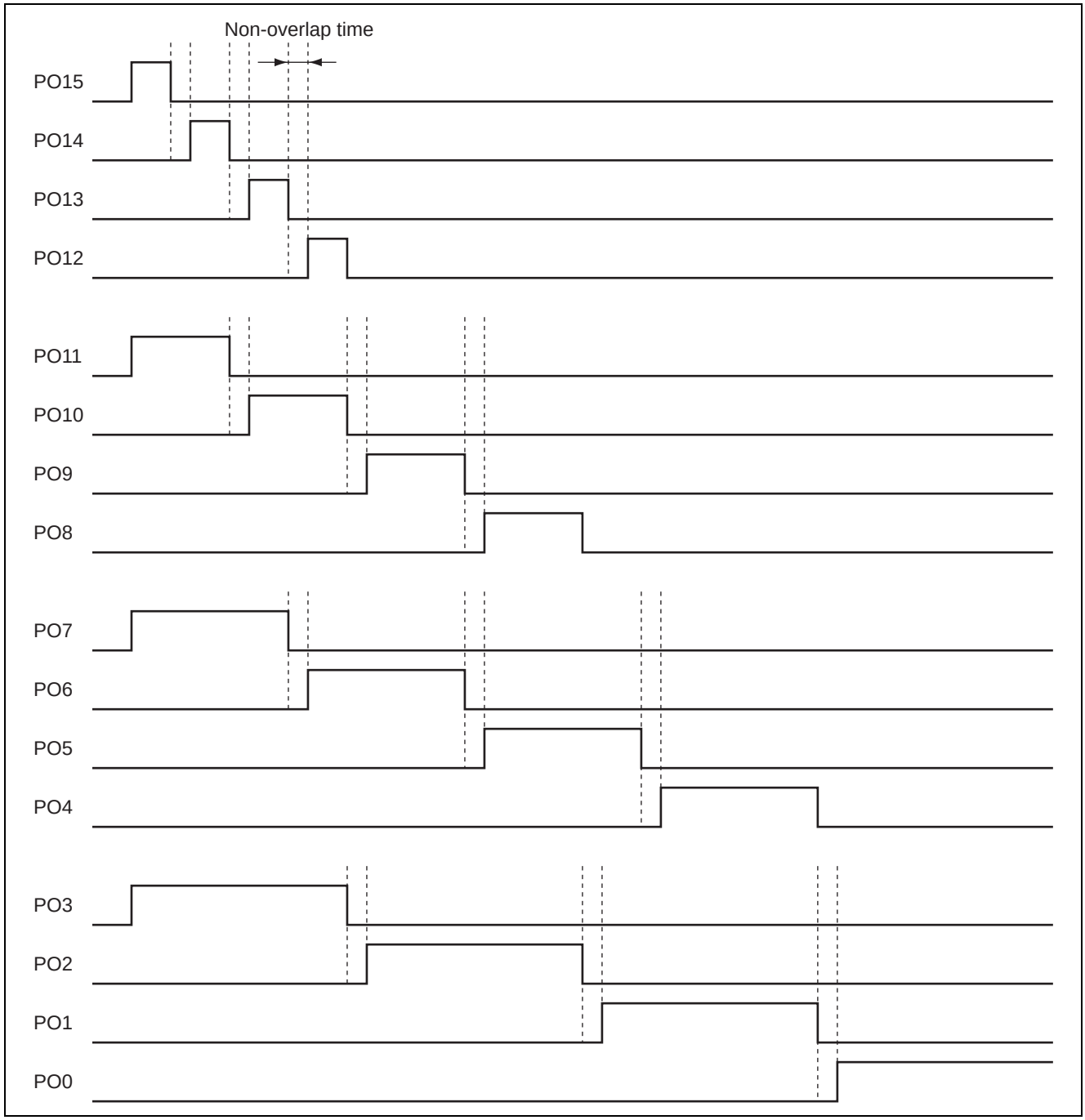


Figure 1 Example Output of Four Groups of 4-Bit Signals

2. Applicable Conditions

Table 1 Applicable Conditions

Item	Contents	
Operating frequency	Input clock:	19.6608 MHz
	System clock:	19.6608 MHz
	Peripheral module clock:	19.6608 MHz
	External bus clock:	19.6608 MHz
Operating mode	Mode 4 (MD2 = 1, MD1 = 0, MD0 = 0)	
Development tool	HEW Version 3.01.02	
C/C++ compiler	H8S, H8/300 SERIES C/C++ Compiler Version 6.00.02 (from Renesas Technology Corp.)	
Compile option	-cpu = 2000a:24, -code = machinecode, -optimize = 1, -regparam = 3 -speed = (register, shift, struct, expression)	

Table 2 Section Settings

Address	Section Name	Description
H'000000	CV1	Reset vector
H'0000A0	CV2	TPU TGI0A interrupt vector
H'0000C0	CV3	TPU TGI1A interrupt vector
H'0000D0	CV4	TPU TGI2A interrupt vector
H'0000E0	CV5	TPU TGI3A interrupt vector
H'001000	P	Program area
	C	Data table storage
H'FF7000	B	RAM area

3. Description of Functions

In this sample task, asynchronous pulses are output as four groups of 4-bit signals by using TPU0 to TPU3 and PPG output groups 3 to 0.

Figure 2 shows a block diagram for the pulse output generated using TPU3 and PPG group3 as an example. This sample task uses the following functions.

- An output trigger signal can be selected for each 4-bit group and up to four 4-bit groups can be output.
- An output trigger signal can be selected for each group from among compare-match signals on the four channels of the TPU.
- Non-overlap period can be set between the multiple pulse outputs.

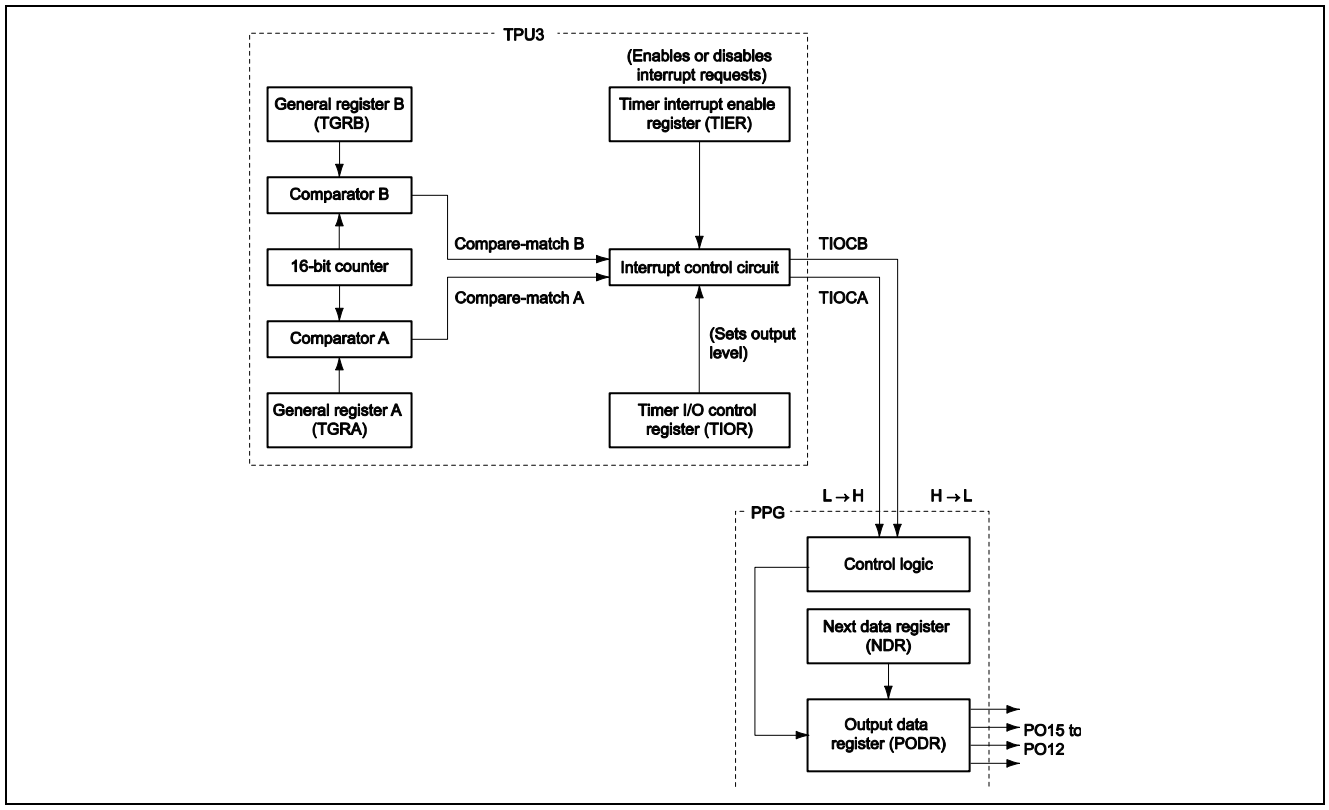


Figure 2 Block Diagram of Output of Four 4-Bit Signals (Group 3)

4. Description of Operation

Figure 3 illustrates the principles of data output operation using PPG output group 3. Four-phase non-overlapping output is generated through the hardware and software processing of the H8S/2377 as shown in figure 3.

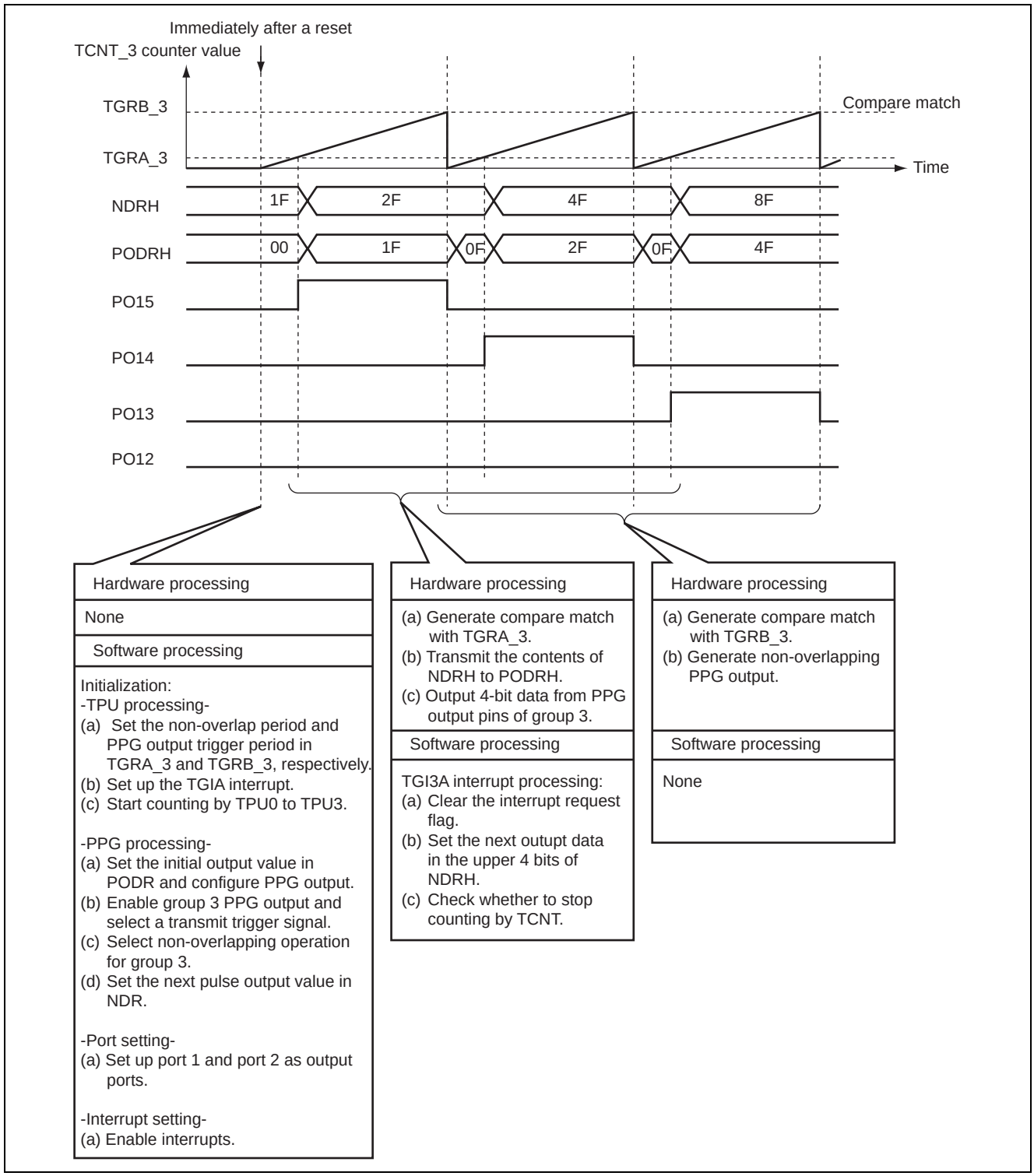


Figure 3 Output of Four 4-Bit Signals (Group 3)

5. Description of Software

5.1 List of Functions

Table 3 List of Functions

Function Name	Functions
init	Initialization routine Cancels module stop mode, sets the clock, and calls the main function.
main	Main routine Initializes the PPG and TPU.
tgi0a_int	Sets the data to be output next in the lower 4 bits of NDRL (group 0).
tgi1a_int	Sets the data to be output next in the upper 4 bits of NDRL (group 1).
tgi2a_int	Sets the data to be output next in the lower 4 bits of NDRH (group 2).
tgi3a_int	Sets the data to be output next in the upper 4 bits of NDRH (group 3).

5.2 Arguments

This sample task does not use arguments.

5.3 Internal Registers

The internal registers used in this sample task are described in table 4.

Table 4 Description of Internal Registers

Register Name		Function
PPG	P1DDR	Sets the P17 to P10 pins (corresponding to PO15 to PO8) as output pins.
	P2DDR	Sets the P27 to P20 pins (corresponding to PO7 to PO0) as output pins.
	P1DR	Stores output pattern data of PO15 to PO8.
	P2DR	Stores output pattern data of PO7 to PO0.
	PMR	Sets PO15 to PO0 as non-overlapping outputs.
	PCR	Selects a pulse output trigger signal for each group. Group 3: TPU3 compare match Group 2: TPU2 compare match Group 1: TPU1 compare match Group 0: TPU0 compare match
	NDERL	Enables PPG outputs of PO7 to PO0.
	NDERH	Enables PPG outputs of PO15 to PO8.
	NDRL	Sets the next pattern to be output as PO7 to PO0.
	NDRH	Sets the next pattern to be output as PO15 to PO0.
TPU	TGRA_0 to TGRA_3	These registers set non-overlap times.
	TGRB_0 to TGRB_3	These registers set PPG output trigger periods.
	TCR_0 to TCR_3	These registers are set such that the corresponding counters are cleared on compare match with TGRB, and counting is based on internal clock ϕ.
	TSR_0 to TSR_3	These registers indicate the occurrence of compare match.
	TIER_0 to TIER_3	These registers enable TGIA interrupts.
	TSTR	Enables counting by TCNT.
MSTPCRH, MSTPCRL EXMSTPCRH, EXMSTPCRL		These registers cancel module stop mode of all modules including the TPU and PPG.
SCKCR, PLLCR		These registers set the system-clock division ratio and the multiplication factor for the PLL circuit, respectively.

5.4 RAM Usage

Table 5 RAM Usage

Label Name	Description	Memory Size	Used In
cnt0	Transfer counter for PPG group 0 output	1 byte	main, tgi0a_int
cnt1	Transfer counter for PPG group 1 output	1 byte	main, tgi1a_int
cnt2	Transfer counter for PPG group 2 output	1 byte	main, tgi2a_int
cnt3	Transfer counter for PPG group 3 output	1 byte	main, tgi3a_int

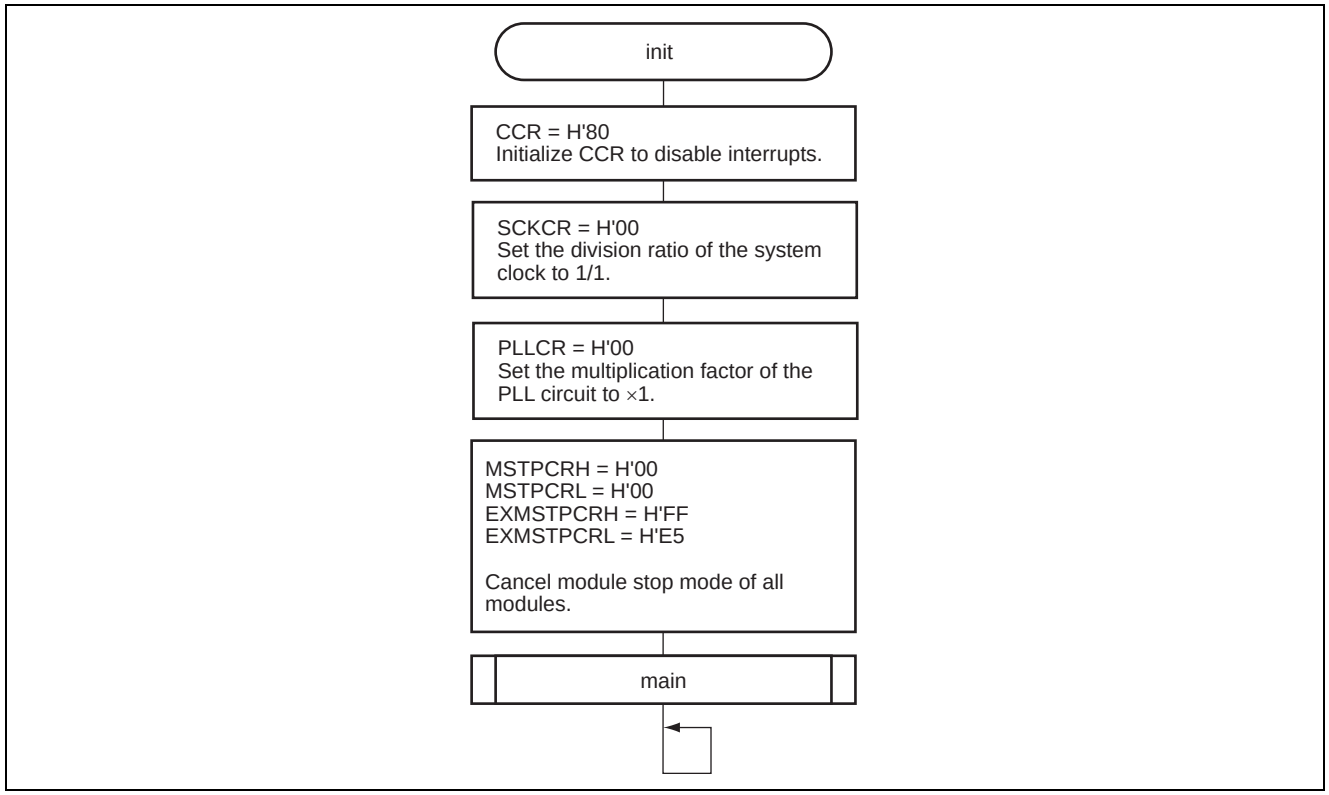
5.5 Data Table

Table 6 Description of Data Table

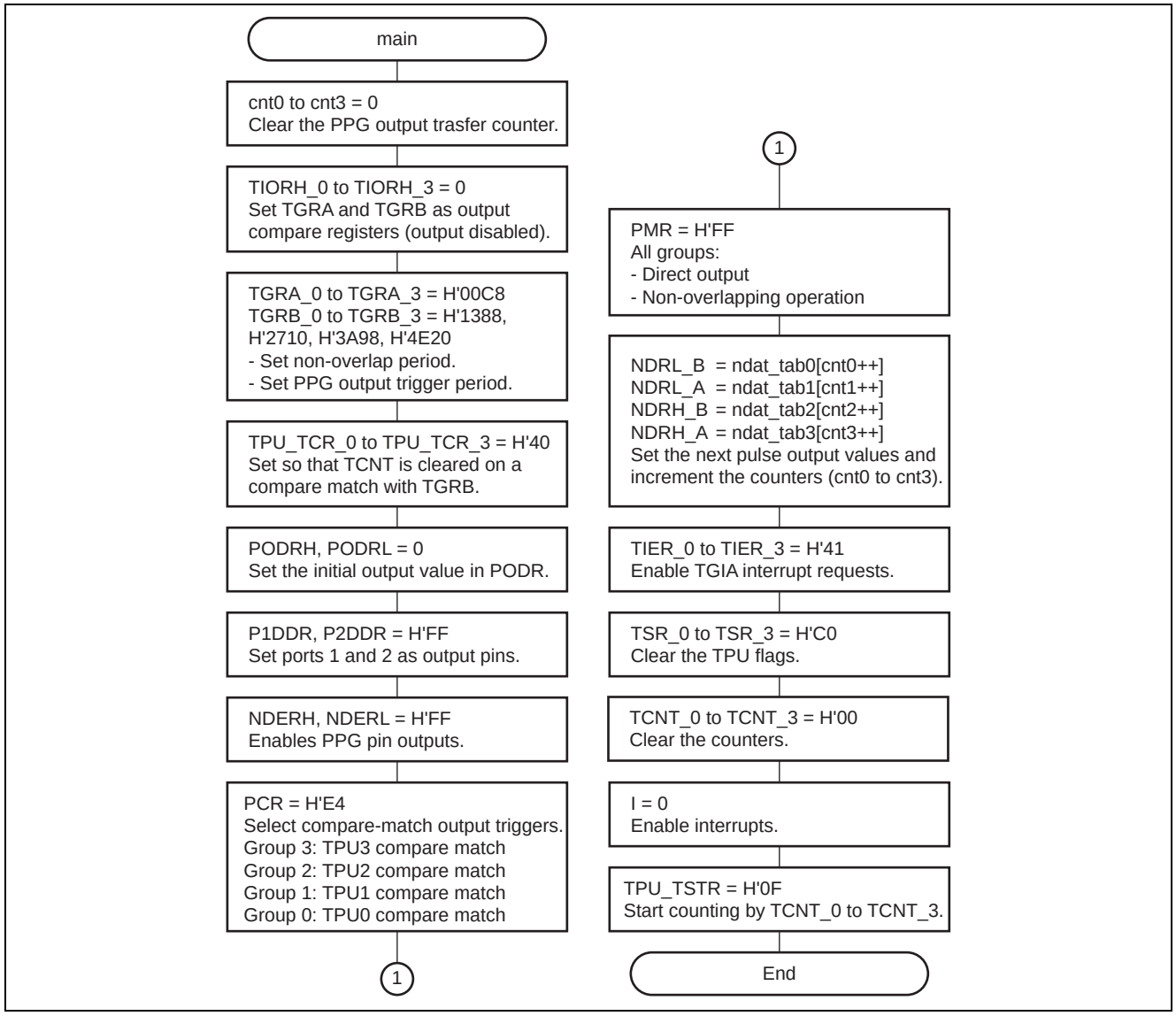
Label Name	Description	Memory Size	Used In
ndat_tab0	Stores data to be output from PPG group 0 {0xF1, 0xF2, 0xF4, 0xF8, 0xF0}	5 bytes	main, tgi0a_int
ndat_tab1	Stores data to be output from PPG group 1 {0x1F, 0x2F, 0x4F, 0x8F, 0x0F}	5 bytes	main, tgi1a_int
ndat_tab2	Stores data to be output from PPG group 2 {0xF1, 0xF2, 0xF4, 0xF8, 0xF0}	5 bytes	main, tgi2a_int
ndat_tab3	Stores data to be output from PPG group 3 {0x1F, 0x2F, 0x4F, 0x8F, 0x0F}	5 bytes	main, tgi3a_int

6. Flowchart

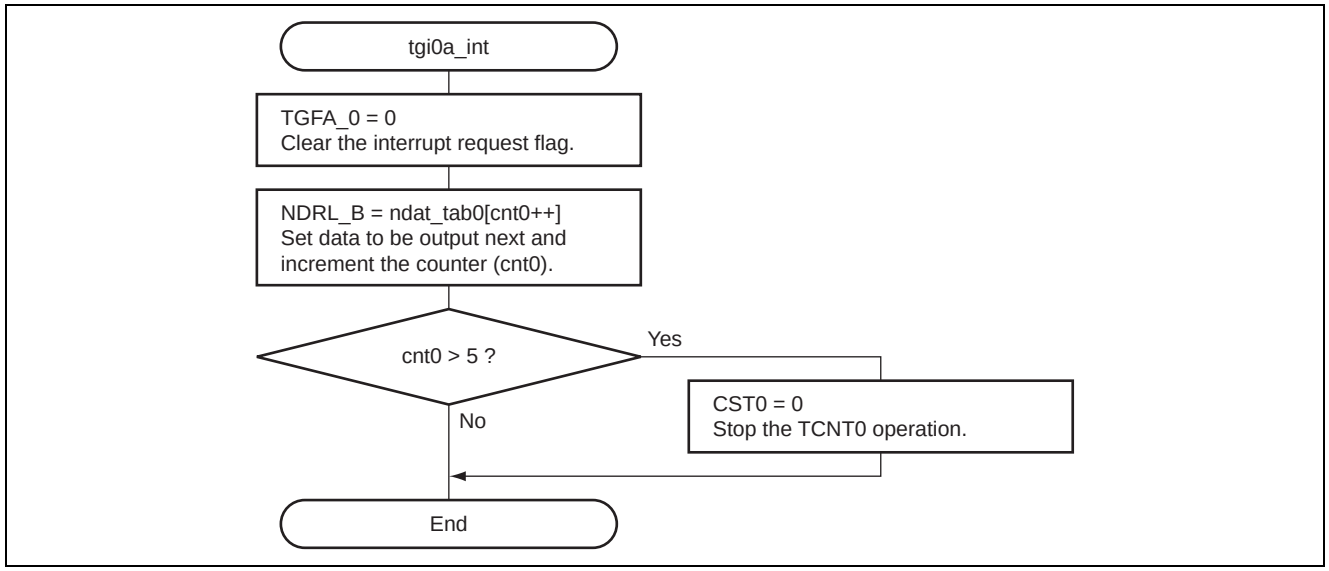
6.1 init Function



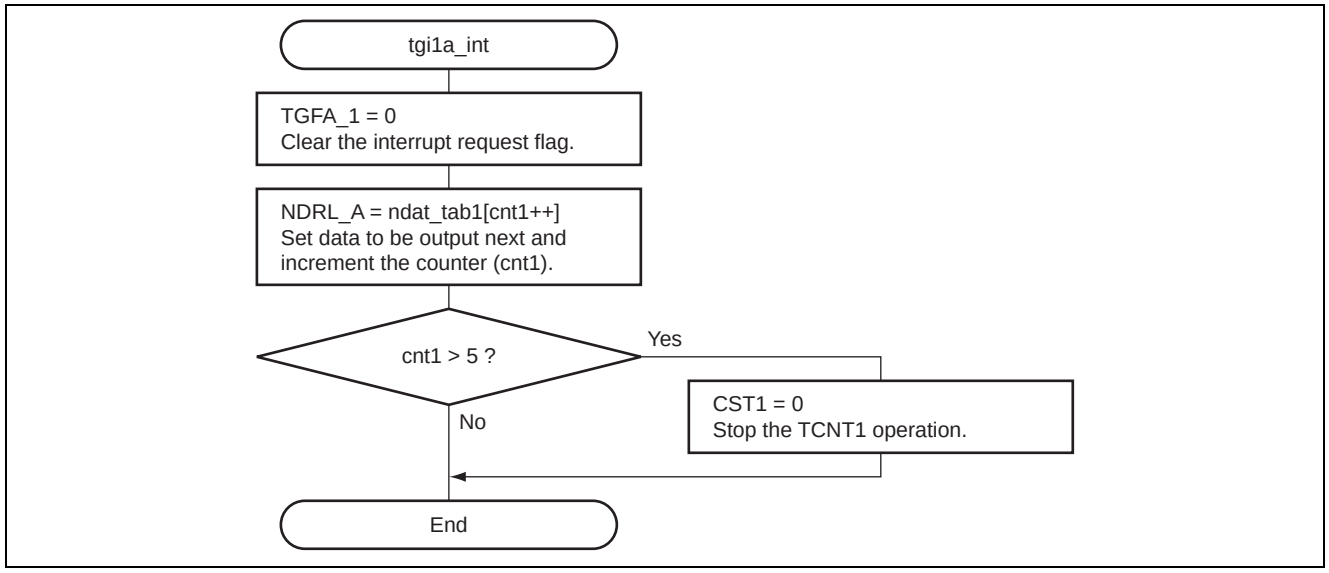
6.2 Main Function



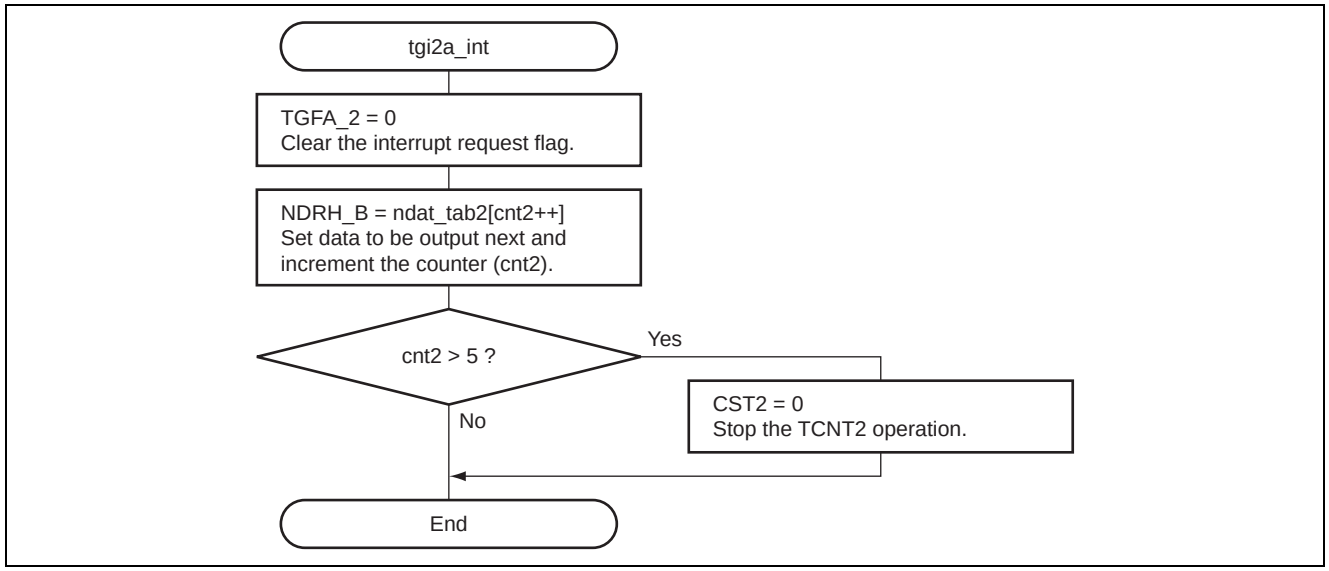
6.3 tgi0a_int Function



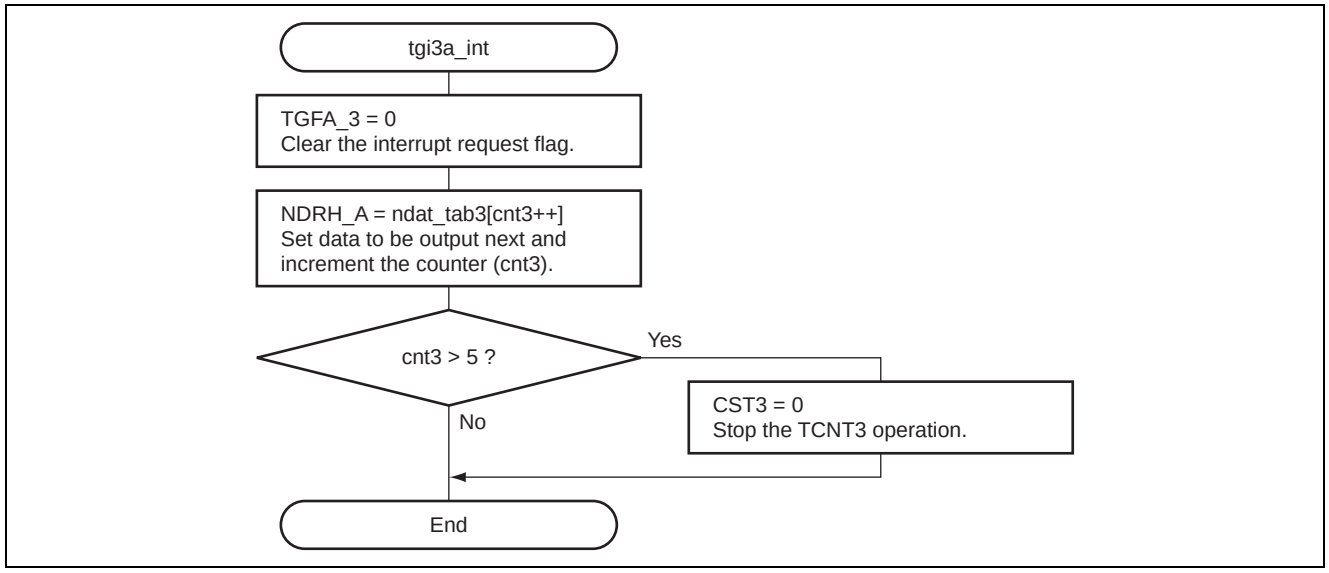
6.4 tgi1a_int Function



6.5 tgi2a_int Function



6.6 tgi3a_int Function



Revision Record

		Description	
Rev.	Date	Page	Summary
1.00	Mar.09.05	—	First edition issued

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