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Renesas Electronics Corporation

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H8S Family

High Speed Data Output

Introduction

12-bit data is output each time a rising edge of an external signal is detected.

Target Device

H8S/2377

Contents

1. Specifications

- An example of 12-bit data output is shown in figure 1.
- An external signal is input from the external clock D input pin (TCLKD).
- 12-bit data is output each time a rising edge of the external signal is detected.

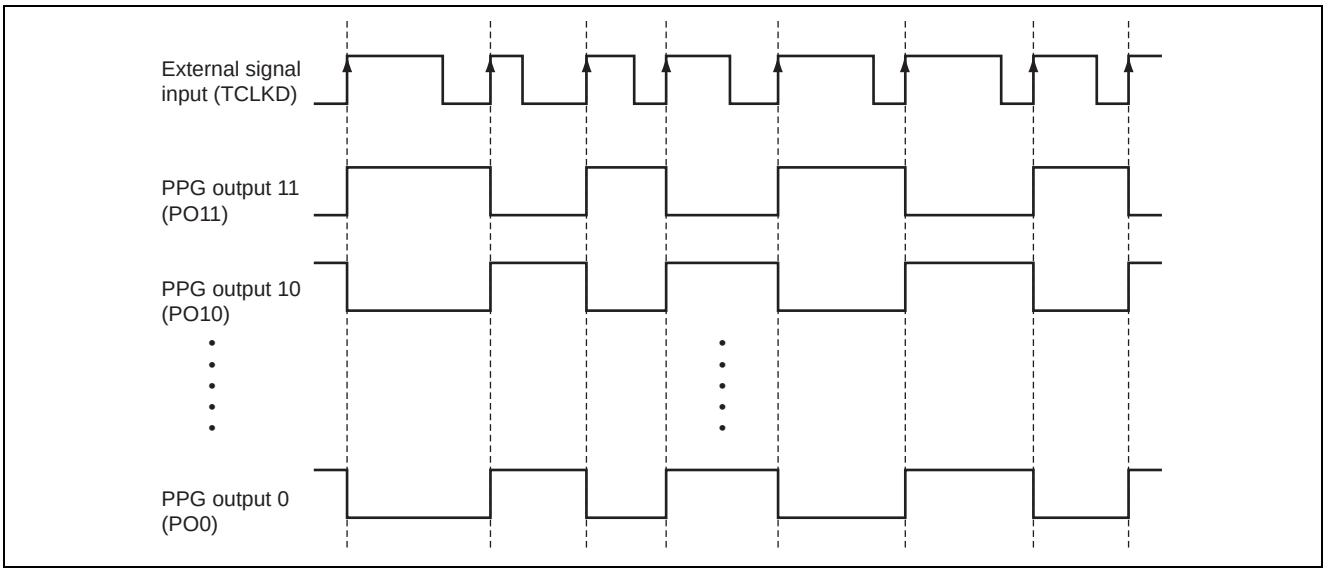


Figure 1 Example of 12-Bit Data Output

2. Applicable Conditions

Table 1 Applicable Conditions

Item	Contents
Operating frequency	Input clock: 19.6608 MHz System clock: 19.6608 MHz Peripheral module clock: 19.6608 MHz External bus clock: 19.6608 MHz
Operating mode	Mode 4 (MD2 = 1, MD1 = 0, MD0 = 0)
Development tool	HEW Version 3.01.02
C/C++ compiler	H8S, H8/300 SERIES C/C++ Compiler Version 6.00.02 (from Renesas Technology Corp.)
Compile option	-cpu = 2000a:24, -code = machinecode, -optimize = 1, -regparam = 3 -speed = (register, shift, struct, expression)

Table 2 Section Settings

Address	Section Name	Description
H'000000	CV1	Reset vector
H'000140	CV2	DMAC DMTEND0A interrupt vector
H'001000	P	Program area
	C	Data table
H'FF7000	B	RAM area

3. Description of Functions

Figure 2 shows a block diagram of the built-in functions used in this sample task. The functions of the H8S/2377 are used as described below to implement high-speed data output.

- Output Pattern Data Table
  Data patterns to be output from the programmable pattern generator (PPG) are store in ROM.
- Timer Pulse Unit (TPU0)
  Activates the DMAC0A and PPG each time compare-match A occurs.
  (TGRA is set to H'0000, and the counter is configured to be incremented on the rising edge of the external signal.)
- DMAC channel 0A (DMAC0A)
  Activated on compare-match A of the TPU0, and transfers the data in the output pattern data table to the NDR register.
- Programmable Pattern Generator (PPG)
  Activated on compare-match A of the TPU0 and outputs 12-bit data.

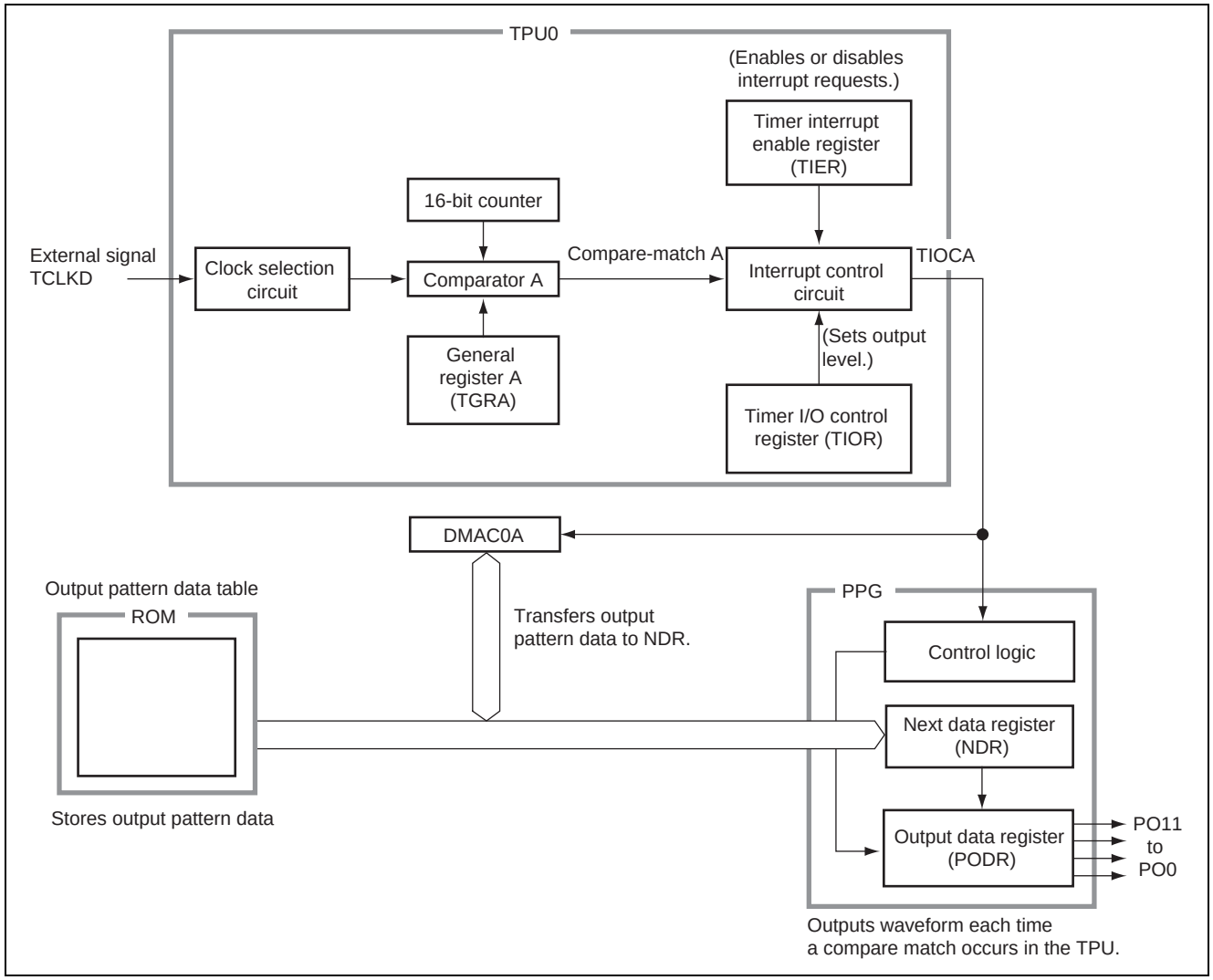


Figure 2 Block Diagram of High Speed Data Output

4. Description of Operation

Figure 3 shows the operation principle. This sample task performs high speed data output through the hardware and software processing shown in figure 3.

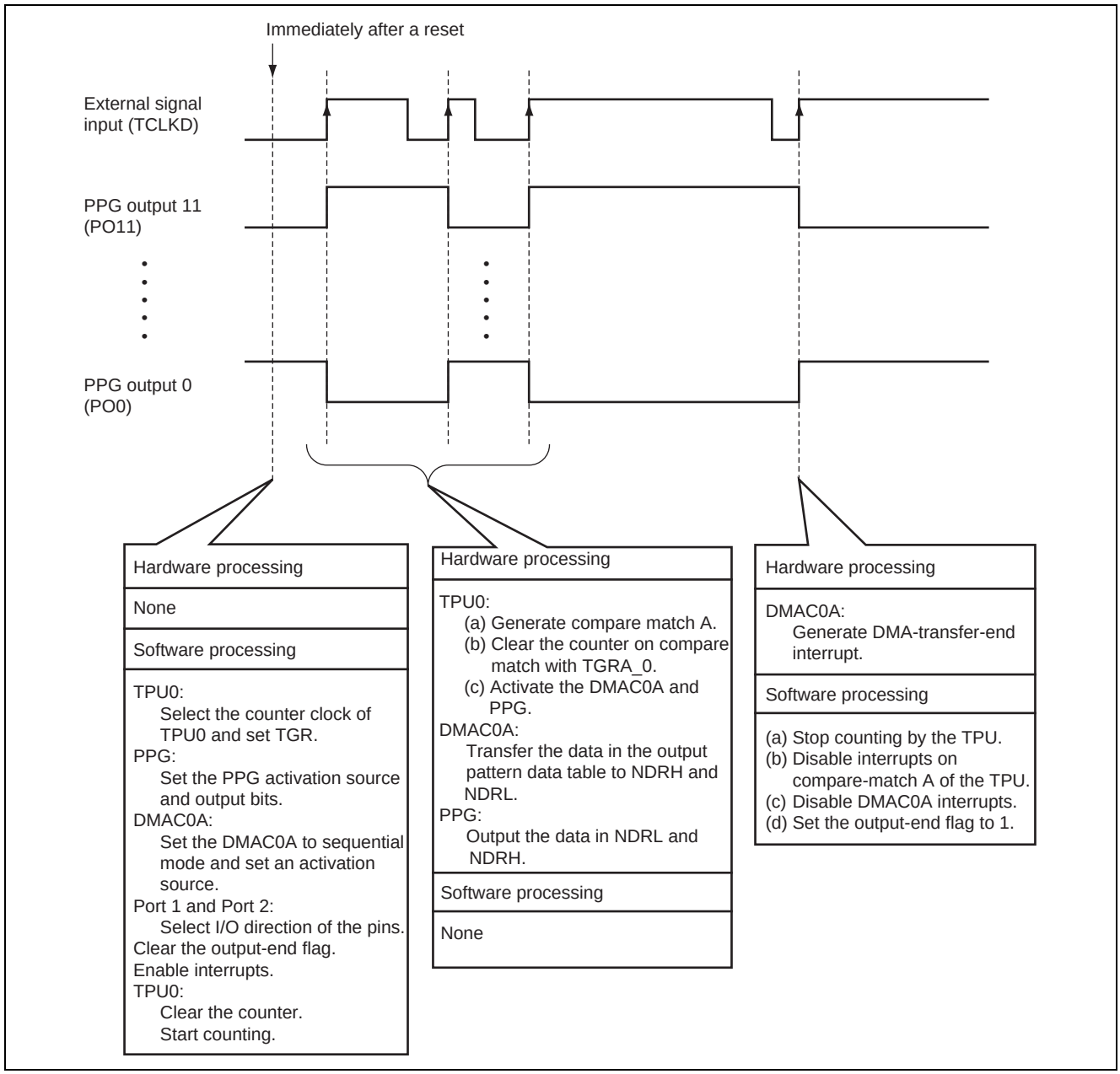


Figure 3 Operation Principle for High Speed Data Output

5. Description of Software

5.1 Functions

Table 3 describes the modules of this sample task.

Table 3 Functions

Function Name	Description
init	Initialization routine: Cancels module stop mode, sets the clock, and calls the main function.
main	Main routine: Initializes the TPU, PPG, and DMAC0A.
dmtend0a_int	DMA interrupt routine: Sets the output end flag.

5.2 Arguments

This sample program does not use arguments.

5.3 Internal Registers

The internal registers used in this sample task are described in table 4.

Table 4 Description of Internal Registers (1)

Register Name	Bit Name	Function
TPU0	TGRA_0	Sets output compare value (H'0000).
	TCR_0	Configures the TPU0 such that: the counter, TCNT_0, is cleared on compare match with TGRA_0; and the counter counts the rising edges of external signal on the TCLKD pin.
	TIOR_0	Specifies TGRA_0 as an output compare register and disables pin output.
	TIER_0	Enables a TGI0A interrupt.
	TSTR	Starts the TCNT_0 counting operation.
	TCNT_0	Counts the rising edges of the signal on the TCLKD pin.
PPG	PODRH	Stores output data for PO11 to PO8.
	PODRL	Stores output data for PO7 to PO0.
	PCR	Specifies the compare-match signal generated in the TPU0 as the output trigger for PO11 to PO0.
	NDERH	Enables the PO11 to PO8 PPG output.
	NDERL	Enables the PO7 to PO0 PPG output.
	NDRL	Stores the next output pattern data.
	NDRH	Stores the next output pattern data.

Register Name	Bit Name	Function
DMAC0A	DMACR0A	Sets data size to word. Sets MAR to increment. Sets data transfer mode to sequential mode. Sets an activation source to a compare-match A generated in the TPU0.
	DMABCRH DMABCRL	Enables or disables data transfer and the transfer end interrupt.
	MAR_0A	Sets the address of the output pattern data table as the transfer source address.
	IOAR_0A	Sets the address of the NDRH register as the transfer destination address.
	ETCR_0A	Sets the number of transfers.
MSTPCRH, MSTPCRL EXMSTPCRH, EXMSTPCRL		These registers cancel module stop mode of all modules including the TPU0, PPG, and DMAC0A.
SCKCR, PLLCR		These registers set the system-clock division ratio and the multiplication factor for the PLL circuit, respectively.

5.4 RAM Usage

Table 5 describes the RAM usage in this sample task.

Table 5 Description of RAM

Label Name	Description	Memory Size	Used In
dma_f	Flag that indicates whether the output of all 12-bit data has been completed. 0: The output of 12-bit data is in progress. 1: The output of all 12-bit data has been completed.	1 byte	main, dmtend0a_int

5.5 Data Table

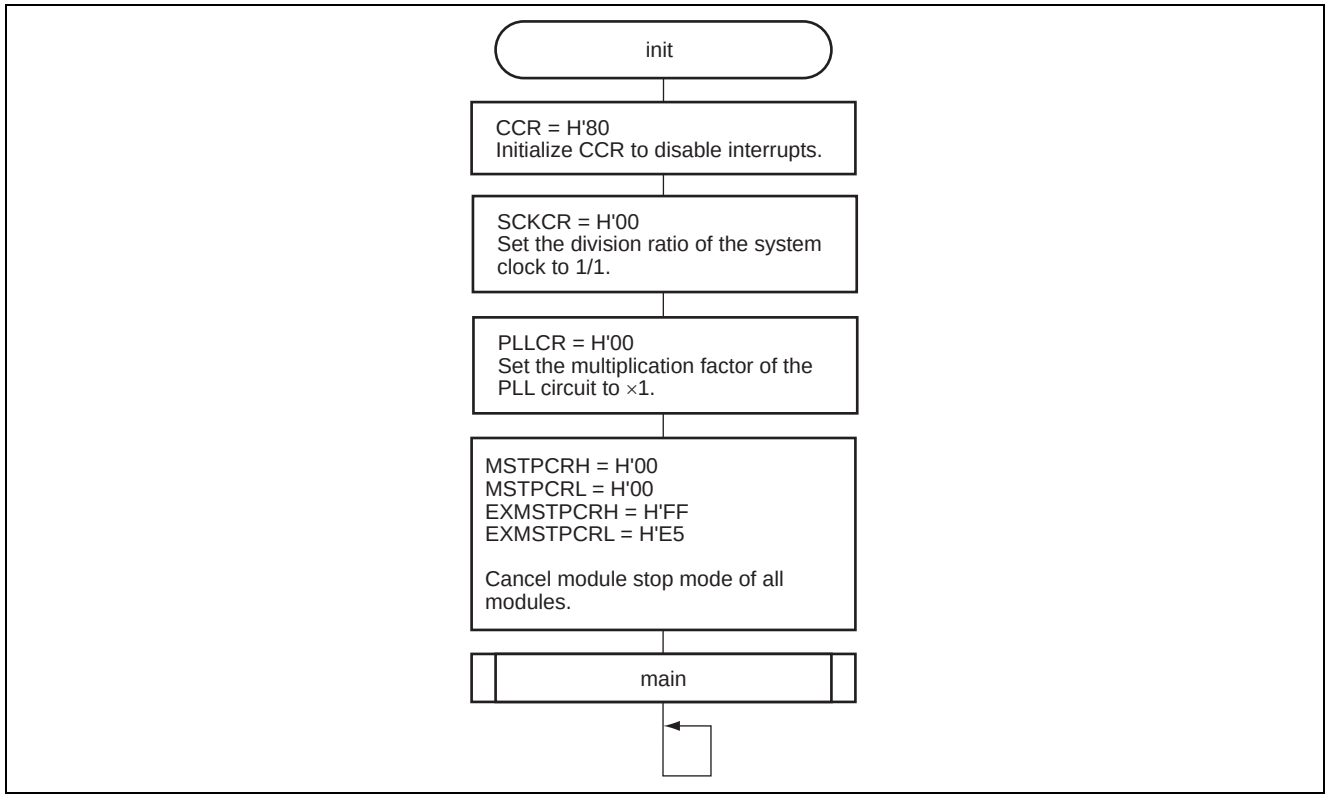
Table 6 describes the data table used in this sample task.

Table 6 Description of Data Table

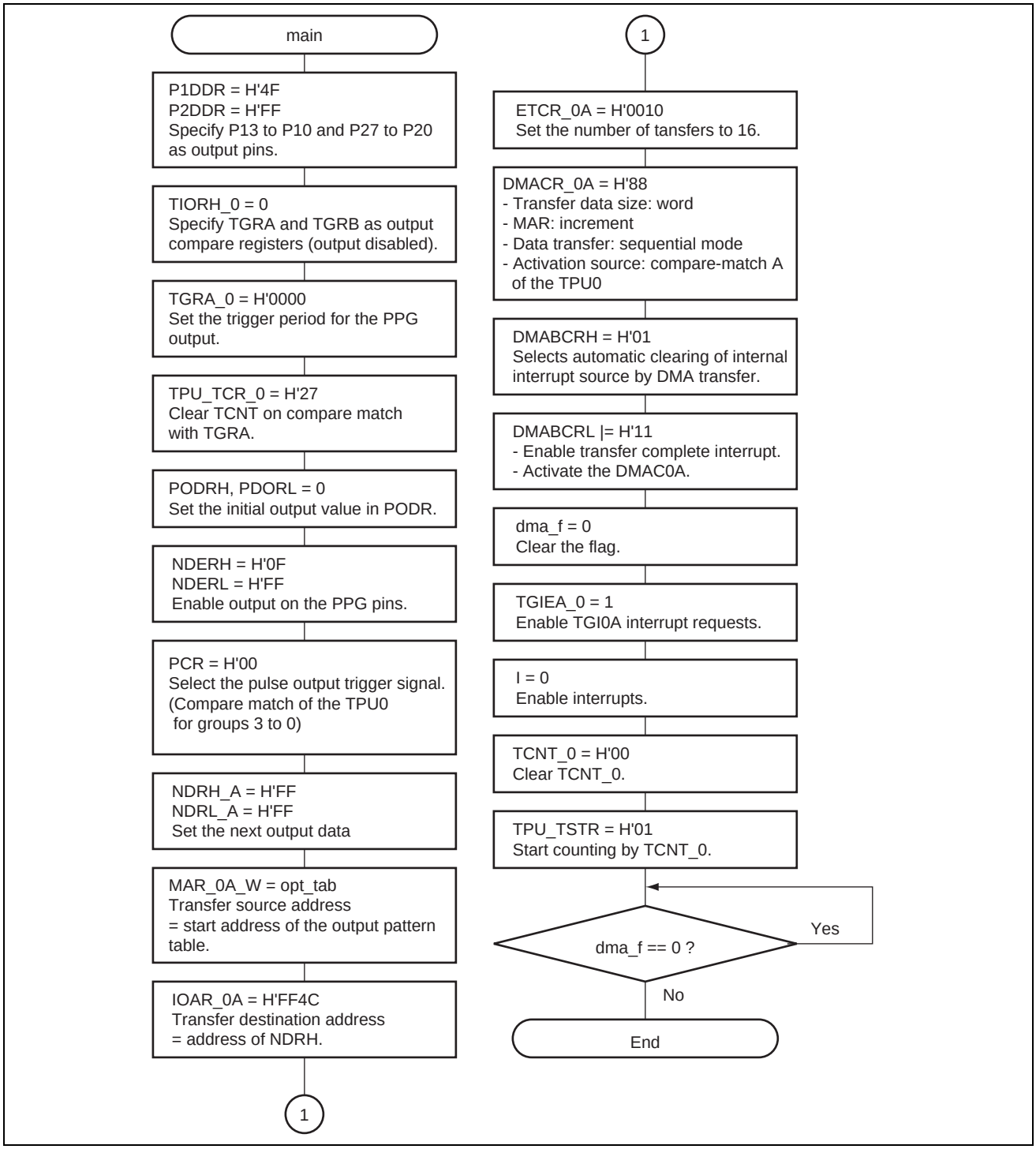
Label Name	Description	Memory Size	Used In
opat_tab	Output pattern data table Stores data to be output from the PPG.	32 bytes	main

6. Flowchart

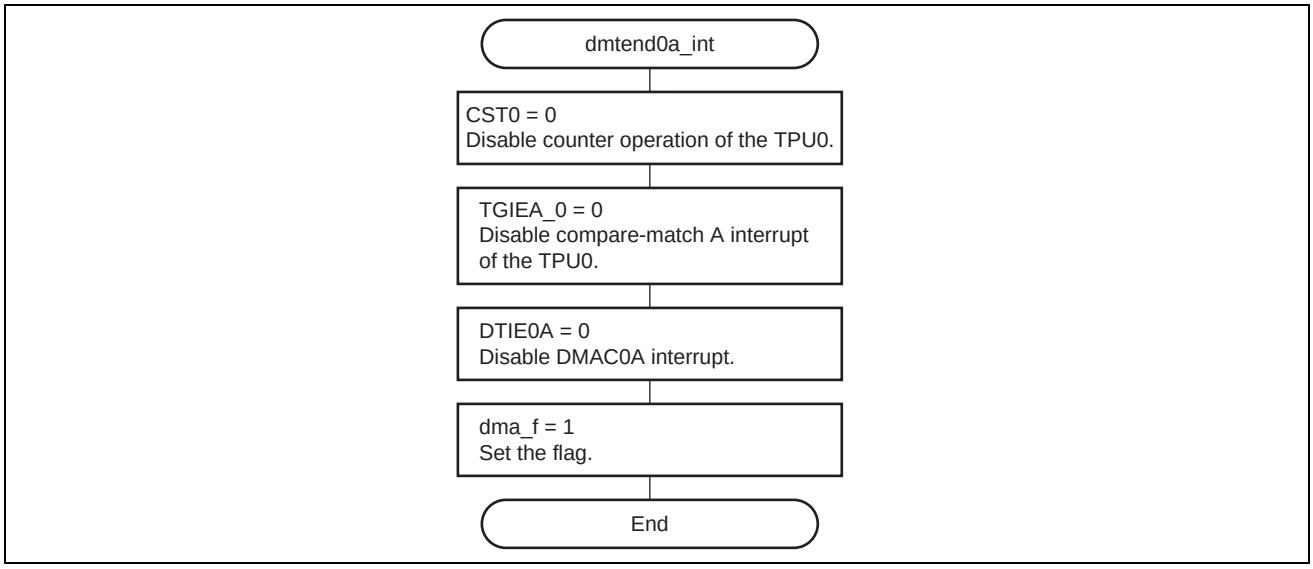
6.1 init Function



6.2 Main Function



6.3 Dmtend0a_int Function



Revision Record

Rev.	Date	Description	
		Page	Summary
1.00	Mar.09.05	—	First edition issued

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