To our customers,

Old Company Name in Catalogs and Other Documents

On April 1st, 2010, NEC Electronics Corporation merged with Renesas Technology Corporation, and Renesas Electronics Corporation took over all the business of both companies. Therefore, although the old company name remains in this document, it is a valid Renesas Electronics document. We appreciate your understanding.

Renesas Electronics website: http://www.renesas.com

April 1st, 2010
Renesas Electronics Corporation

Issued by: Renesas Electronics Corporation (http://www.renesas.com)

Send any inquiries to http://www.renesas.com/inquiry.

Notice

1. All information included in this document is current as of the date this document is issued. Such information, however, is subject to change without any prior notice. Before purchasing or using any Renesas Electronics products listed herein, please confirm the latest product information with a Renesas Electronics sales office. Also, please pay regular and careful attention to additional and different information to be disclosed by Renesas Electronics such as that disclosed through our website.
2. Renesas Electronics does not assume any liability for infringement of patents, copyrights, or other intellectual property rights of third parties by or arising from the use of Renesas Electronics products or technical information described in this document. No license, express, implied or otherwise, is granted hereby under any patents, copyrights or other intellectual property rights of Renesas Electronics or others.
3. You should not alter, modify, copy, or otherwise misappropriate any Renesas Electronics product, whether in whole or in part.
4. Descriptions of circuits, software and other related information in this document are provided only to illustrate the operation of semiconductor products and application examples. You are fully responsible for the incorporation of these circuits, software, and information in the design of your equipment. Renesas Electronics assumes no responsibility for any losses incurred by you or third parties arising from the use of these circuits, software, or information.
5. When exporting the products or technology described in this document, you should comply with the applicable export control laws and regulations and follow the procedures required by such laws and regulations. You should not use Renesas Electronics products or the technology described in this document for any purpose relating to military applications or use by the military, including but not limited to the development of weapons of mass destruction. Renesas Electronics products and technology may not be used for or incorporated into any products or systems whose manufacture, use, or sale is prohibited under any applicable domestic or foreign laws or regulations.
6. Renesas Electronics has used reasonable care in preparing the information included in this document, but Renesas Electronics does not warrant that such information is error free. Renesas Electronics assumes no liability whatsoever for any damages incurred by you resulting from errors in or omissions from the information included herein.
7. Renesas Electronics products are classified according to the following three quality grades: "Standard", "High Quality", and "Specific". The recommended applications for each Renesas Electronics product depends on the product's quality grade, as indicated below. You must check the quality grade of each Renesas Electronics product before using it in a particular application. You may not use any Renesas Electronics product for any application categorized as "Specific" without the prior written consent of Renesas Electronics. Further, you may not use any Renesas Electronics product for any application for which it is not intended without the prior written consent of Renesas Electronics. Renesas Electronics shall not be in any way liable for any damages or losses incurred by you or third parties arising from the use of any Renesas Electronics product for an application categorized as "Specific" or for which the product is not intended where you have failed to obtain the prior written consent of Renesas Electronics. The quality grade of each Renesas Electronics product is "Standard" unless otherwise expressly specified in a Renesas Electronics data sheets or data books, etc.

   "Standard": Computers; office equipment; communications equipment; test and measurement equipment; audio and visual equipment; home electronic appliances; machine tools; personal electronic equipment; and industrial robots.

   "High Quality": Transportation equipment (automobiles, trains, ships, etc.); traffic control systems; anti-disaster systems; anti-crime systems; safety equipment; and medical equipment not specifically designed for life support.

   "Specific": Aircraft; aerospace equipment; submersible repeaters; nuclear reactor control systems; medical equipment or systems for life support (e.g. artificial life support devices or systems), surgical implantations, or healthcare intervention (e.g. excision, etc.), and any other applications or purposes that pose a direct threat to human life.
8. You should use the Renesas Electronics products described in this document within the range specified by Renesas Electronics, especially with respect to the maximum rating, operating supply voltage range, movement power voltage range, heat radiation characteristics, installation and other product characteristics. Renesas Electronics shall have no liability for malfunctions or damages arising out of the use of Renesas Electronics products beyond such specified ranges.
9. Although Renesas Electronics endeavors to improve the quality and reliability of its products, semiconductor products have specific characteristics such as the occurrence of failure at a certain rate and malfunctions under certain use conditions. Further, Renesas Electronics products are not subject to radiation resistance design. Please be sure to implement safety measures to guard them against the possibility of physical injury, and injury or damage caused by fire in the event of the failure of a Renesas Electronics product, such as safety design for hardware and software including but not limited to redundancy, fire control and malfunction prevention, appropriate treatment for aging degradation or any other appropriate measures. Because the evaluation of microcomputer software alone is very difficult, please evaluate the safety of the final products or system manufactured by you.
10. Please contact a Renesas Electronics sales office for details as to environmental matters such as the environmental compatibility of each Renesas Electronics product. Please use Renesas Electronics products in compliance with all applicable laws and regulations that regulate the inclusion or use of controlled substances, including without limitation, the EU RoHS Directive. Renesas Electronics assumes no liability for damages or losses occurring as a result of your noncompliance with applicable laws and regulations.
11. This document may not be reproduced or duplicated, in any form, in whole or in part, without prior written consent of Renesas Electronics.
12. Please contact a Renesas Electronics sales office if you have any questions regarding the information contained in this document or Renesas Electronics products, or if you have any other inquiries.

(Note 1) "Renesas Electronics" as used in this document means Renesas Electronics Corporation and also includes its majority-owned subsidiaries.

(Note 2) "Renesas Electronics product(s)" means any product developed or manufactured by or for Renesas Electronics.

H8/38602R Group

Clocked Synchronous Communication Mode of SSU

Introduction

This application note discusses communication by the synchronous serial communication unit (SSU) in clocked synchronous communication mode.

Target Device

H8/38602R

Contents

1. Specifications

- As shown in figure 1, the H8/38602R performs communication by the SSU in clocked synchronous communication mode.
- In this sample task, the master device transmits four-byte data, and the slave device receives it. The slave device transmits the received four-byte data back to the master device, and the master device receives it.
- In this sample task, the transfer clock rate is $\phi/8$ (ϕ = 10 [MHz]).

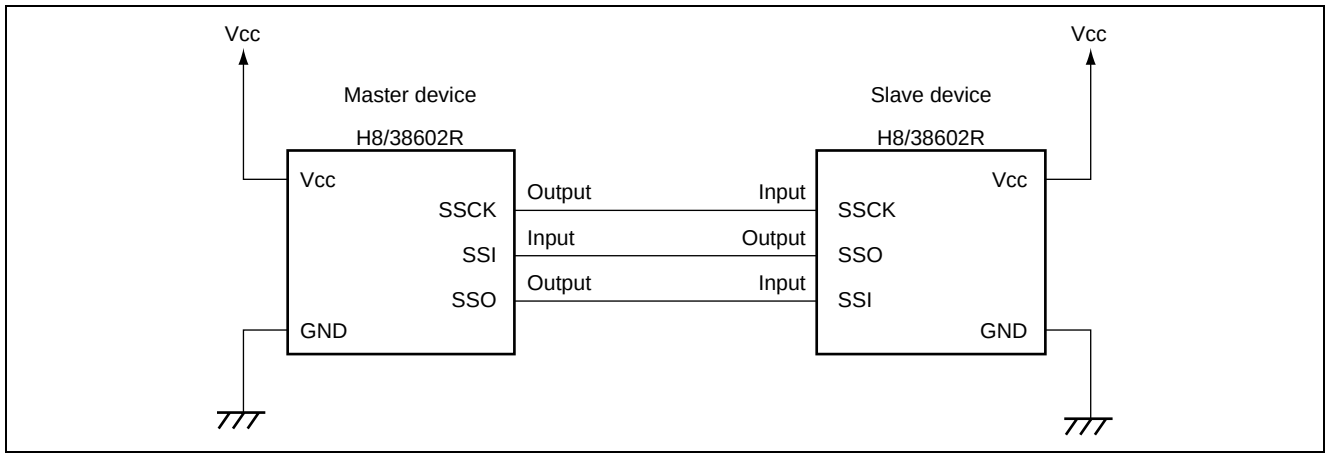


Figure 1 Connections in Clocked Synchronous Communication Mode of SSU

2. Description of Functions

2.1 Functions

This sample task implements communication by the SSU in clocked synchronous communication mode. Figure 2 shows a block diagram of the SSU when it configured for clocked synchronous communication mode, and below is the functional explanation.

2.1.1 Functions of SSU in Clocked Synchronous Communication Mode

The master device transmits four-byte data, and the slave device receives it. The slave device transmits the received four-byte data back to the master device, and the master device receives it. The transfer clock rate is $\phi/8$ (ϕ = 10 [MHz]).

- SS Control Register H (SSCRH)
  SSCRH is a register that selects whether the SSU operates as a master or slave device, and selects the SSCK pin function.
- SS Control Register L (SSCRL)
  SSCRL is a register that selects the operating mode of the SSU.
- SS Mode Register (SSMR)
  SSMR is a register that selects MSB-first or LSB-first, and selects transfer clock rate.
- SS Enable Register (SSER)
  SSER is a register that enables transmit or receive operation.
- SS Status Register (SSSR)
  SSSR is a register that consists of interrupt flags.
- SS Receive Data Register (SSRDR)
  SSRDR is an 8-bit register that stores received serial data. When the SSU has received one byte of serial data, it transfers the data from SSTRSR to SSRDR. The SSTRSR is then ready to receive the next byte. This double-buffered configuration of SSTRSR and SSRDR allows continuous receive operation. SSRDR is a read-only register and cannot be written to by the CPU. The initial value of SSRDR is H'00.
- SS Transmit Data Register (SSTDR)
  SSTDR is an 8-bit register that stores serial data to be transmitted. SSTDR can be read or written to by the CPU at any time. When the SSU detects that SSTRSR is empty, it transfers the transmit data stored in SSTDR to SSTRSR and then starts serial transmission. By writing the next transmit data to SSTDR during serial transmission of the data in SSTRSR, continuous serial transmission is possible. The initial value of SSTDR is H'00.
- SS Shift Register (SSTRSR)
  SSTRSR is a shift register used to transmit and receive serial data. When transmit data is transferred from SSTDR to SSTRSR, bit 0 in SSTDR is transferred to bit 0 in SSTRSR if the MLS bit in SSMR is 0 (LSB-first transfer), and bit 7 in SSTDR is transferred to bit 0 in SSTRSR if the MLS bit is 1 (MSB-first transfer). SSTRSR cannot be directly accessed by the CPU.

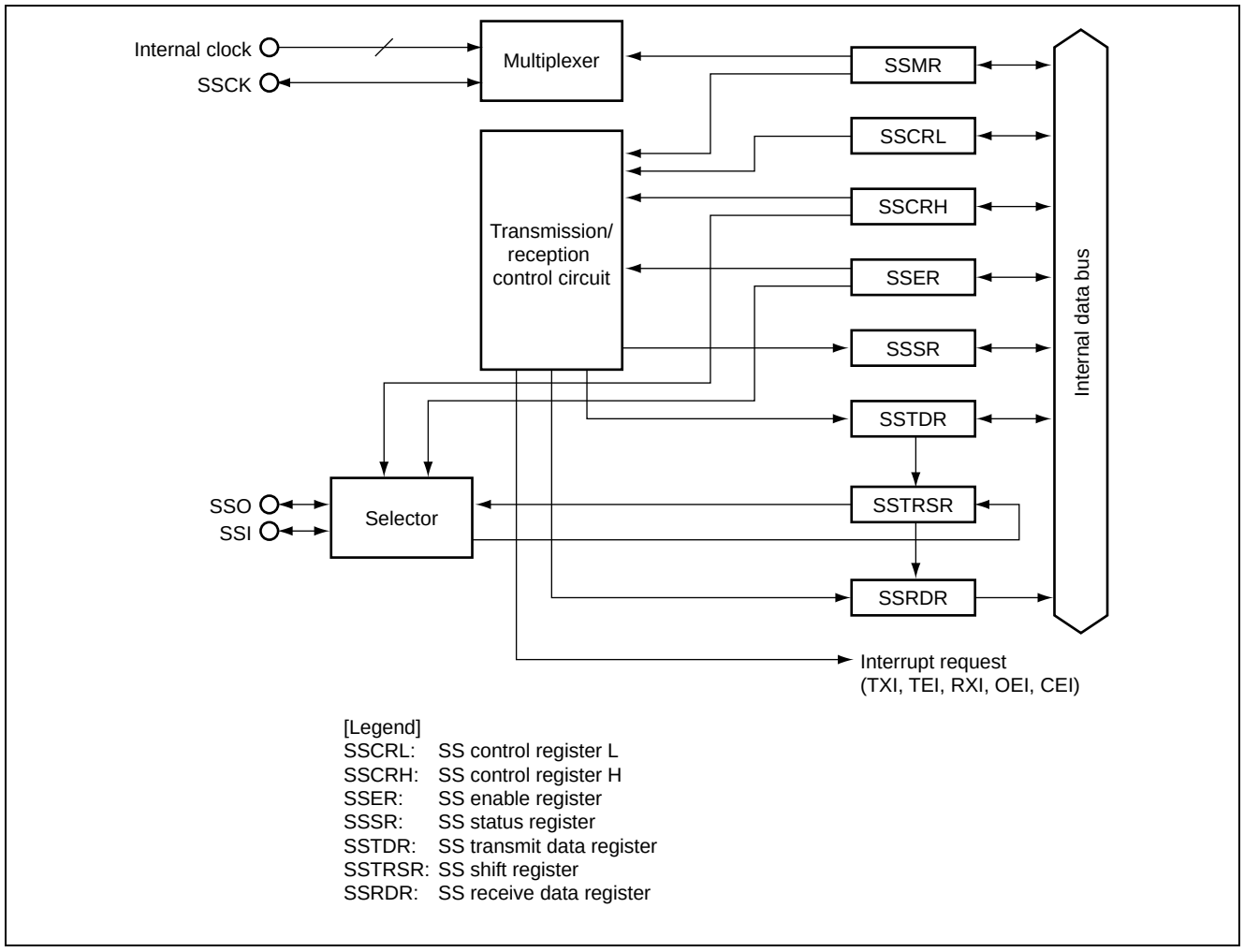


Figure 2 Block Diagram in Clocked Synchronous Communication Mode of SSU

2.1.2 Watchdog Timer Function

The H8/38602R includes a watchdog timer. The watchdog timer is active after reset. The timer counter WD (TCWD) is incremented and if the TCWD overflows, the H8/38602R is internally reset. This sample task does not use the watchdog timer function, and thus stops this timer.

- Timer Control/Status Register WD1 (TCSRWD1)
  TCSRWD1 controls writing to TCSRWD1 and TCWD. TCSRWD1 also controls the watchdog timer operation and indicates the operating status. TCSRWD1 must be rewritten by using the MOV instruction. Bit manipulation instructions cannot be used to change the setting value.

2.1.3 Module Standby Function

The module standby function places the SSU in the module standby mode after the reset is released. The module standby mode can be cancelled by setting the SSUCKSTP bit of the clock halt register 2 (CKSTPR2) to 1.

- Clock Halt Register 2 (CKSTPR2)
  CKSTPR2 allows the on-chip peripheral modules to enter standby mode in module units.

2.1.4 I/O Port Function

The P91/SSCK/SDA pin is pulled up so that the pin normally stays high (slave device only).

- Port Pull-Up Control Register 9 (PUCR9)
  PUCR9 controls the pull-up MOS of the port 9 pins in bit units.

2.2 Assignment of Functions

Functions used for this sample task are listed in tables 1 and 2. Communication by the SSU is performed in clocked synchronous communication mode by assigning the functions as shown in tables 1 and 2.

Table 1 Function Assignment of Master Device

Function	Category	Description
SSCK	Pin	SSU clock output
SSI	Pin	SSU data input
SSO	Pin	SSU data output
SSCRH	SSU	Selects master mode and the SSCK pin function.
SSCRL	SSU	Selects clocked synchronous communication mode.
SSMR	SSU	Selects LSB-first and a transfer clock rate of ϕ/8.
SSER	SSU	Enables transmission/reception and controls RSSTP.
SSSR	SSU	Status flags
SSRDR	SSU	A register that stores received data
SSTDR	SSU	A register that stores transmit data
SSTRSR	SSU	A shift register used to transmit or receive data
CKSTPR2	Low power	Cancels module standby mode of the SSU.
TCSRWD1	WDT	Stops the watchdog timer.

Table 2 Function Assignment of Slave Device

Function	Category	Description
SSCK	Pin	SSU clock output
SSI	Pin	SSU data input
SSO	Pin	SSU data output
SSCRH	SSU	Selects slave mode and the SSCK pin function.
SSCRL	SSU	Selects clocked synchronous communication mode.
SSMR	SSU	Selects LSB-first and a transfer clock rate of ϕ/8.
SSER	SSU	Enables data transmission/reception.
SSSR	SSU	Status flags
SSRDR	SSU	A register that stores receive data
SSTDR	SSU	A register that stores transmit data
SSTRSR	SSU	A shift register used to transmit or receive data
PUCR9	I/O port	Pulls up the SSCK pin.
CKSTPR2	Low power	Cancels module standby mode of the SSU.
TCSRWD1	WDT	Stops the watchdog timer.

3. Description of Operation

3.1 Transmit Mode

Figure 3 illustrates the operation timing in transmit mode for this sample task, with description of the hardware and software processing.

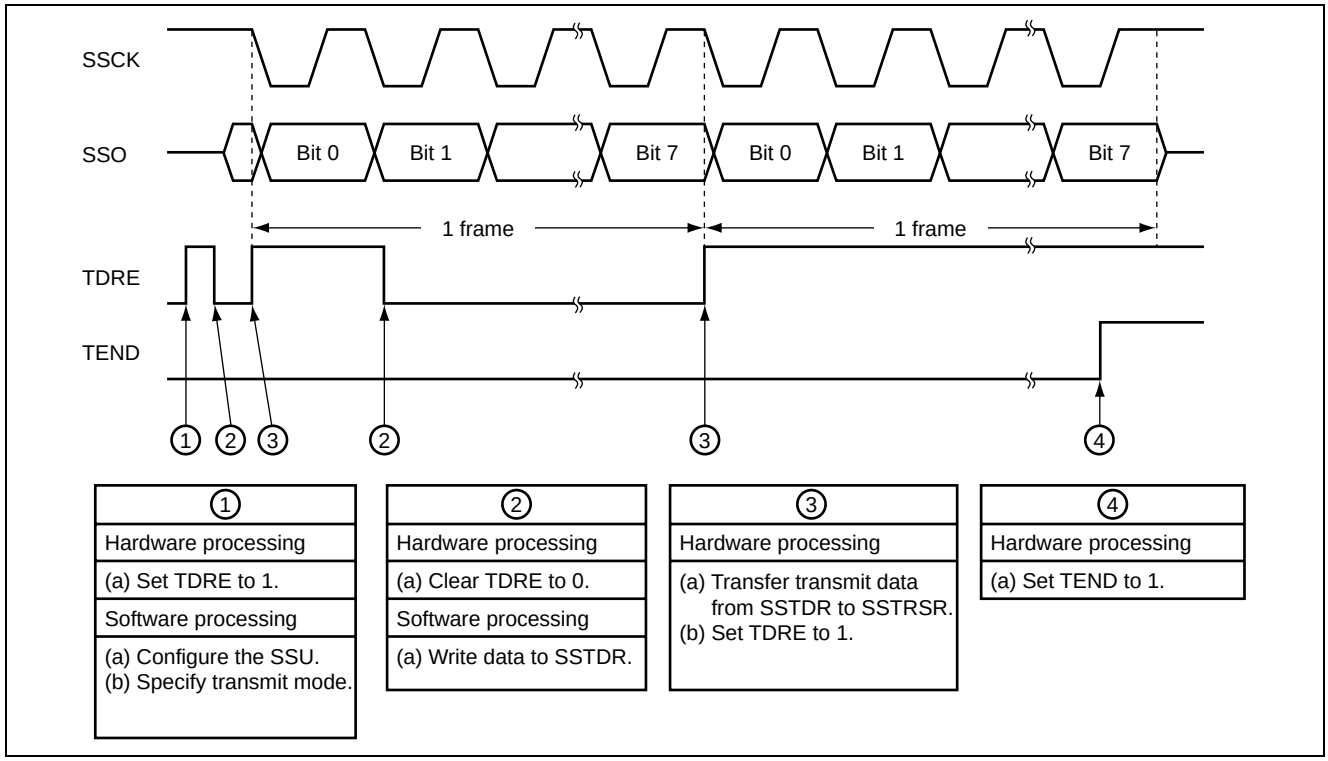
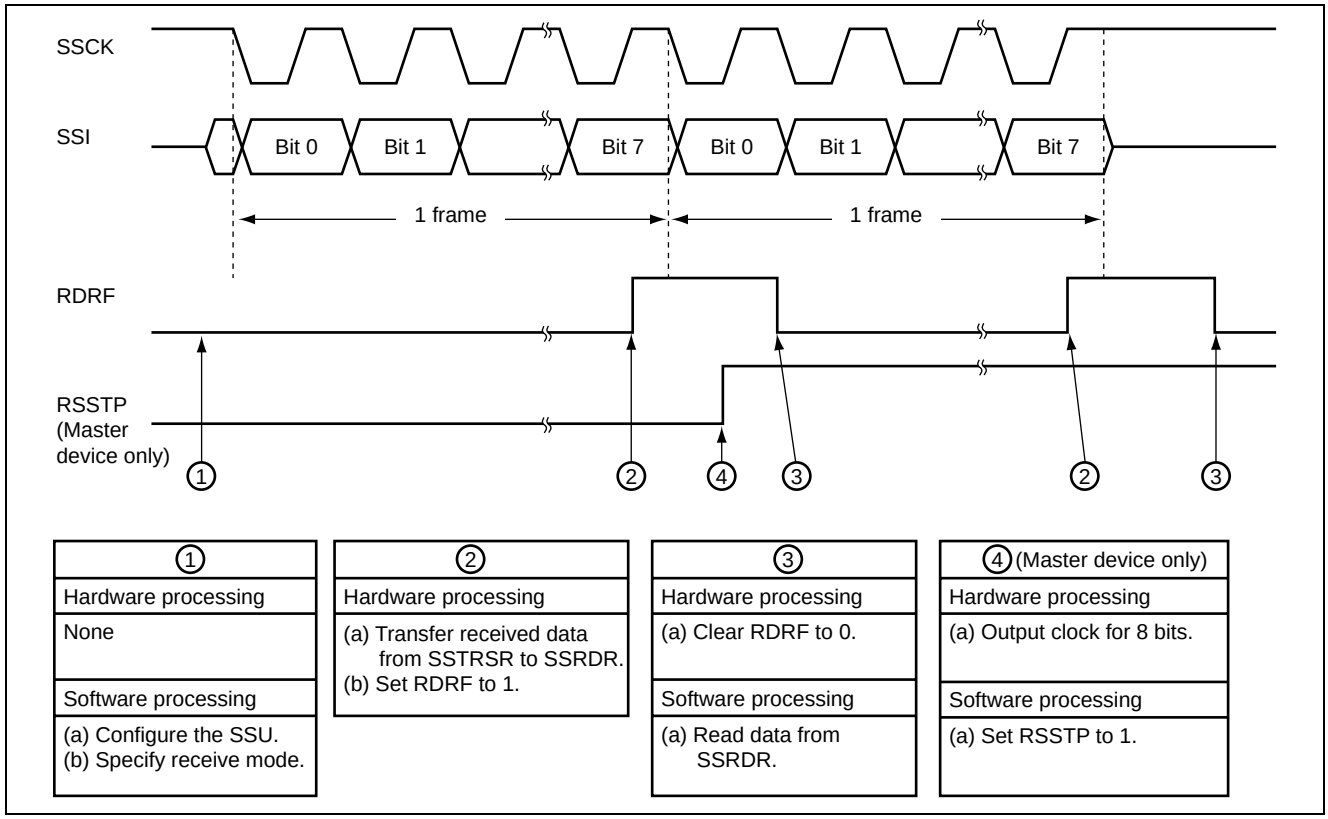


Figure 3 Operation Timing in Transmit Mode

3.2 Receive Mode

Figure 4 illustrates the operation timing in receive mode for this sample task, with description of the hardware and software processing.



①	②	③	④ (Master device only)
Hardware processing	Hardware processing	Hardware processing	Hardware processing
None	(a) Transfer received data from SSTRSR to SSRDR. (b) Set RDRF to 1.	(a) Clear RDRF to 0.	(a) Output clock for 8 bits.
Software processing		Software processing	Software processing
(a) Configure the SSU. (b) Specify receive mode.		(a) Read data from SSRDR.	(a) Set RSSTP to 1.

Figure 4 Operation Timing in Receive Mode

4. Description of Software (Master)

This sample task performs processing for master transmission and master reception using clocked synchronous communication mode of the SSU.

4.1 List of Functions

Table 3 lists the functions used in this sample task.

Table 3 Master Program Functions

Function Name	Description
main	Stops the watchdog timer, controls master transmission/reception, and initializes the RAM area to be used.
SSU_clock_int	Initializes the SSU in clocked synchronous communication mode and cancels module standby state of the SSU.
transmit	Master transmission
receive	Master reception

4.2 Constants

This sample task does not use constants.

4.3 RAM Usage

Table 4 describes the RAM usage in this sample task.

Table 4 Description of RAM

Label Name	Function	Data Length	Used In
m_trs[0] to m_trs[3]	Buffer for storing transmit data	4 bytes	main
m_rcv[0] to m_rcv[3]	Buffer for storing received data	4 bytes	main

4.4 Description of Module

4.4.1 main() Function

(1) Module Specifications

Function: Stops the watchdog timer, controls master transmission and reception, and initializes the RAM area to be used.

Table 5 Module Specifications

Item	Type	Variable Name	Description
Argument	None	None	None

(2) Internal Registers

The internal registers used in this sample task are described below. The setting values in the tables below are used in this task and are different from the initial values.

- SS Enable Register (SSER) Address: H'F0E3

Bit	Bit Name	Setting	R/W	Function
7	TE	0/1	R/W	Transmit enable When this bit is 1, transmit operation is enabled. 0: Disables transmit operation. 1: Enables transmit operation.
6	RE	0/1	R/W	Receive enable When this bit is 1, receive operation is enabled. 0: Disables receive operation. 1: Enables receive operation.
5	RSSTP	1	R/W	Receive single stop When this bit is 1, receive operation ends after receiving one byte.

- SS Status Register (SSSR) Address: H'F0E4

Bit	Bit Name	Setting	R/W	Function
6	ORER	—	R/(W)*	Overrun Error Flag Indicates that reception has ended abnormally because of an overrun error. SSRDR retains the data received before the overrun error occurs, and the data received after the overrun error will be lost. In addition, subsequent serial reception cannot be continued when this bit is 1. If the MSS bit in SSCRH is 1, serial transmission also cannot be continued. [Setting condition] • When the next serial reception is completed while RDRF = 1. [Clearing condition] • When 0 is written to this bit after reading 1.
3	TEND	—	R/(W)*	Transmit end [Setting condition] • When the last bit of data is transmitted with the TDRE bit set to 1. [Clearing conditions] 0 is written to this bit after reading 1. Data is written to SSTDR.
1	RDRF	—	R/(W)*	Receive Data Register Full [Setting condition] • When serial reception ended normally and received data has been transferred from SSTRSR to SSRDR. [Clearing condition] • When 0 is written to this bit after reading 1 • When data is read from SSRDR.

Note: Only 0 can be written to clear the flag.

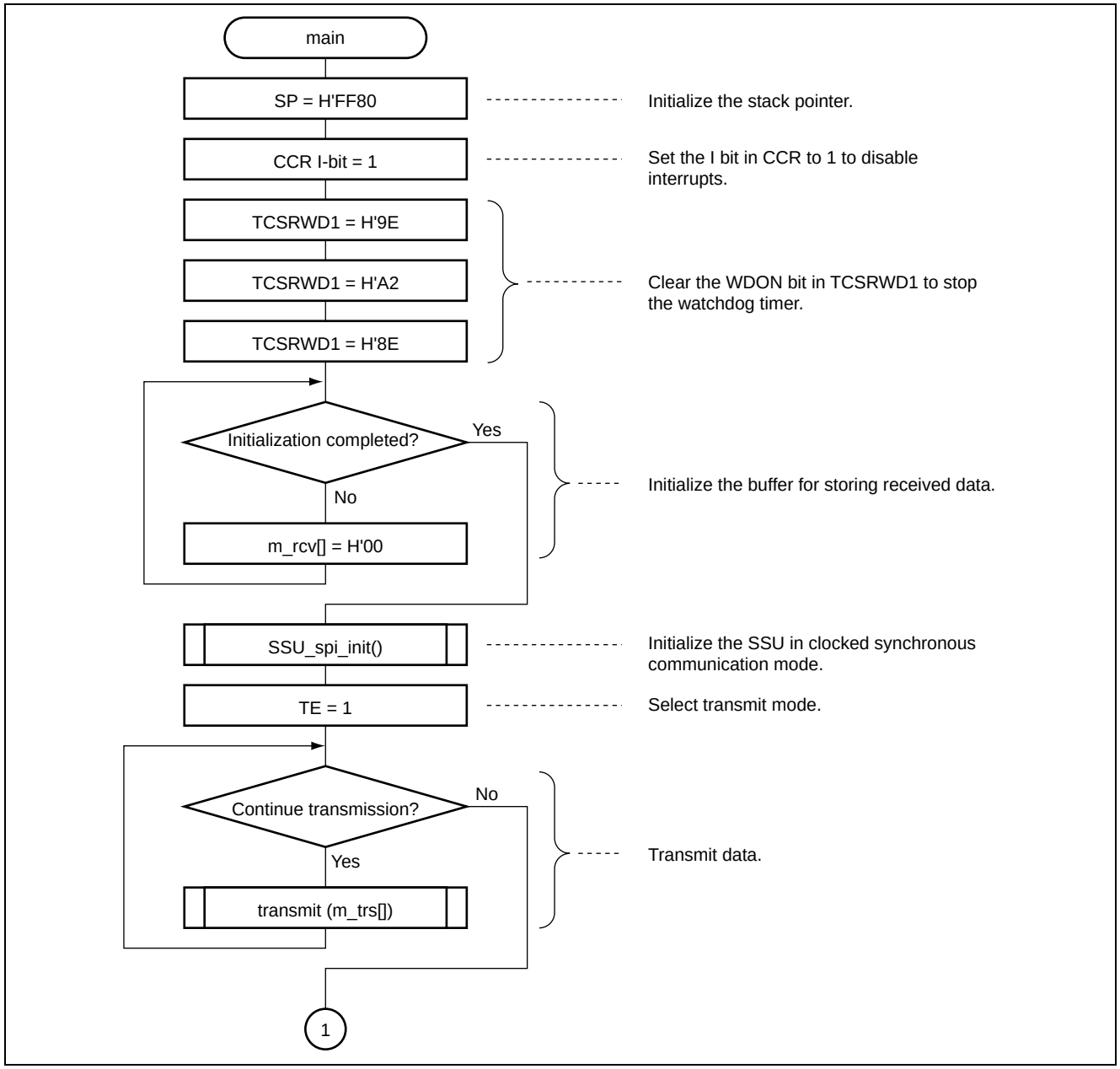
- SS Receive Data Register (SSRDR) Address: H'F0E9

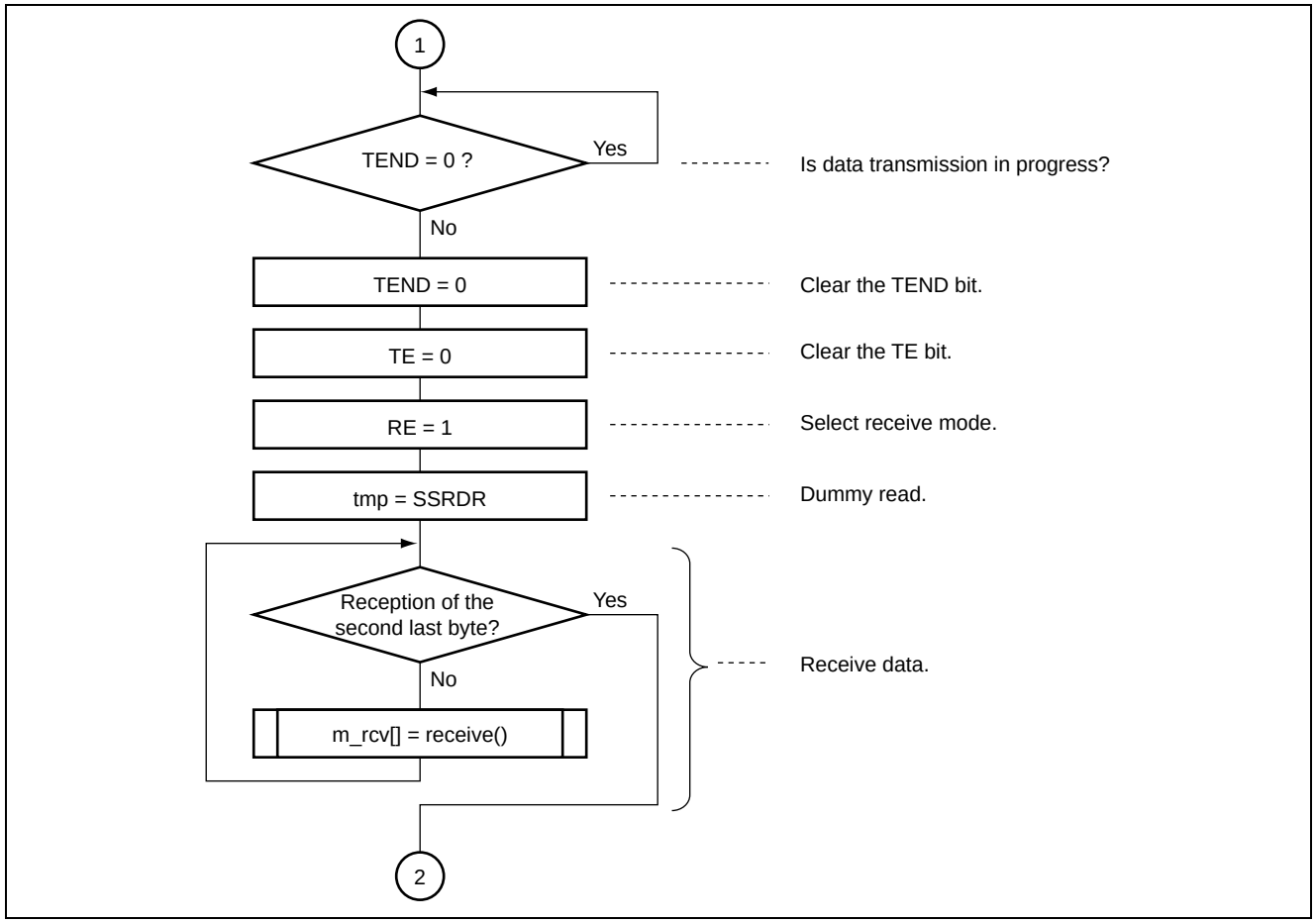
Bit	Bit Name	Setting	R/W	Function
7	bit7	—	R	SSRDR is an 8-bit register that stores received serial data. When the SSU has received one byte of serial data, it transfers the received serial data from SSTRSR to SSRDR. SSTRSR is then ready to receive the next data. This double-buffered configuration of SSTRSR and SSRDR allows continuous receive operation. SSRDR is a read-only register and cannot be written to by the CPU. The initial value of SSRDR is H'00.
6	bit6	—	R	
5	bit5	—	R	
4	bit4	—	R	
3	bit3	—	R	
2	bit2	—	R	
1	bit1	—	R	
0	bit0	—	R	

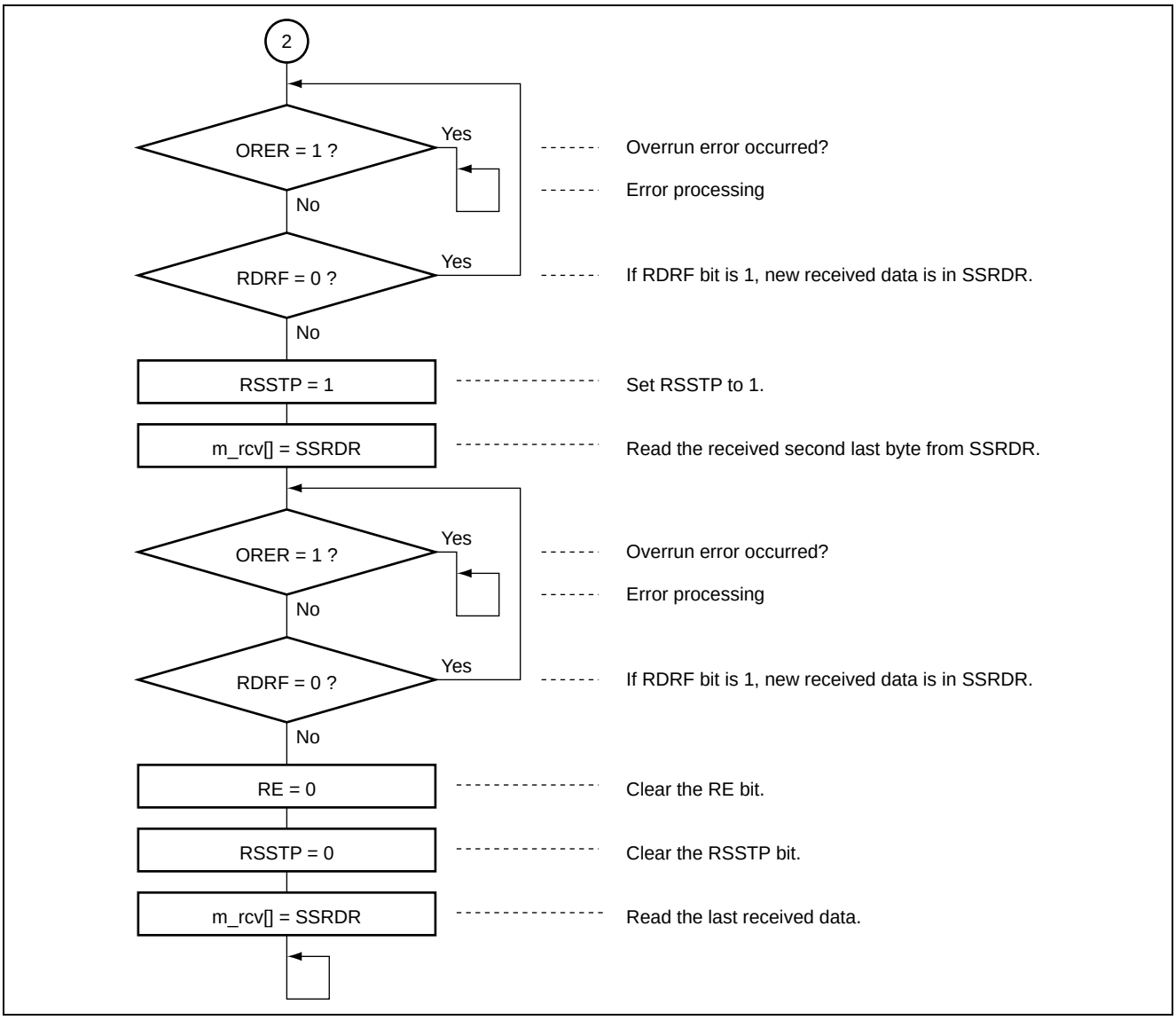
- Timer Control Register/Status Register WD1 (TCSRWD1) Address: H'FFB1

Bit	Bit Name	Setting	R/W	Function
7	B6WI	1	R/W	Bit 6 Write Disable Writing to the TCWE bit is only enabled when 0 is written to the B6WI bit. This bit is always read as 1.
6	TCWE	0	R/W	Timer Counter WD Write Enable Writing to the timer counter WD (TCWD) is enabled when the TCWE bit is set to 1. When writing to this bit, 0 must be written to the B6WI bit.
5	B4WI	1	R/W	Bit 4 Write Disable Writing to the TCSRWE bit is only enabled when 0 is written to the B4MI bit. The B4WI bit is always read as 1.
4	TCSRWE	0	R/W	Timer Control/Status Register WD1 Write Enable Writing to the WDON and WRST bits are enabled when the TCSRWE bit is set to 1. When writing to this bit, 0 must be written to the B4WI bit.
3	B2WI	1	R/W	Bit 2 Write Disable Writing to the WDON is only enabled when 0 is written to the B2WI bit. This bit is always read as 1.
2	WDON	0	R/W	Watchdog Timer On The TDWD starts counting up when the WDON bit is set to 1 and stops counting when the WDON bit is cleared to 0. [Setting condition] • If 0 is written to the B2WI bit and 1 to the WDON bit while the TCSRWE bit is 1. • Reset [Clearing condition] • If 0 is written to the B2WI and WDON bits while the TCSRWE bit is 1.
1	B0WI	1	R/W	Bit 0 Write Disable Writing to the WRST bit is only enabled when 0 is written to the B0WI bit. This bit is always read as 1.
0	WRST	0	R/W	Watchdog Timer Reset [Setting condition] • When the TCWD overflows and an internal reset signal is generated. [Clearing condition] • Reset by the $\overline{\text{RES}}$ pin • If 0 is written to both the BOWI and WRST bits while the TCSRWE bit is 1.

(3) Flowchart


main
SP = H'FF80
Initialize the stack pointer.
CCR I-bit = 1
Set the I bit in CCR to 1 to disable interrupts.
TCSRWD1 = H'9E
TCSRWD1 = H'A2
TCSRWD1 = H'8E
Clear the WDON bit in TCSRWD1 to stop the watchdog timer.
Initialization completed?
Yes
No
m_rcv[] = H'00
Initialize the buffer for storing received data.
SSU_spi_init()
Initialize the SSU in clocked synchronous communication mode.
TE = 1
Select transmit mode.
Continue transmission?
No
Yes
transmit (m_trs[])
Transmit data.
1


1
TEND = 0 ?
Yes
No
Is data transmission in progress?
TEND = 0
Clear the TEND bit.
TE = 0
Clear the TE bit.
RE = 1
Select receive mode.
tmp = SSRDR
Dummy read.
Reception of the second last byte?
Yes
No
m_rcv[] = receive()
Receive data.
2


2
ORER = 1 ?
Yes
No
Overrun error occurred?
Error processing
RDRF = 0 ?
Yes
No
If RDRF bit is 1, new received data is in SSRDR.
RSSTP = 1
Set RSSTP to 1.
m_rcv[] = SSRDR
Read the received second last byte from SSRDR.
ORER = 1 ?
Yes
No
Overrun error occurred?
Error processing
RDRF = 0 ?
Yes
No
If RDRF bit is 1, new received data is in SSRDR.
RE = 0
Clear the RE bit.
RSSTP = 0
Clear the RSSTP bit.
m_rcv[] = SSRDR
Read the last received data.

4.4.2 SSU_clock_init() Function

(1) Module Specifications

Function: Initializes the SSU in clocked synchronous communication mode, and cancels SSU module standby mode.

Table 6 Module Specifications

Item	Type	Variable Name	Description
Argument	None	None	None

(2) Internal Registers

The internal registers used in this sample task are described below. The setting values in the tables below are used in this task and are different from the initial values.

- SS Control Register H (SSCRH) Address: H'F0E0

Bit	Bit Name	Setting	R/W	Function
7	MSS	1	R/W	Master/Slave Device Select Selects whether this module is used as a master device or a slave device. When this module is used as a master device, transfer clock is output from the SSCK pin. When the CE bit in SSSR is set, the MSS bit is automatically cleared. 1: Operates as a master device
2	SCKS	1	R/W	SSCK Pin Select Selects whether the SSCK pin functions as a port or a serial clock pin. 1: Functions as a serial clock pin

- SS Control Register L (SSCRL) Address: H'F0E1

Bit	Bit Name	Setting	R/W	Function
6	SSUMS	0	R/W	SSU Mode Select Selects which combination of the serial data input pin and serial data output pin is used. 0: Clocked synchronous communication mode • Data input: SSI pin, Data output: SSO pin

- SS Mode Register (SSMR) Address: H'F0E2

Bit	Bit Name	Setting	R/W	Function
7	MLS	0	R/W	MSB-First/LSB-First Select Selects whether data transfer is performed in MSB-first or LSB-first. 0: LSB-first
2	CKS2	1	R/W	Transfer Clock Rate Select
1	CKS1	0	R/W	Sets transfer clock rate (prescaler division ratio) when the internal clock is selected. Table 7 shows the transfer rate.
0	CKS0	1	R/W	CKS2 = 1, CKS1 = 0, CKS0 = 1: ϕ/8

Table 7 Transfer Rate

Bit 2	Bit 1	Bit 0		Transfer Rate
CKS2	CKS1	CKS0	Clock	ϕ = 10 MHz
1	0	1	ϕ/8	1.25 MHz

- SS Enable Register (SSER) Address: H'F0E3

Bit	Bit Name	Setting	R/W	Function
7	TE	0	R/W	Transmit Enable When this bit is 1, transmit operation is enabled. 0: Disables transmit operation
6	RE	0	R/W	Receive Enable When this bit is 1, receive operation is enabled. 0: Disables receive operation

- SS Status Register (SSSR) Address: H'F0E4

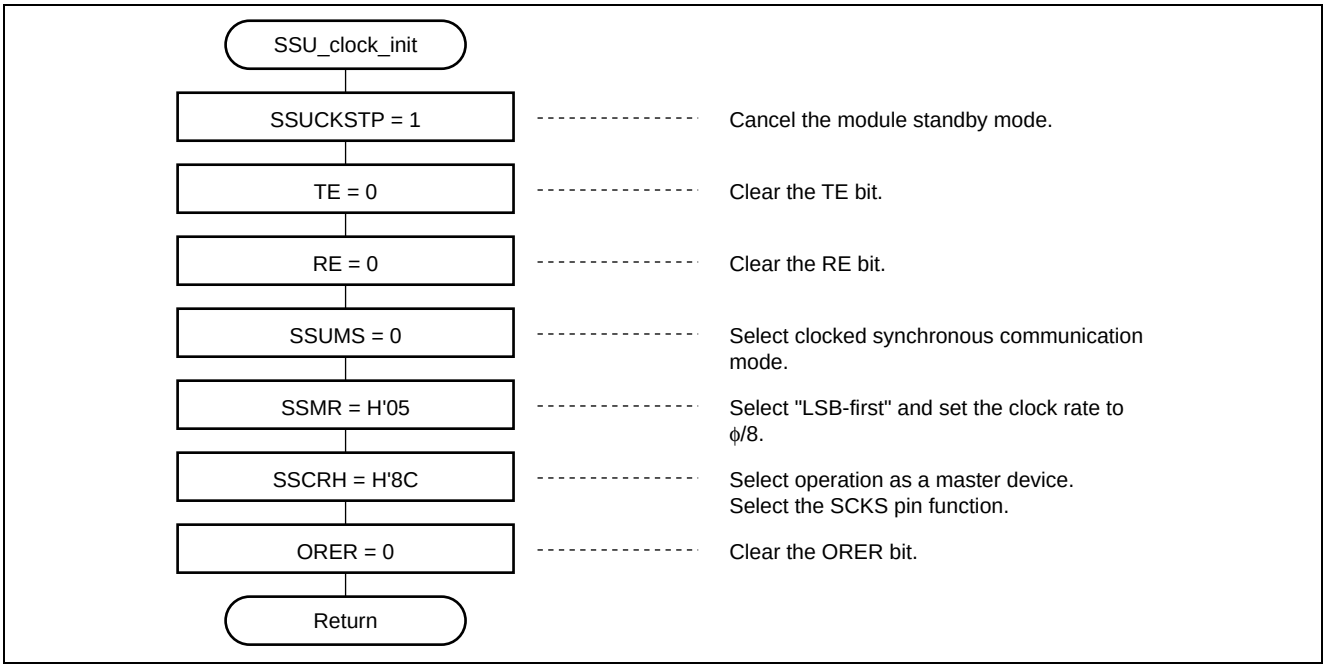
Bit	Bit Name	Setting	R/W	Function
6	ORER	0	R/(W)*	Overrun Error Flag Indicates that reception has ended abnormally because of an overrun error. SSRDR retains the data received before the overrun error occurs, and the data received after the overrun error will be lost. In addition, subsequent serial reception cannot be continued when this bit is 1. If the MSS bit in SSCRH is 1, serial transmission also cannot be continued. [Setting condition] • When the next serial reception is completed while RDRF = 1. [Clearing condition] • When 0 is written to this bit after reading 1.

Note: Only 0 can be written to clear the flag.

- Clock Halt Register (CKSTPR2) Address: H'FFFB

Bit	Bit Name	Setting	R/W	Function
4	SSUCKSTP	1	R/W	SSU Module Standby SSU enters module standby mode when this bit is cleared to 0. 1: Cancels SSU module standby mode.

(3) Flowchart


SSU_clock_init
SSUCKSTP = 1
Cancel the module standby mode.
TE = 0
Clear the TE bit.
RE = 0
Clear the RE bit.
SSUMS = 0
Select clocked synchronous communication mode.
SSMR = H'05
Select "LSB-first" and set the clock rate to ϕ/8.
SSCRH = H'8C
Select operation as a master device.
Select the SCKS pin function.
ORER = 0
Clear the ORER bit.
Return

4.4.3 transmit() Function

(1) Module Specifications

Function: Master transmission

Table 8 Module Specifications

Item	Type	Variable Name	Description
Argument	unsigned char	trs_data	Transmit data

(2) Internal Registers

The internal registers used in this sample task are described below. The setting values in the tables below are used for this task and are different from the initial values.

- SS Status Register (SSSR) Address: H'F0E4

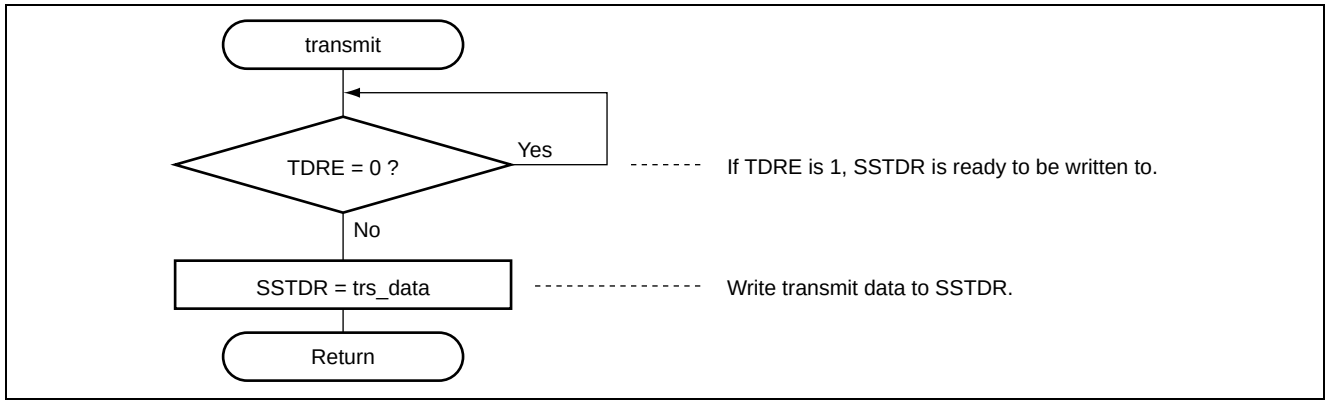
Bit	Bit Name	Setting	R/W	Function
2	TDRE	—	R/(W)*	Transmit Data Empty [Setting condition] • When the TE bit of SSER is 0. • When data is transferred from SSTDR to SSTRSR and SSTDR has become ready to be written to. [Clearing condition] • When 0 is written to this bit after reading 1 • When data is written to SSTDR

Note: Only 0 can be written to clear the flag.

- SS Transmit Data Register (SSTDR) Address: H'F0EB

Bit	Bit Name	Setting	R/W	Function
7	bit7	—	R/W	SSTDR is an 8-bit register that stores serial data to be transmitted. SSTDR can be read from or written to by the CPU at any time. When the SSU detects that SSTRSR is empty, it transfers the transmit data stored in SSTDR to SSTRSR to start serial transmission. If the next transmit data has already been written to SSTDR during serial transmission, continuous serial transmission is possible. The initial value of SSTDR is H'00.
6	bit6	—	R/W	
5	bit5	—	R/W	
4	bit4	—	R/W	
3	bit3	—	R/W	
2	bit2	—	R/W	
1	bit1	—	R/W	
0	bit0	—	R/W	

(3) Flowchart


transmit
TDRE = 0 ?
Yes
If TDRE is 1, SSTDR is ready to be written to.
No
SSTDR = trs_data
Write transmit data to SSTDR.
Return

4.4.4 receive() Function

(1) Module Specifications

Function: Master reception

Table 9 Module Specifications

Item	Type	Variable Name	Description
Argument	None	None	None
Return value	unsigned char	—	Receive data

(2) Internal Registers

The internal registers used in this sample task are described below. The setting values in the tables below are used in this task and are different from the initial values.

- SS Status Register (SSSR) Address: H'F0E4

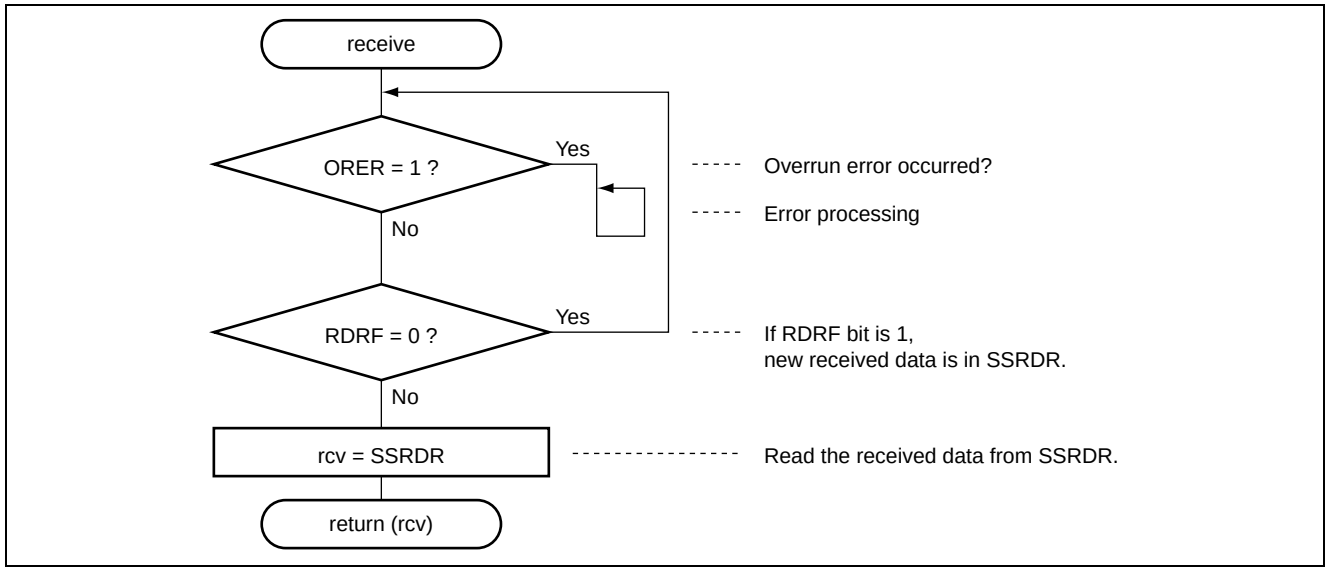
Bit	Bit Name	Setting	R/W	Function
6	ORER	0	R/(W)*	Overrun Error Flag Indicates that reception has ended abnormally because of an overrun error. SSRDR retains the data received before the overrun error occurs, and the data received after the overrun error will be lost. In addition, subsequent serial reception cannot be continued when this bit is 1. If the MSS bit in SSCRH is 1, serial transmission also cannot be continued. [Setting condition] • When the next serial reception is completed while RDRF = 1. [Clearing condition] • When 0 is written to this bit after reading 1.
1	RDRF	0	R/(W)*	Receive Data Register Full [Setting condition] • When serial reception ended normally and received data has been transferred from SSTRSR to SSRDR. [Clearing condition] • When 0 is written to this bit after reading 1 • When data is read from SSRDR.

Note: Only 0 can be written to clear the flag.

- SS Receive Data Register (SSRDR) Address: H'F0E9

Bit	Bit Name	Setting	R/W	Function
7	bit7	—	R	SSRDR is an 8-bit register that stores received serial data. When the SSU has received one byte of serial data, it transfers the received serial data from SSTRSR to SSRDR. SSTRSR is then ready to receive the next data. This double-buffered configuration of SSTRSR and SSRDR allows continuous receive operation. SSRDR is a read-only register and cannot be written to by the CPU. The initial value of SSRDR is H'00.
6	bit6	—	R	
5	bit5	—	R	
4	bit4	—	R	
3	bit3	—	R	
2	bit2	—	R	
1	bit1	—	R	
0	bit0	—	R	

(3) Flowchart



4.5 Link Address Specification

Section Name	Address
CVECT	H'0000
P	H'0100
D,B	H'FB80

5. Description of Software (Slave)

This sample task performs processing for slave transmission and slave reception using clocked synchronous communication mode of the SSU.

5.1 List of Functions

Table 10 lists the functions used in this sample task.

Table 10 Slave Program Functions

Function Name	Description
main	Stops the watchdog timer, controls slave transmission/reception, pulls up the SSCK pin, and initializes the RAM area to be used.
SSU_clock_int	Initializes the SSU in clocked synchronous communication mode and cancels module standby mode of the SSU.
transmit	Slave transmission
receive	Slave reception

5.2 Constants

This sample task does not use constants.

5.3 RAM Usage

Table 11 describes the RAM usage in this sample task.

Table 11 Description of RAM

Label Name	Function	Data Length	Used In
s_rcv[0] to s_rcv[3]	Buffer for storing received data and transmit data	4 bytes	main

5.4 Description of Modules

5.4.1 main() Function

(1) Module Specification

Function: Stops the watchdog timer, controls the slave transmission and reception, and initializes the RAM area to be used.

Table 12 Module Specifications

Item	Type	Variable Name	Description
Argument	None	None	None

(2) Internal Registers

The internal registers used in this sample task are described below. The setting values in the tables below are used in this task and are different from the initial values.

- Port Pull-up Control Register 9 (PUCR9) Address: H'F087

Bit	Bit Name	Setting	R/W	Function
1	PUCR91	1	R/W	With a PCR9 bit cleared to 0, setting the corresponding PUCR9 bit to 1 turns on the pull-up MOS for the corresponding pin, while clearing the bit to 0 turns off the pull-up MOS.

- SS Enable Register (SSER) Address: H'F0E3

Bit	Bit Name	Setting	R/W	Function
7	TE	0/1	R/W	Transmit enable When this bit is 1, transmit operation is enabled. 0: Disables transmit operation. 1: Enables transmit operation.
6	RE	0/1	R/W	Receive enable When this bit is 1, receive operation is enabled. 0: Disables receive operation. 1: Enables receive operation.

- SS Status Register (SSSR) Address: H'F0E4

Bit	Bit Name	Setting	R/W	Function
3	TEND	—	R/(W)*	Transmit end [Setting condition] • When the last bit of data is transmitted with the TDRE bit set to 1. [Clearing conditions] • 0 is written to this bit after reading 1. • Data is written to SSTDR.

Note: Only 0 can be written to clear the flag.

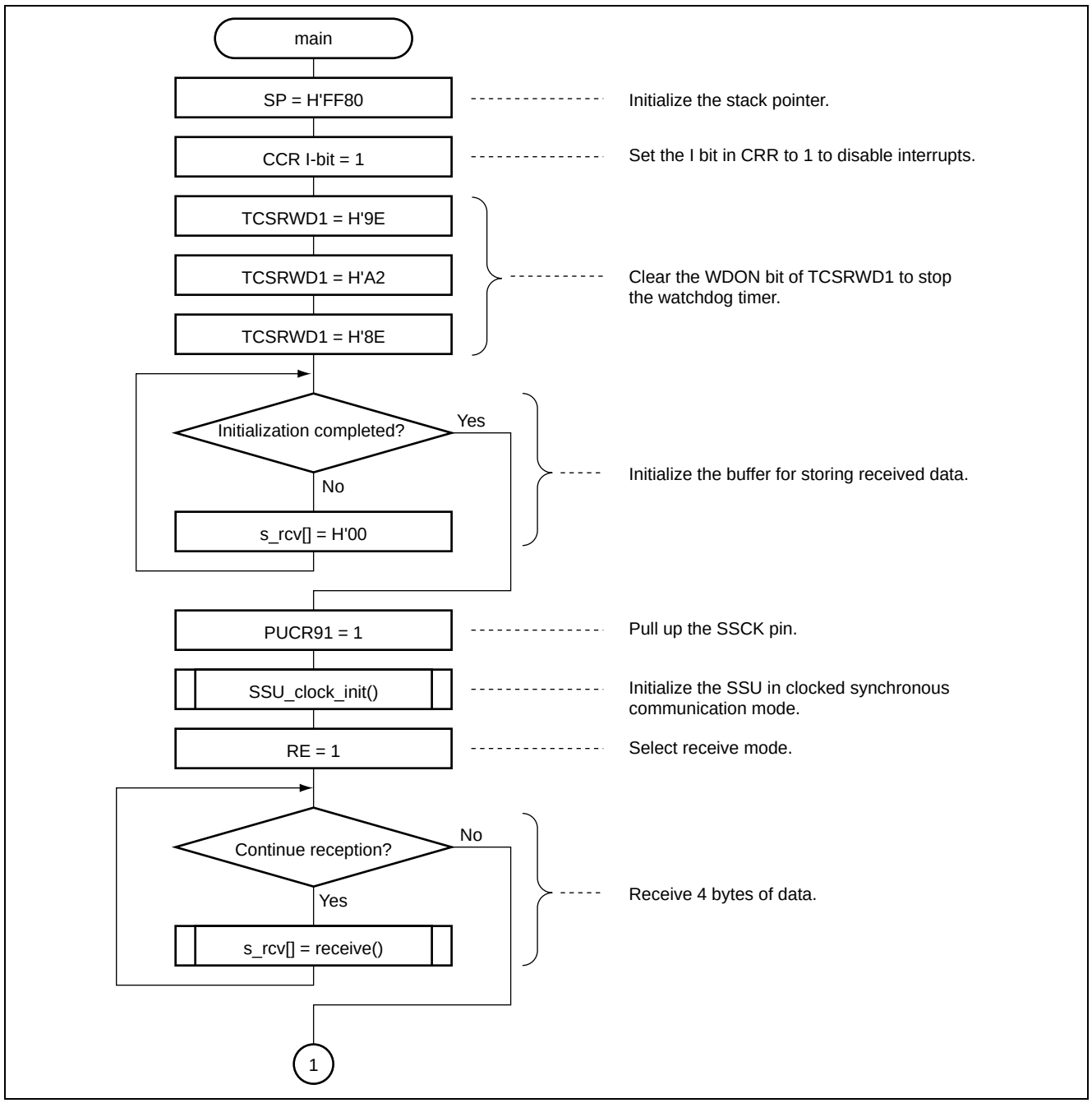
- SS Receive Data Register (SSRDR) Address: H'F0E9

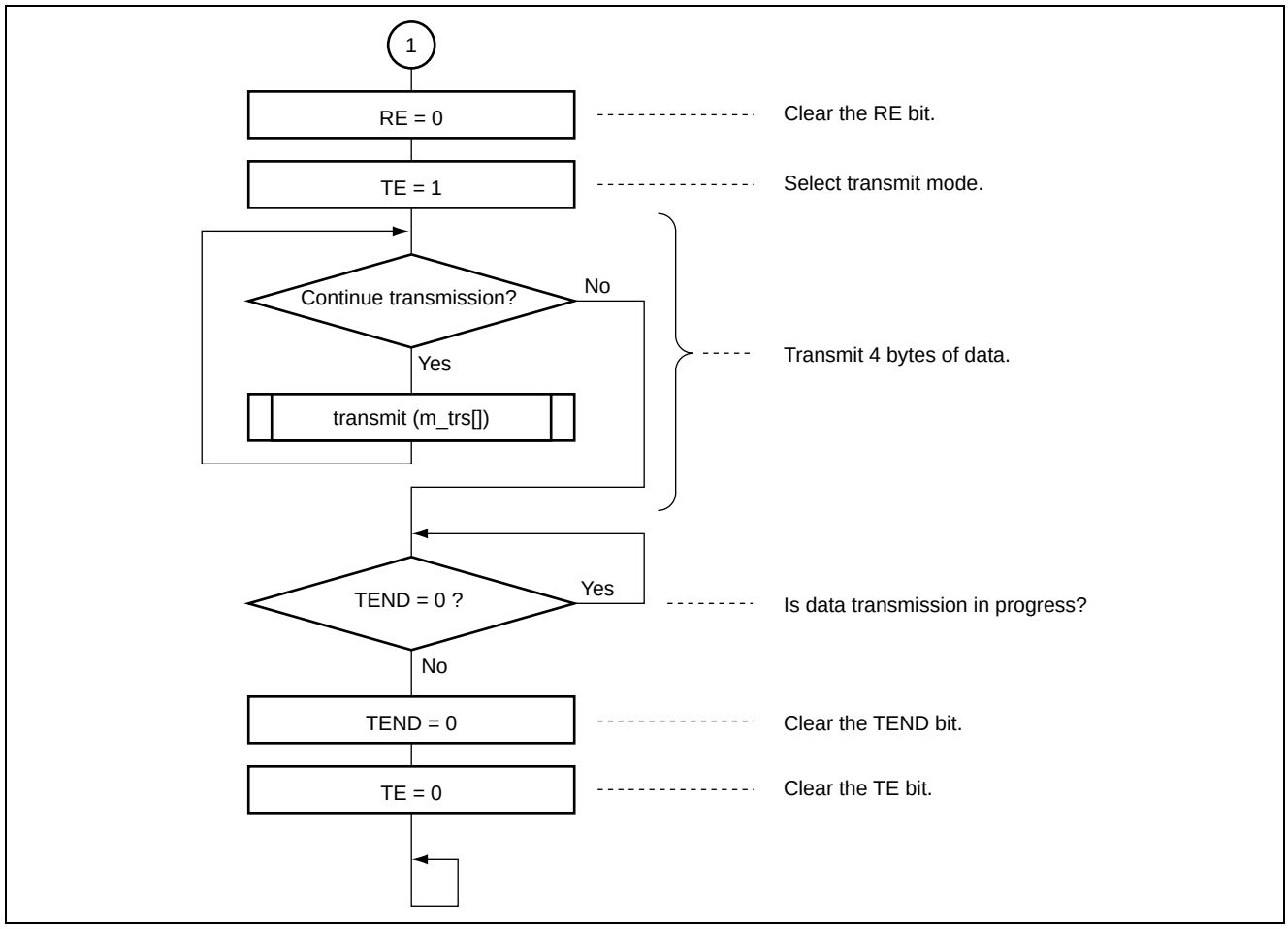
Bit	Bit Name	Setting	R/W	Function
7	bit7	—	R	SSRDR is an 8-bit register that stores received serial data. When the SSU has received one byte of serial data, it transfers the received serial data from SSTRSR to SSRDR. SSTRSR is then ready to receive the next data. This double-buffered configuration of SSTRSR and SSRDR allows continuous receive operation. SSRDR is a read-only register and cannot be written to by the CPU. The initial value of SSRDR is H'00.
6	bit6	—	R	
5	bit5	—	R	
4	bit4	—	R	
3	bit3	—	R	
2	bit2	—	R	
1	bit1	—	R	
0	bit0	—	R	

- Timer Control Register/Status Register WD1 (TCSRWD1) Address: H'FFB1

Bit	Bit Name	Setting	R/W	Function
7	B6WI	1	R/W	Bit 6 Write Disable Writing to the TCWE bit is only enabled when 0 is written to the B6WI bit. This bit is always read as 1.
6	TCWE	0	R/W	Timer Counter WD Write Enable Writing to the timer counter WD (TCWD) is enabled when the TCWE bit is set to 1. When writing to this bit, 0 must be written to the B6WI bit.
5	B4WI	1	R/W	Bit 4 Write Disable Writing to the TCSRWE bit is only enabled when 0 is written to the B4MI bit. The B4WI bit is always read as 1.
4	TCSRWE	0	R/W	Timer Control/Status Register WD1 Write Enable Writing to the WDON and WRST bits are enabled when the TCSRWE bit is set to 1. When writing to this bit, 0 must be written to the B4WI bit.
3	B2WI	1	R/W	Bit 2 Write Disable Writing to the WDON is only enabled when 0 is written to the B2WI bit. This bit is always read as 1.
2	WDON	0	R/W	Watchdog Timer On The TDWD starts counting up when the WDON bit is set to 1 and stops counting when the WDON bit is cleared to 0. [Setting condition] • If 0 is written to the B2WI bit and 1 to the WDON bit while the TCSRWE bit is 1. • Reset [Clearing condition] • If 0 is written to the B2WI and WDON bits while the TCSRWE bit is 1.
1	B0WI	1	R/W	Bit 0 Write Disable Writing to the WRST bit is only enabled when 0 is written to the B0WI bit. This bit is always read as 1.
0	WRST	0	R/W	Watchdog Timer Reset [Setting condition] • When the TCWD overflows and an internal reset signal is generated. [Clearing condition] • Reset by the $\overline{\text{RES}}$ pin • If 0 is written to both the BOWI and WRST bits while the TCSRWE bit is 1.

(3) Flowchart


main
SP = H'FF80
Initialize the stack pointer.
CCR I-bit = 1
Set the I bit in CRR to 1 to disable interrupts.
TCSRWD1 = H'9E
TCSRWD1 = H'A2
TCSRWD1 = H'8E
Clear the WDON bit of TCSRWD1 to stop the watchdog timer.
Initialization completed?
Yes
No
s_rcv[] = H'00
Initialize the buffer for storing received data.
PUCR91 = 1
Pull up the SSCK pin.
SSU_clock_init()
Initialize the SSU in clocked synchronous communication mode.
RE = 1
Select receive mode.
Continue reception?
No
Yes
s_rcv[] = receive()
Receive 4 bytes of data.
1


1
RE = 0
Clear the RE bit.
TE = 1
Select transmit mode.
Continue transmission?
No
Yes
transmit (m_trs[])
Transmit 4 bytes of data.
TEND = 0 ?
Yes
Is data transmission in progress?
No
TEND = 0
Clear the TEND bit.
TE = 0
Clear the TE bit.

5.4.2 SSU_clock_init() Function

(1) Module Specifications

Function: Initializes the SSU in clocked synchronous communication mode, and cancels module standby mode of the SSU.

Table 13 Module Specifications

Item	Type	Variable Name	Description
Argument	None	None	None

(2) Internal Registers

The internal registers used in this sample task are described below. The setting values in the tables below are used in this task and are different from the initial values.

- SS Control Register H (SSCRH) Address: H'F0E0

Bit	Bit Name	Setting	R/W	Function
7	MSS	0	R/W	Master/Slave Device Select Selects whether this module is used as a master device or a slave device. When this module is used as a master device, transfer clock is output from the SSCK pin. When the CE bit in SSSR is set, the MSS bit is automatically cleared. 0: Operates as a slave device
2	SCKS	1	R/W	SSCK Pin Select Selects whether the SSCK pin functions as a port or a serial clock pin. 1: Functions as a serial clock pin

- SS Control Register L (SSCRL) Address: H'F0E1

Bit	Bit Name	Setting	R/W	Function
6	SSUMS	0	R/W	SSU Mode Select Selects which combination of the serial data input pin and serial data output pin is used. 0: Clocked synchronous communication mode • Data input: SSI pin, Data output: SSO pin

- SS Mode Register (SSMR) Address: H'F0E2

Bit	Bit Name	Setting	R/W	Function
7	MLS	0	R/W	MSB-First/LSB-First Select Selects whether data transfer is performed in MSB-first or LSB-first. 0: LSB-first
2	CKS2	1	R/W	Transfer Clock Rate Select
1	CKS1	0	R/W	Sets transfer clock rate (prescaler division ratio) when the internal clock is selected. Table 14 shows the transfer rate.
0	CKS0	1	R/W	CKS2 = 1, CKS1 = 0, CKS0 = 1: ϕ/8

Table 14 Transfer Rates

Bit 2	Bit 1	Bit 0		Transfer Rate
CKS2	CKS1	CKS0	Clock	φ = 10 MHz
1	0	1	φ/8	1.25 MHz

- SS Enable Register (SSER) Address: H'F0E3

Bit	Bit Name	Setting	R/W	Function
7	TE	0	R/W	Transmit Enable When this bit is 1, transmit operation is enabled. 0: Disables transmit operation
6	RE	0	R/W	Receive Enable When this bit is 1, receive operation is enabled. 0: Disables receive operation

- SS Status Register (SSSR) Address: H'F0E4

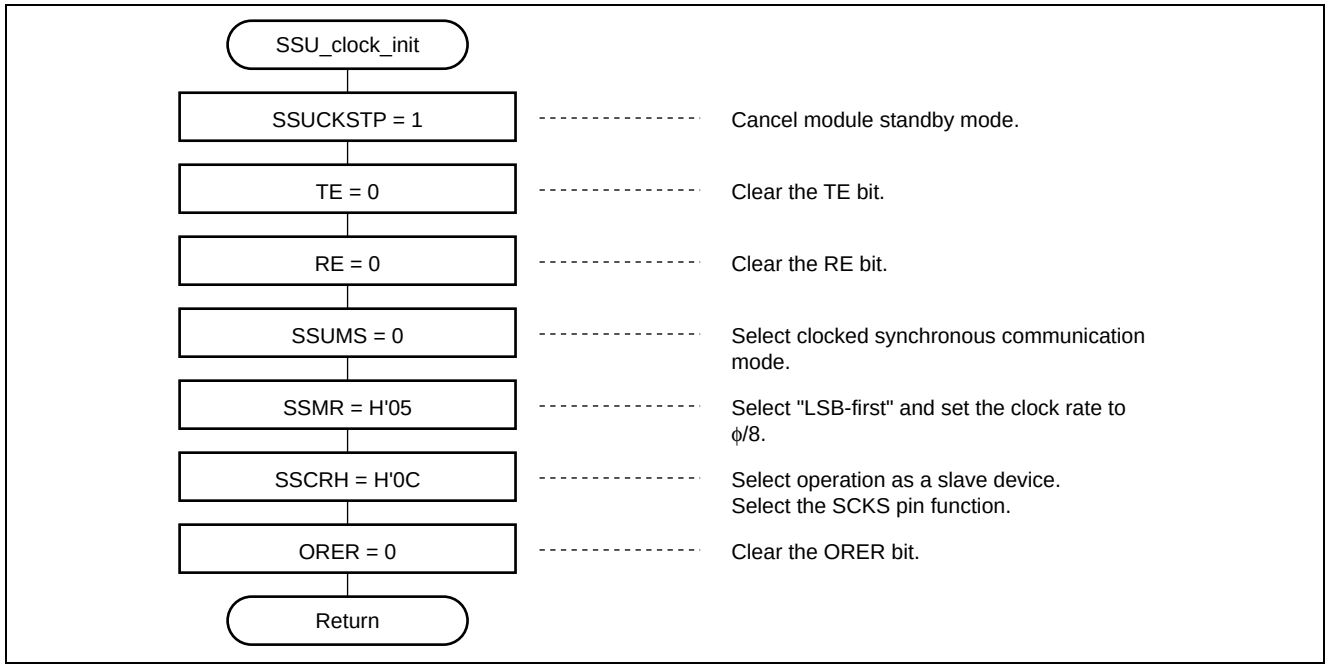
Bit	Bit Name	Setting	R/W	Function
6	ORER	0	R/(W)*	Overrun Error Flag Indicates that reception has ended abnormally because of an overrun error. SSRDR retains the data received before the overrun error occurs, and the data received after the overrun error will be lost. In addition, subsequent serial reception cannot be continued when this bit is 1. If the MSS bit in SSCRH is 1, serial transmission also cannot be continued. [Setting condition] • When the next serial reception is completed while RDRF = 1. [Clearing condition] • When 0 is written to this bit after reading 1.

Note: Only 0 can be written to clear the flag.

- Clock Halt Register 2 (CKSTPR2) Address: H'FFFB

Bit	Bit Name	Setting	R/W	Function
4	SSUCKSTP	1	R/W	SSU Module Standby SSU enters the module standby mode when this bit is cleared to 0. 1: Cancels SSU module standby mode

(3) Flowchart



5.4.3 transmit() Function

(1) Module Specifications

Function: Slave transmission (For details, refer to section 4.4.3, transmit() Function.)

5.4.4 receive() Function

(1) Module Specifications

Function: Slave reception (For details, refer to section 4.4.4, receive() Function.)

5.5 Link Address Specification

Section Name	Address
CVECT	H'0000
P	H'0100
B	H'FB80

Revision Record

		Description	
Rev.	Date	Page	Summary
1.00	Mar.18.05	—	First edition issued

Keep safety first in your circuit designs!

1. Renesas Technology Corp. puts the maximum effort into making semiconductor products better and more reliable, but there is always the possibility that trouble may occur with them. Trouble with semiconductors may lead to personal injury, fire or property damage.
   Remember to give due consideration to safety when making your circuit designs, with appropriate measures such as (i) placement of substitutive, auxiliary circuits, (ii) use of nonflammable material or (iii) prevention against any malfunction or mishap.

Notes regarding these materials

1. These materials are intended as a reference to assist our customers in the selection of the Renesas Technology Corp. product best suited to the customer's application; they do not convey any license under any intellectual property rights, or any other rights, belonging to Renesas Technology Corp. or a third party.
2. Renesas Technology Corp. assumes no responsibility for any damage, or infringement of any third-party's rights, originating in the use of any product data, diagrams, charts, programs, algorithms, or circuit application examples contained in these materials.
3. All information contained in these materials, including product data, diagrams, charts, programs and algorithms represents information on products at the time of publication of these materials, and are subject to change by Renesas Technology Corp. without notice due to product improvements or other reasons. It is therefore recommended that customers contact Renesas Technology Corp. or an authorized Renesas Technology Corp. product distributor for the latest product information before purchasing a product listed herein.
   The information described here may contain technical inaccuracies or typographical errors.
   Renesas Technology Corp. assumes no responsibility for any damage, liability, or other loss rising from these inaccuracies or errors.
   Please also pay attention to information published by Renesas Technology Corp. by various means, including the Renesas Technology Corp. Semiconductor home page (http://www.renesas.com).
4. When using any or all of the information contained in these materials, including product data, diagrams, charts, programs, and algorithms, please be sure to evaluate all information as a total system before making a final decision on the applicability of the information and products. Renesas Technology Corp. assumes no responsibility for any damage, liability or other loss resulting from the information contained herein.
5. Renesas Technology Corp. semiconductors are not designed or manufactured for use in a device or system that is used under circumstances in which human life is potentially at stake. Please contact Renesas Technology Corp. or an authorized Renesas Technology Corp. product distributor when considering the use of a product contained herein for any specific purposes, such as apparatus or systems for transportation, vehicular, medical, aerospace, nuclear, or undersea repeater use.
6. The prior written approval of Renesas Technology Corp. is necessary to reprint or reproduce in whole or in part these materials.
7. If these products or technologies are subject to the Japanese export control restrictions, they must be exported under a license from the Japanese government and cannot be imported into a country other than the approved destination.
   Any diversion or reexport contrary to the export control laws and regulations of Japan and/or the country of destination is prohibited.
8. Please contact Renesas Technology Corp. for further details on these materials or the products contained therein.