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H8/38602R Group

Asynchronous Serial Communication (2400-bits/s at 38.4-kHz Operation)

Introduction

The H8/38062R enters subactive mode and performs asynchronous serial communication. Using the subclock frequency of 38.4 kHz, four bytes of data are transmitted and received at a bit rate of 2400 bits/s.

Target Device

H8/38602R

Contents

1. Specifications

- The H8/38062R is made to enter subactive mode, where the subclock (38.4 kHz) is selected as the operating clock.
- Four bytes of data are transmitted and received.
- The communication format of this sample task includes eight data bits and one stop bit.
- The bit rate is 2400 bits/s.

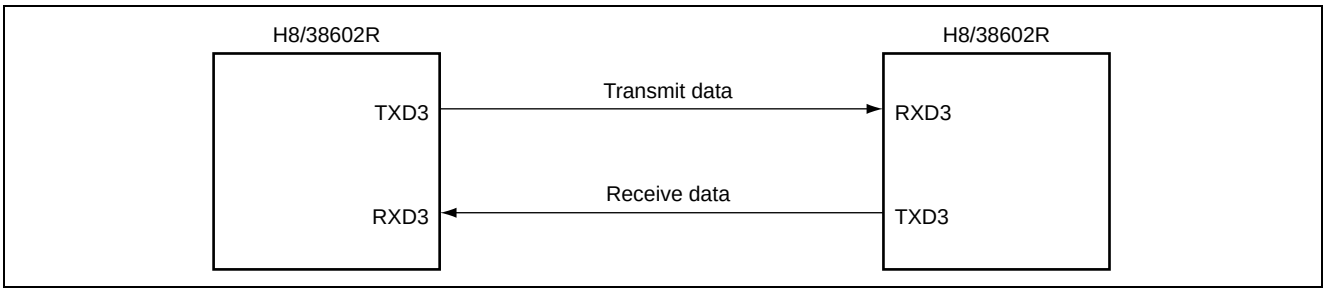


Figure 1 Asynchronous Serial Communication

2. Description of Functions

2.1 Functions

In this sample task, asynchronous serial communication is performed using the SCI3 (Serial Communication Interface 3). Figure 2 shows a block diagram of the SCI3, and below is the functional explanation.

2.1.1 SCI3 Module

The H8/38602R transmits and receives four bytes of data at a bit rate of 2400 bits/s by using the SCI3 module.

- Operating Frequency
  In this sample task, a mode transition is made to subactive mode and the SCI3 operates with a subclock of 38.4 kHz.

- Asynchronous Mode
  In asynchronous mode, serial communication is carried out with synchronization done in character units. This allows serial data communication with LSIs for the standard asynchronous communication, such as the Universal Asynchronous Receiver/Transmitter (UART) and the Asynchronous Communication Interface Adapter (ACIA).

- Internal Clock ϕw
  This is a reference clock that is used to drive on-chip peripheral functions, and is generated by the clock pulse generator.

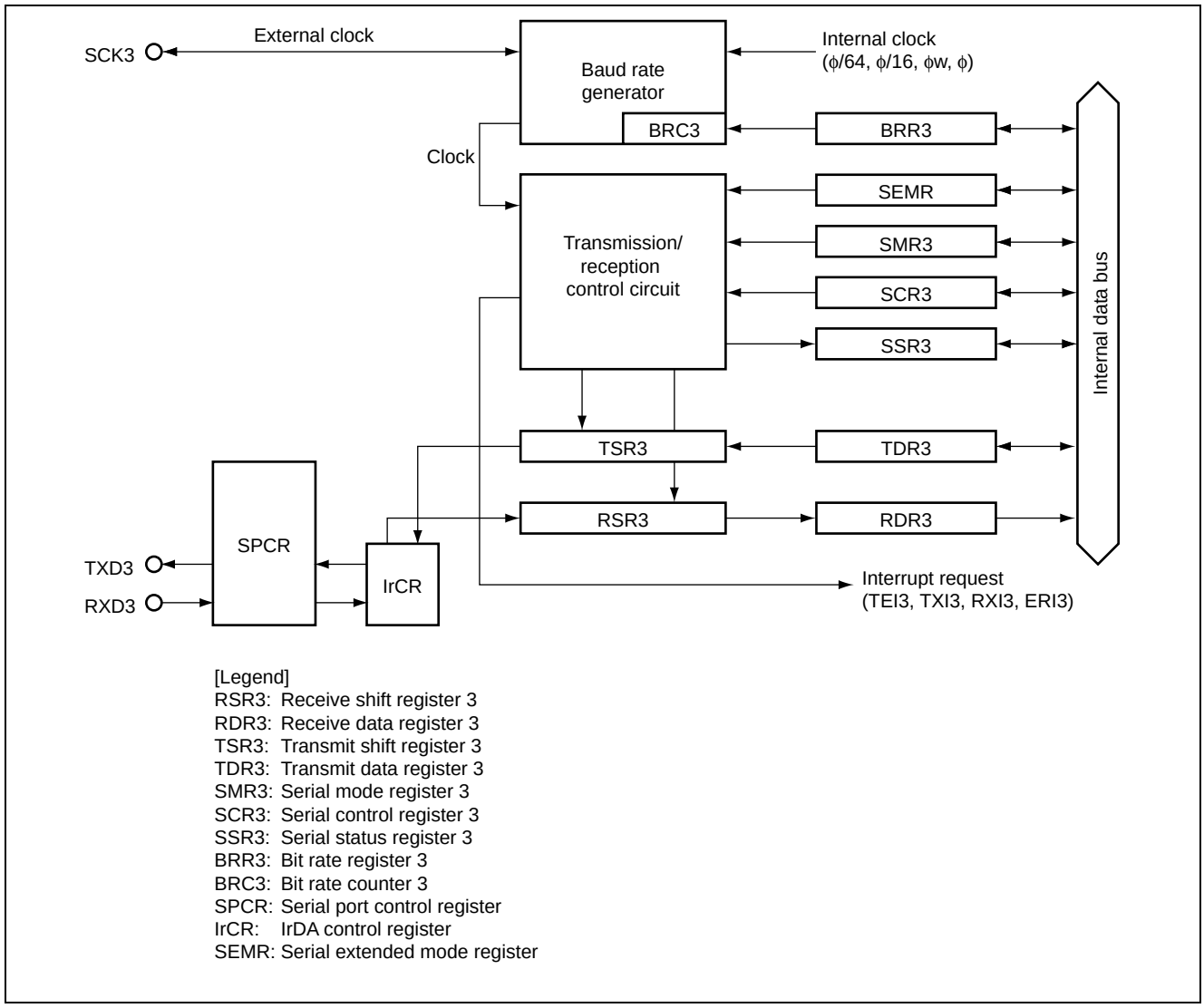


Figure 2 Block Diagram of SCI3

- Serial Port Control Register (SPCR)
  SPCR selects the TXD3 pin function.
- Serial Mode Register 3 (SMR3)
  SMR3 is an 8-bit register that sets the serial data communication format and selects the clock source for the internal baud rate generator.
- Bit Rate Register 3 (BRR3)
  BRR3 is an 8-bit register that controls the bit rate. Because the SC13 has separate baud rate generators for different channels, different baud rates can be set for each channel. For detailed information such as the relationship between the setting values and resulting bit rates, see the hardware manual.
- Serial Control Register 3 (SCR3)
  SCR3 controls transmission/reception operation and interrupt requests, and selects the clock source for transmission/reception.

- Transmit Data Register 3 (TDR3)
  TDR3 is an 8-bit register that stores data for transmission. When the SCI3 detects that TSR3 is empty, it automatically transfers the transmit data written in TDR3 to TSR3 and starts serial data transmission. The double-buffered structure of TDR3 and TSR3 enables continuous serial transmission. If the next transmit data has already been written to TDR3 during transmission of one frame of data, the SCI3 transfers the written data to TSR3 to continue transmission. Although TDR3 can always be read or written by the CPU, transmit data should be written to TDR3 after confirming that the TDRE bit in SSR3 is set to 1.

- Serial Status Register 3 (SSR3)
  SSR3 consists of status flags of the SCI3 and multiprocessor bits for transmission and reception. Flags TDRE, RDRF, OER, PER, and FER can only be cleared.

- Receive Data Register 3 (RDR3)
  RDR3 is an 8-bit register that stores received data. When the SCI3 has received one frame of serial data, it transfers the received data in RSR3 to RDR3. This double-buffered structure of RSR3 and RDR3 permits continuous reception. RDR3 is a receive-only register and can only be read by the CPU.

- Receive Shift Register 3 (RSR3)
  RSR3 is a register that is used to receive serial data. The serial data input from the RXD3 pin is placed in RSR3 from the LSB (bit 0) in the received order, and converted into parallel data. When one frame of data has been received, it is transferred to RDR3 automatically. RSR cannot be directly accessed by the CPU.

- Transmit Shift Register 3 (TSR3)
  TSR3 is a register that is used to transmit serial data. After transmitting one frame of data, the SCI3 transfers the transmit data in TDR3 to TSR3 and outputs the data via the TXD3 pin. TSR3 cannot be directly accessed by the CPU.

- Serial extended mode register (SEMR)
  SEMR sets the basic clock used in asynchronous mode.

2.1.2 Watchdog Timer Function

The H8/38602R includes a watchdog timer. The watchdog timer is active after reset. The timer counter WD (TCWD) is incremented and, if the TCWD overflows, the H8/38602R is internally reset. This sample task does not use the watchdog timer function, and thus stops this timer.

- Timer Control/Status Register WD1 (TCSRWD1)
  TCSRWD1 controls writing to TCSRWD1 and TCWD. TCSRWD1 also controls the watchdog timer operation and indicates the operating status. TCSRWD1 must be rewritten by using the MOV instruction. Bit manipulation instructions cannot be used to change the setting value.

2.1.3 Power-Down Mode Function

In subactive mode, the system clock oscillator stops but on-chip peripheral modules except for the IIC2 operate. As long as a required voltage is applied, the contents of some registers of the on-chip peripheral modules are retained.

Subactive mode is cleared by the SLEEP instruction. When subactive mode is cleared, a transition to subsleep mode, active mode, or watch mode is made, depending on the combination of bits SSBY, LSON, and TMA3 in SYSCR1 and bits MSON and DTON in SYSCR2. Subactive mode will not be cleared if the I bit in CCR is set to 1 or the associated interrupt is disabled by the interrupt enable register.

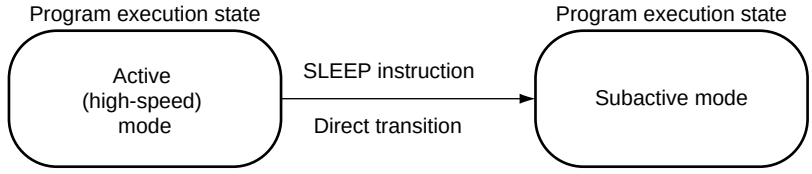
The operating frequency of subactive mode is selected from among ϕw (watch clock), ϕw/2, ϕw/4, and ϕw/8 by the SA1 and SA0 bits in SYSCR2. After the SLEEP instruction is executed, the operating frequency changes to the frequency that is set before the execution.

In this sample task, a direct transition is made from active (high-speed) mode to subactive mode. The CPU can execute programs in two modes: active and subactive mode. A direct transition is a transition between these two modes without stopping program execution. A direct transition is made by executing a SLEEP instruction while the DTON bit in SYSCR2 is set to 1. The direct transition can also be used to change the operating frequency in active or subactive mode. After the mode transition, direct transition interrupt exception handling starts. Note that if a direct transition is attempted while the I bit in CCR is set to 1, sleep or watch mode will be entered, and the resulting mode cannot be cleared by means of an interrupt.

When a SLEEP instruction is executed in active (high-speed) mode while the SSBY, TMA3, and LSON bits in SYSCR1 are set to 1 and the DTON bit in SYSCR2 is set to 1, a transition is made to subactive mode via watch mode.

Figure 3 shows a block diagram of direct transition from active (high-speed) mode to subactive mode.

- System Control Register 1 (SYSCR1)
  SYSCR1 controls the power-down modes, in combination with SYSCR2.
- System Control Register 2 (SYSCR2)
  SYSCR2 controls the power-down modes, in combination with SYSCR1.



Mode transition conditions

LSON	MSON	SSBY	TMA3	DTON
1	X	1	1	1

[Legend] X: Don't care

Figure 3 Direct Transition from Active (High-Speed) Mode to Subactive Mode

2.1.4 Module Standby Function

The module standby function places the SCI3 in the module standby state after the reset is released. The module standby state of the SCI3 can be cleared by setting the S3CKSTP bit in the clock halt register 1 (CKSTPR1) to 1.

- Clock Halt Register 1 (CKSTPR1)
  CKSTPR1 allows the on-chip peripheral modules to enter the standby state in module units.

2.2 Assignment of Functions

Table 1 lists the function assignment for this sample task. By assigning the functions as shown in table 1, transition to subactive mode is made and the subclock of 38.4 kHz is selected as the operating frequency. Four bytes of 8-bit data are transmitted and received at a bit rate of 2400-bits/s.

Table 1 Assignment of Functions

Element	Category	Description
SCK3	Pin	SCI3 clock input/output pin
TXD3	Pin	SCI3 transmit data output pin
RXD3	Pin	SCI3 receive data input pin
SMR3	SCI3	Selects the communication format in asynchronous mode and selects ϕw as the internal baud rate generator clock source.
BRR3	SCI3	Sets the communication bit rate to 2400 bps.
SCR3	SCI3	Enables transmission and reception operations.
TDR3	SCI3	Stores transmit data.
SSR3	SCI3	Includes status flags to indicate SCI3 operation state.
RDR3	SCI3	Stores received data.
RSR3	SCI3	Register used to receive serial data.
TSR3	SCI3	Register used to transmit serial data.
SPCR	SCI3	Selects the TXD3 pin function.
SEMR	SCI3	Sets the basic clock for the bit period in asynchronous mode to a frequency of eight times the transfer rate
SYSCR1	Power-down	Set to make a transition to subactive mode in combination with SYSCR2.
SYSCR2	Power-down	Set to make a transition to subactive mode in combination with SYSCR1.
CKSTPR1	Power-down	Clears the SCI3 module standby state.
TCSRWD1	WDT	Stops the watchdog timer.

3. Principles of Operation

3.1 Asynchronous Serial Data Transmission

Figure 4 illustrates the transmission operation of this sample task. Asynchronous serial transmission is performed through the hardware and software processing shown in the figure. In this sample task, the bit rate is set to 2400 bits/s.

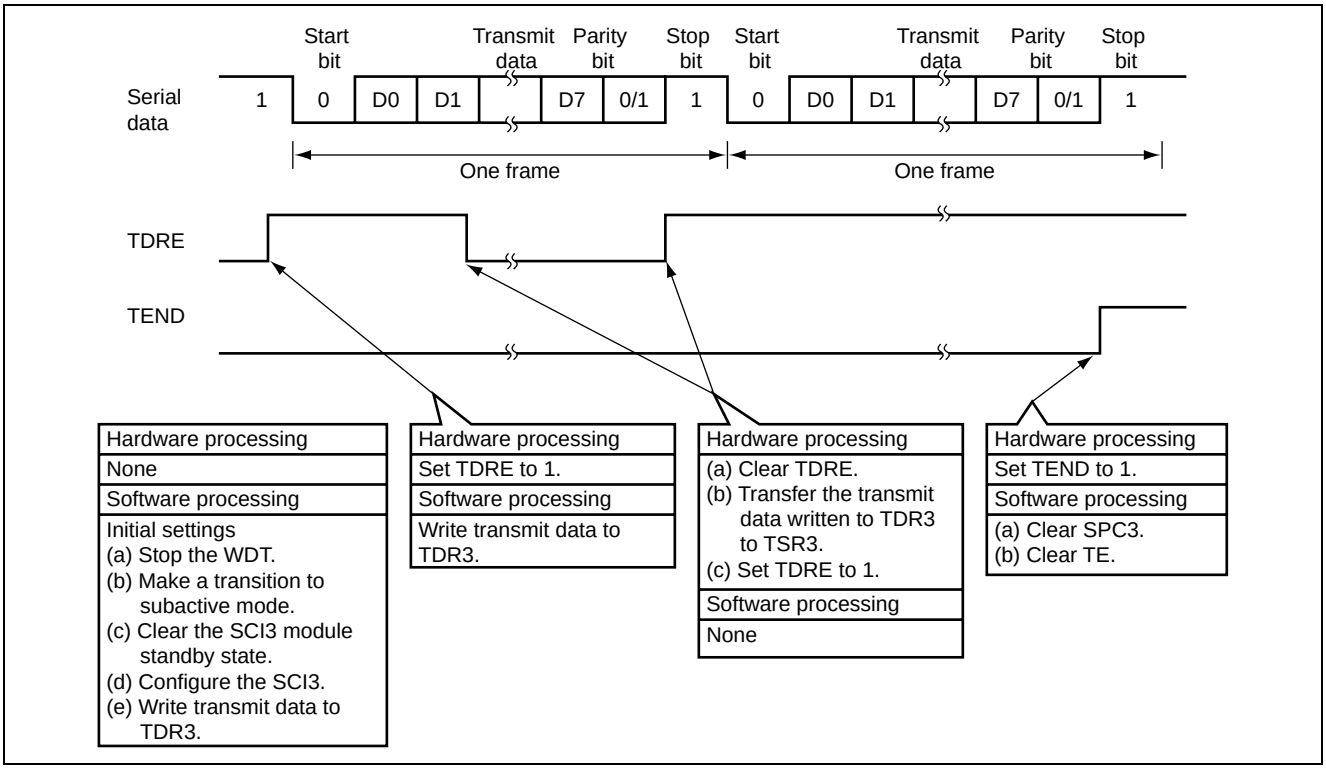


Figure 4 Operation of Asynchronous Serial Data Transmission

3.2 Asynchronous Serial Data Reception

Figure 5 illustrates the reception operation of this sample task. Asynchronous serial reception is performed through the hardware and software processing shown in the figure. In this sample task, the bit rate is set to 2400 bits/s.

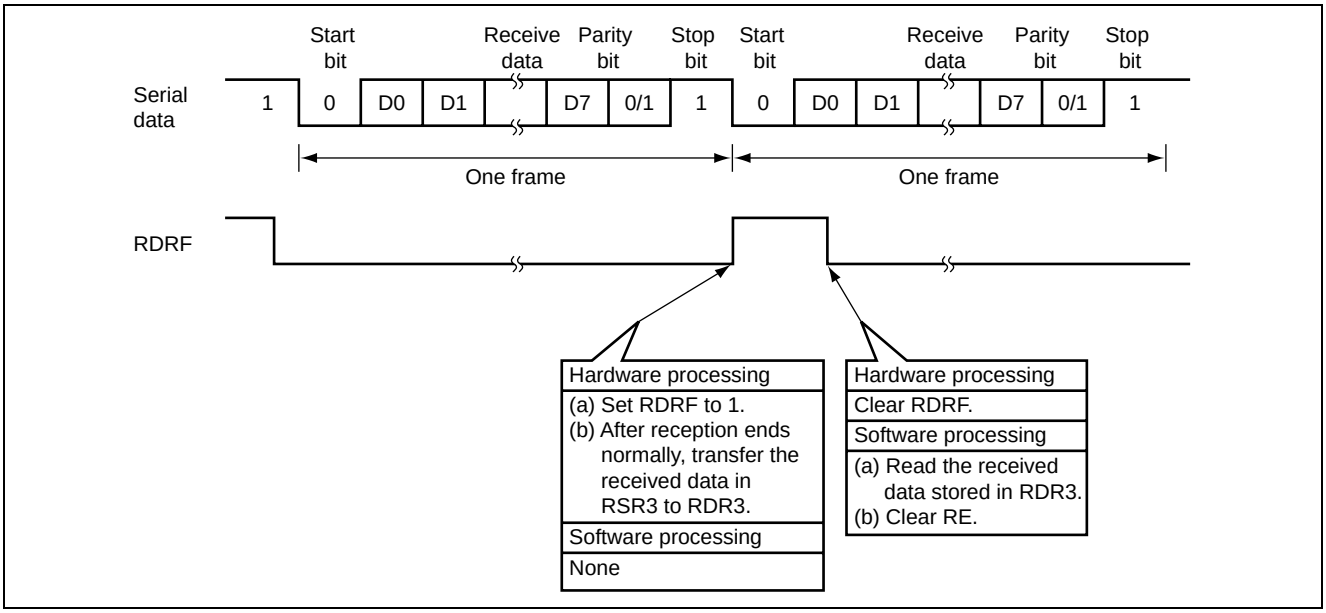


Figure 5 Operation of Asynchronous Serial Data Reception

4. Description of Software

4.1 Modules

Table 2 describes the modules of this sample task.

Table 2 Description of Modules

Function Name	Description
main	Stops the watchdog timer, initializes RAM area to be used, controls interrupts, and performs asynchronous serial data communication.
SCI3_init	Initializes the SCI3 and clears SCI3 module standby state.
transmit	Transmits serial data.
receive	Receives serial data.
ActiveHighToSubactive	Makes a transition from active (high-speed) mode to subactive mode.
dtint	Direct transition interrupt processing

4.2 Arguments

Table 3 describes the argument used in this sample task.

Table 3 Description of Argument

Label Name	Description	Used in
unsigned char trs_data	Transmit data	transmit

4.3 Internal Registers

The following describes internal registers used in this sample task. Note that the settings in the tables are the values used in this sample task and are different from the initial values.

- Serial Port Control Register (SPCR) Address H'FF91

Bit	Bit Name	Setting	R/W	Function
4	SPC3	1	R/W	P32/TXD3/IrTXD Pin Function Switch Selects whether the P32/TXD3/IrTXD pin is used as the P32 or TXD3/IrTXD pin. 1: TXD3/IrTXD output pin Set the TE bit in SCR after setting this bit to 1.

- Serial Mode Register 3 (SMR3) Address H'FF98

Bit	Bit Name	Setting	R/W	Function
7	COM	0 (Default)	R/W	Communication Mode 0: Asynchronous mode. 1: Clocked synchronous mode.
6	CHR	0 (Default)	R/W	Character Length (only valid in asynchronous mode) 0: Data length is 8 bits. 1: Data length is 7 bits.
5	PE	0 (Default)	R/W	Parity Enable (only valid in asynchronous mode) When this bit is set to 1, a parity bit is added in transmission, and parity check is done in reception.
3	STOP	0 (Default)	R/W	Stop Bit Length (only valid in asynchronous mode) Selects the stop bit length in transmission. 0: 1 stop bit 1: 2 stop bits In reception, only the first stop bit is checked regardless of the value in the bit. If the second stop bit is 0, it is treated as the start bit of the next received character.
1	CKS1	0	R/W	Clock Select 0 and 1
0	CKS0	1	R/W	These bits select the clock source for the internal baud rate generator. 00: ϕ clock (n = 0) 01: ϕw clock (n = 0) 10: ϕ/16 clock (n = 2) 11: ϕ/64 clock (n = 3) For the relationship between the setting of these bits and the baud rate, see the description of the bit rate register (BRR) in the Hardware Manual. “n” is the decimal representation of the setting of these bits and is the value of n in the description of BRR.

- Bit Rate Register 3 (BRR3) Address H'FF99

Bit	Bit Name	Setting	R/W	Function
7	bit7	0	R/W	BRR3 is an 8-bit readable/writable register that sets the bit rate.
6	bit6	0	R/W	In relation to the operating clock of the baud rate generator in asynchronous mode, which is selected by the CKS1 and CKS0 bits in SMR3, BRR3 sets a bit rate of 2400 bits/s.
5	bit5	0	R/W	
4	bit4	0	R/W	
3	bit3	0	R/W	
2	bit2	0	R/W	
1	bit1	0	R/W	
0	bit0	0	R/W	

- Serial Control Register 3 (SCR3) Address H'FF9A

Bit	Bit Name	Setting	R/W	Function
5	TE	1	R/W	Transmit Enable Transmission is enabled when this bit is set to 1.
4	RE	1	R/W	Receive Enable Reception is enabled when this bit is set to 1.
1	CKE1	0	R/W	Clock Enable 1 and 0
0	CKE0	0	R/W	These bits select the clock source. 00: Internal baud rate generator (SCK3 pin functions as an I/O port) 01: Internal baud rate generator (clock signal of the same frequency as the bit rate is output from the SCK3 pin) 10: External clock (clock signal with a frequency 16 times the bit rate should be input from the SCK3 pin) 11: Reserved

- Transmit Data Register 3 (TDR3) Address H'FF9B

Bit	Bit Name	Setting	R/W	Function
7	bit7	—	R/W	TDR3 is an 8-bit readable/writable register that stores data for transmission.
6	bit6	—	R/W	
5	bit5	—	R/W	
4	bit4	—	R/W	
3	bit3	—	R/W	
2	bit2	—	R/W	
1	bit1	—	R/W	
0	bit0	—	R/W	

- Serial Status Register 3 (SSR3) Address H'FF9C

Bit	Bit Name	Setting	R/W	Function
7	TDRE	—	R/(W)*	Transmit Data Register Empty Indicates whether transmit data is stored in TDR3. [Setting conditions] • When the TE bit in SCR3 is 0 • When data is transferred from TDR3 to TSR3 [Clearing conditions] • When 0 is written to TDRE after reading TDRE = 1 • When the transmit data is written to TDR3
6	RDRF	—	R/(W)*	Receive Data Register Full Indicates whether received data is stored in RDR3. [Setting condition] • When serial reception ends normally and received data is transferred from RSR3 to RDR3 [Clearing conditions] • When 0 is written to RDRF after reading RDRF = 1 • When data is read from RDR3
5	OER	0	R/(W)*	Overrun Error [Setting condition] • When an overrun error occurs during reception [Clearing condition] • When 0 is written to OER after reading OER = 1
4	FER	0	R/(W)*	Framing Error [Setting condition] • When a framing error occurs during reception [Clearing condition] • When 0 is written to FER after reading FER = 1
3	PER	0	R/(W)*	Parity Error [Setting condition] • When a parity error occurs during reception [Clearing condition] • When 0 is written to PER after reading PER = 1
2	TEND	—	R	Transmit End [Setting conditions] • When the TE bit in SCR3 is 0 • When the last bit of a transmit character is transmitted with TDRE = 1 [Clearing conditions] • When 0 is written to TDRE after reading TDRE = 1 • When transmit data is written to TDR3

Note: * Only 0 can be written to clear the flag.

- Receive Data Register 3 (RDR3) Address H'FF9D

Bit	Bit Name	Setting	R/W	Function
7	bit7	—	R	RDR3 is an 8-bit read-only register that stores received data.
6	bit6	—	R	
5	bit5	—	R	
4	bit4	—	R	
3	bit3	—	R	
2	bit2	—	R	
1	bit1	—	R	
0	bit0	—	R	

- Serial Extended Mode Register (SEMR) Address H'FFA6

Bit	Bit Name	Setting	R/W	Function
3	ABCS	1	R/W	Asynchronous Mode Basic Clock Select Selects the basic clock for the bit period in asynchronous mode. This setting is only valid in asynchronous mode (COM bit in SMR3 is 0). 0: Operates on a basic clock with a frequency of 16 times the transfer rate 1: Operates on a basic clock with a frequency of 8 times the transfer rate

- Timer Control/Status Register WD1 (TCSRWD1) Address H'FFB1

Bit	Bit Name	Setting	R/W	Function
7	B6WI	1	R/W	Bit 6 Write Disable Writing to the TCWE bit is only enabled when 0 is written to the B6WI bit. This bit is always read as 1.
6	TCWE	0	R/W	Timer Counter WD Write Enable Writing to the timer counter WD (TCWD) is enabled when the TCWE bit is set to 1. When writing to this bit, 0 must be written to the B6WI bit.
5	B4WI	1	R/W	Bit 4 Write Disable Writing to the TCSRWE bit is only enabled when 0 is written to the B4MI bit. The B4WI bit is always read as 1.
4	TCSRWE	0	R/W	Timer Control/Status Register WD1 Write Enable Writing to the WDON and WRST bits are enabled when the TCSRWE bit is set to 1. When writing to this bit, 0 must be written to the B4WI bit.
3	B2WI	1	R/W	Bit 2 Write Disable Writing to the WDON is only enabled when 0 is written to the B2WI bit. This bit is always read as 1.

Bit	Bit Name	Setting	R/W	Function
2	WDON	0	R/W	Watchdog Timer On The TDWD starts counting up when the WDON bit is set to 1 and stops counting when the WDON bit is cleared to 0. [Setting condition] • If 0 is written to the B2WI bit and 1 to the WDON bit while the TCSRWE bit is 1. • Reset [Clearing condition] • If 0 is written to the B2WI and WDON bits while the TCSRWE bit is 1.
1	B0WI	1	R/W	Bit 0 Write Disable Writing to the WRST bit is only enabled when 0 is written to the B0WI bit. This bit is always read as 1.
0	WRST	0	R/W	Watchdog Timer Reset [Setting condition] • When the TCWD overflows and an internal reset signal is generated. [Clearing condition] • Reset by the $\overline{\text{RES}}$ pin • If 0 is written to both the BOWI and WRST bits while the TCSRWE bit is 1.

- System Control Register 1 (SYSCR1) Address H'FFF0

Bit	Bit Name	Setting	R/W	Function
7	SSBY	1	R/W	Software Standby Selects to which the transition is made after the SLEEP instruction is executed. 1: Transition is made to standby mode or watch mode.
3	LSON	1	R/W	Selects the system clock (ϕ) or subclock (ϕw) as the CPU operating clock after watch mode is cleared. 1: The CPU operates on the subclock (ϕw)
2	TMA3	1	R/W	Selects the mode to which the transition is made after the SLEEP instruction is executed, in combination with bits SSBY and LSON in SYSCR1 and bits DTON and MSON in SYSCR2.

- System Control Register 2 (SYSCR2) Address H'FFF1

Bit	Bit Name	Setting	R/W	Function
3	DTON	1	R/W	Direct Transfer ON Flag Selects the mode to which the transition is made after the SLEEP instruction is executed, in combination with bits SSBY, TMA3, and LSON in SYSCR1 and bit MSON in SYSCR2.
1	SA1	1	R/W	Subactive Mode Clock Select 1 and 0
0	SA0	1	R/W	These bits select the operating clock frequency in subactive and subsleep modes. The operating clock frequency changes to the set frequency after the SLEEP instruction is executed. 11: ϕw

- Clock Halt Register 1 (CKSTPR1) Address H'FFFA

Bit	Bit Name	Setting	R/W	Function
6	S3CKSTP	1	R/W	SCI3 Module Standby The SCI3 enters standby mode when this bit is cleared to 0. 1: Clears module standby state.

4.4 RAM Usage

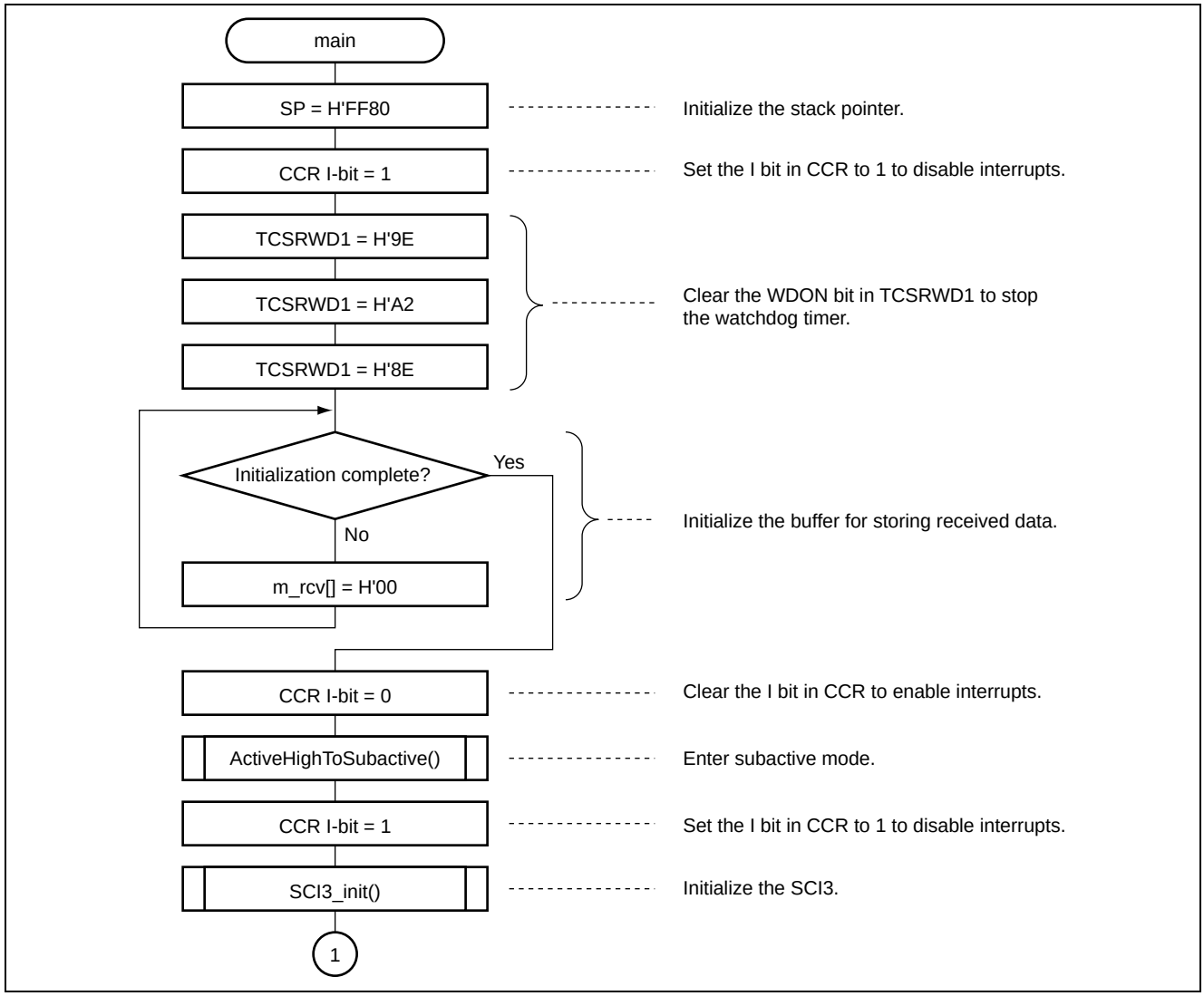
Table 4 describes the RAM usage in this sample task.

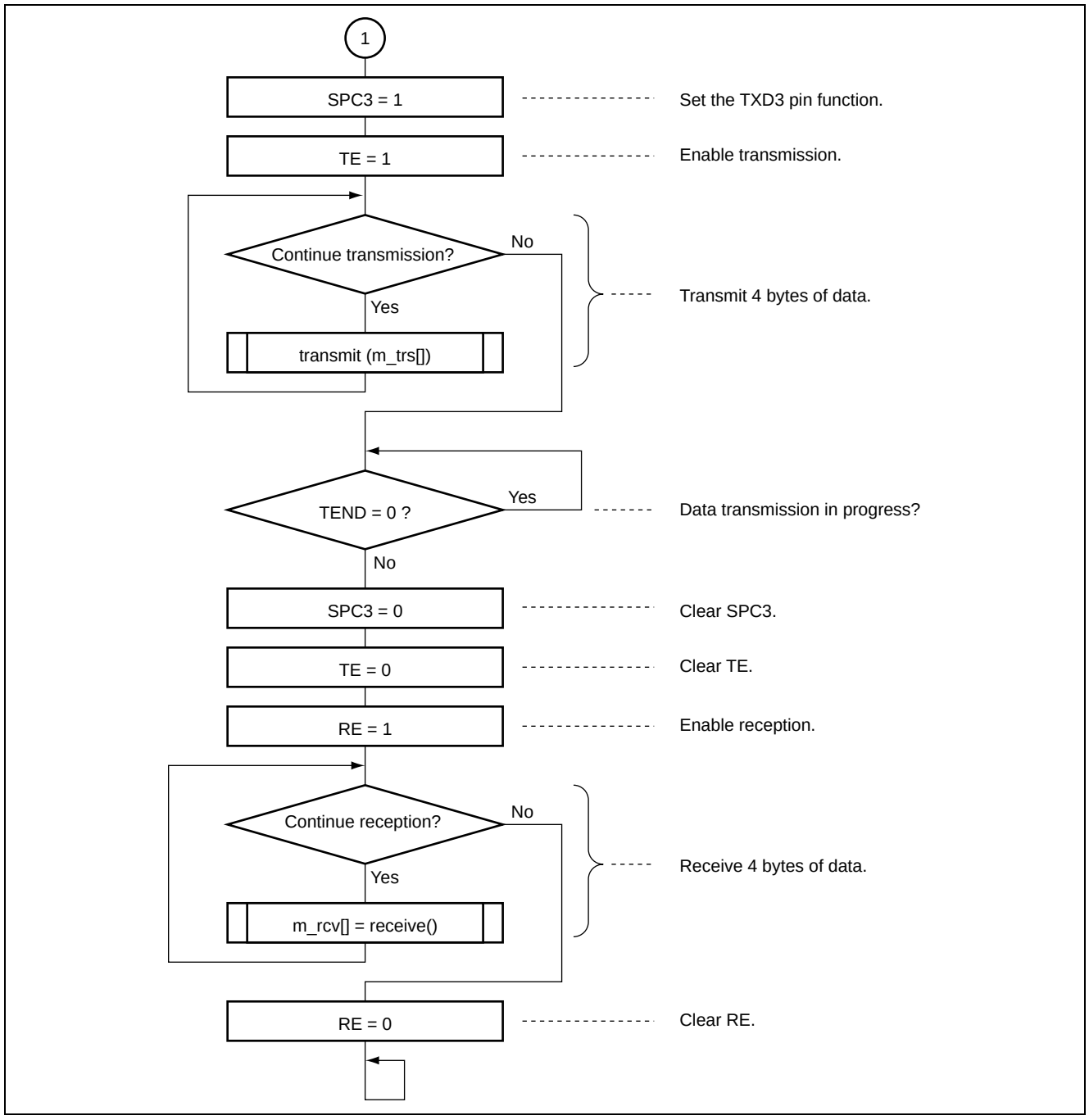
Table 4 Description of RAM

Label Name	Function	Data Length	Used In
m_trs[0] to m_trs[3]	Stores data for asynchronous serial transmission	4 bytes	main
m_rcv[0] to m_rcv[3]	Stores data for asynchronous serial reception	4 bytes	main

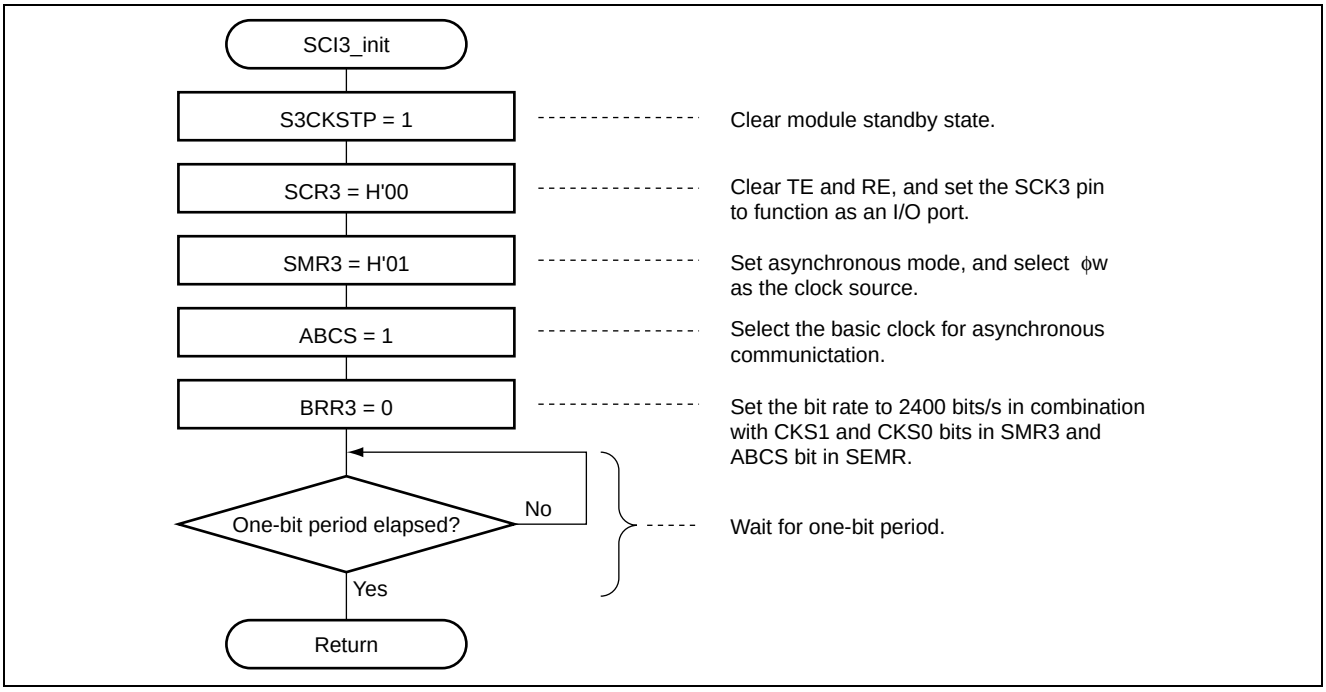
5. Flowchart

5.1 main

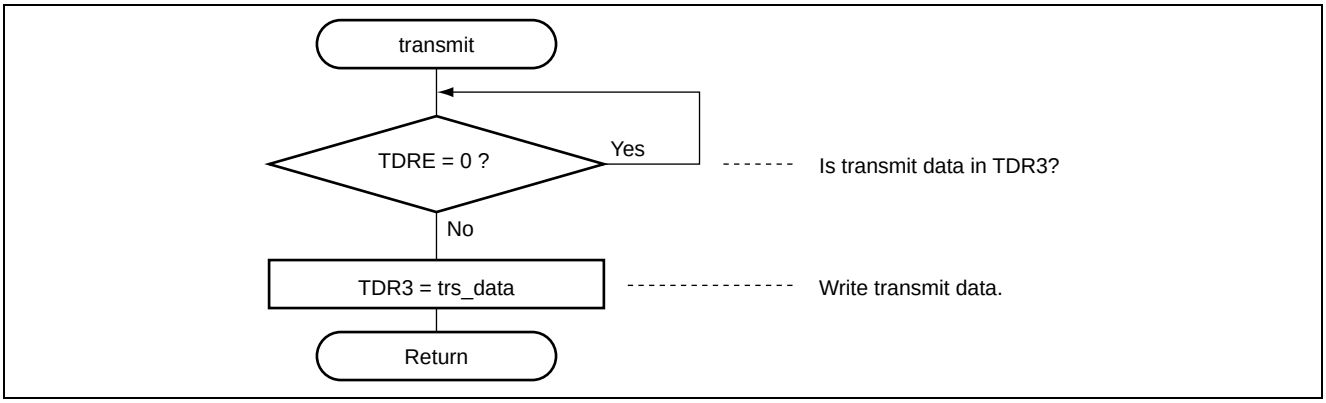



1
SPC3 = 1
Set the TXD3 pin function.
TE = 1
Enable transmission.
Continue transmission?
No
Yes
transmit (m_trs[])
Transmit 4 bytes of data.
TEND = 0 ?
Yes
Data transmission in progress?
No
SPC3 = 0
Clear SPC3.
TE = 0
Clear TE.
RE = 1
Enable reception.
Continue reception?
No
Yes
m_rcv[] = receive()
Receive 4 bytes of data.
RE = 0
Clear RE.

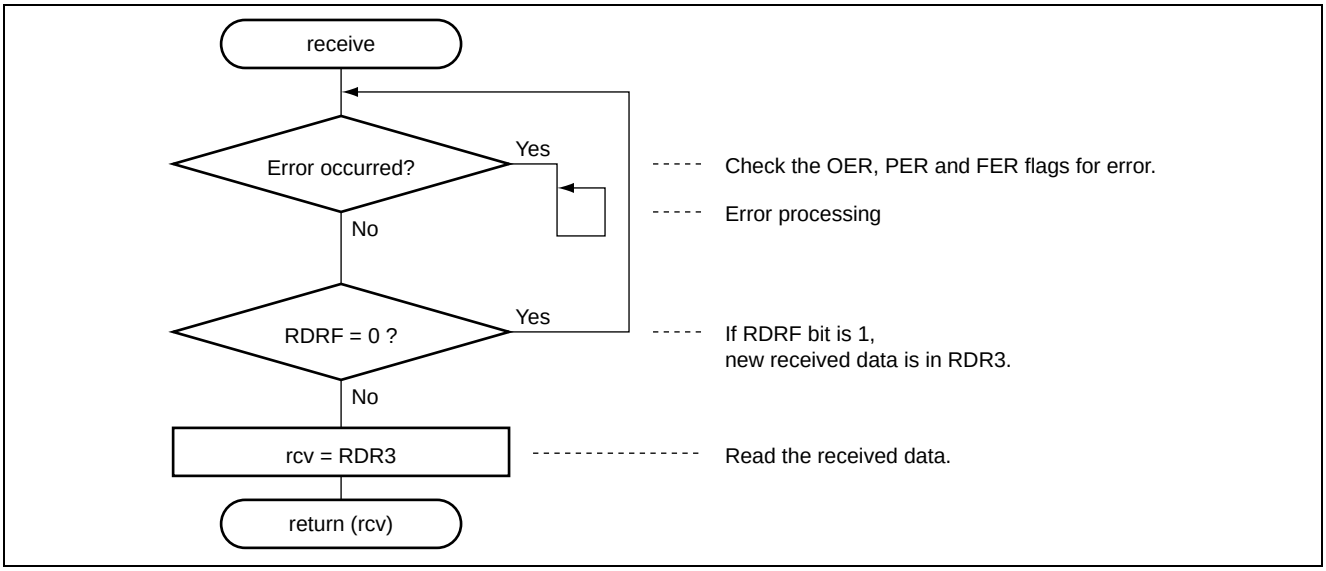
5.2 SCI3_init



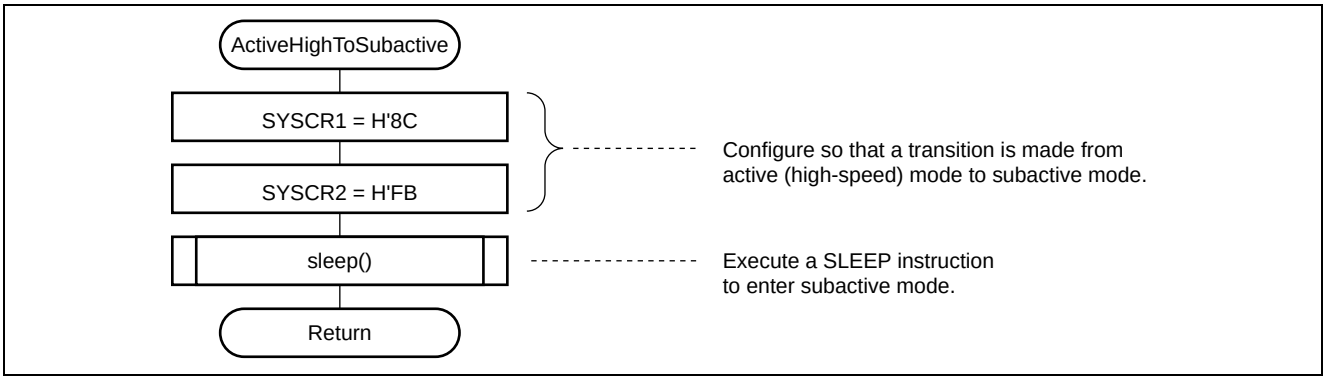
5.3 transmit



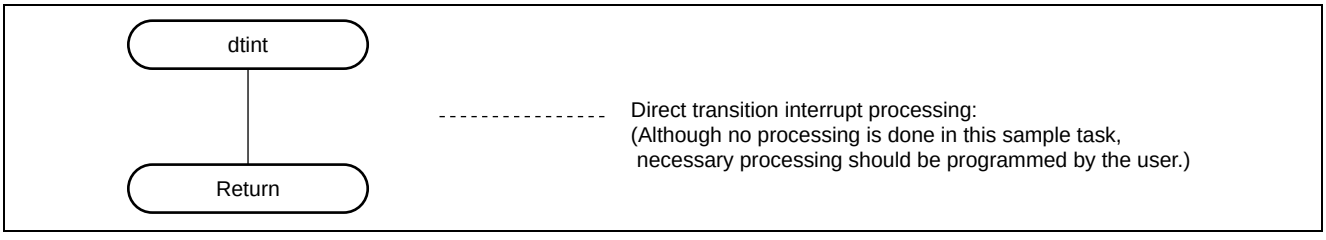
5.4 Receive



5.5 ActiveHighToSubactive



5.6 dtint



5.7 Link Address Specification

Section Name	Address
CVECT	H'0000
P	H'0100
D, B	H'FB80

Revision Record

Rev.	Date	Description	
		Page	Summary
1.00	Mar.18.05	—	First edition issued

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