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H8/38602R Group

A/D Conversion Using Subclock

Introduction

This application note discusses A/D conversion in subactive mode. The subclock is generated by the subclock oscillator circuit that uses a 32.768-kHz crystal resonator. A variable resistor is connected to analog input pin 0 (AN0) and A/D conversion is carried out every 0.5 seconds, with the results of the A/D conversion being stored to on-chip RAM.

Target Device

H8/38602R

Contents

1. Specifications

A/D conversion is carried out in subactive mode. The subclock is generated by the subclock oscillator circuit that uses a 32.768-kHz crystal resonator. A variable resistor is connected to analog input pin 0 (AN0) and A/D conversion is carried out every 0.5 seconds, with the results of A/D conversion being stored to on-chip RAM. The 0.5-second periodic interrupt function of the RTC is used to provide the 0.5-second periodic timing. Figure 1 shows a block diagram of the A/D conversion operation with subclock.

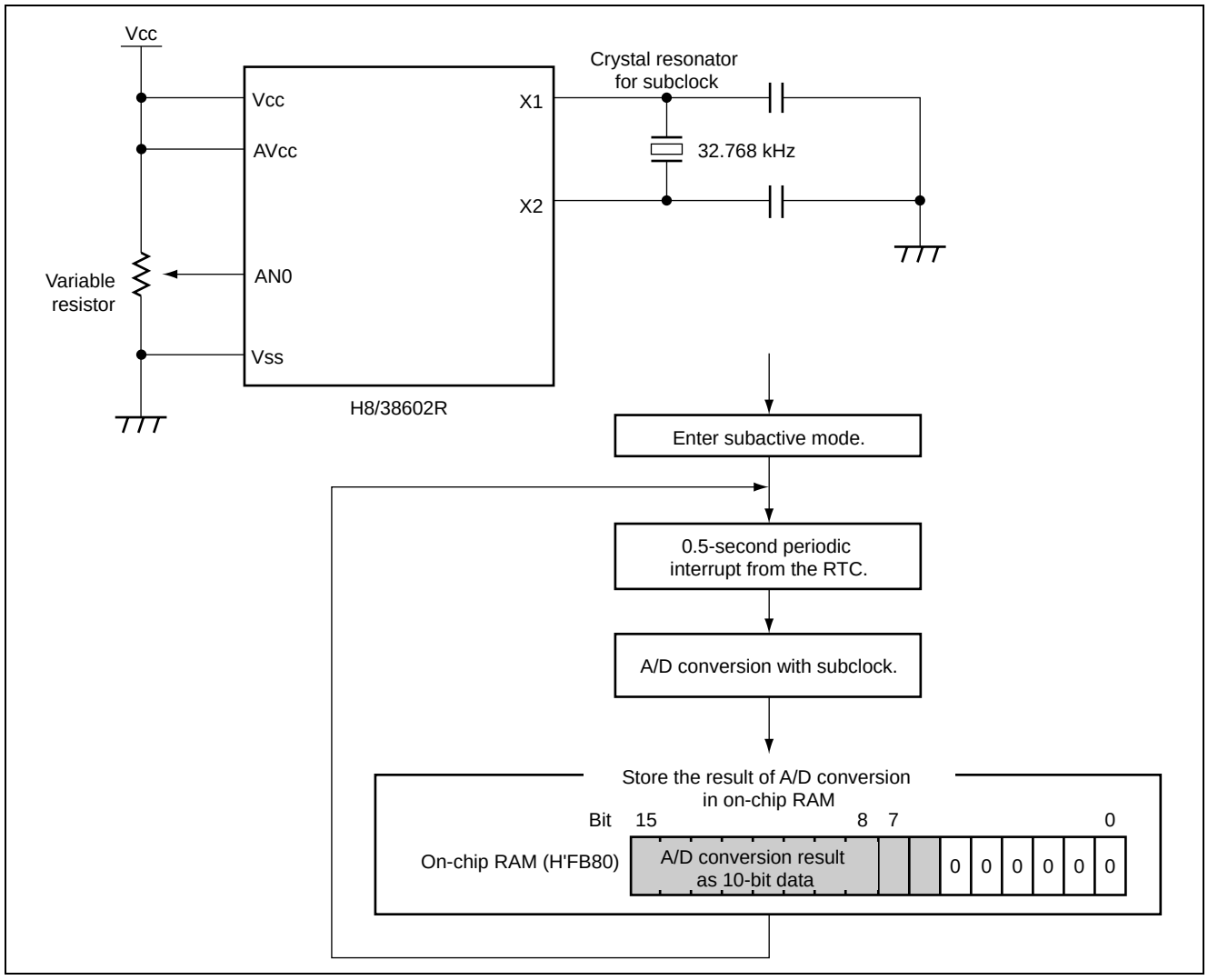


Figure 1 A/D Conversion with Subclock

2. Description of Functions

2.1 Functions

This sample task performs A/D conversion in subactive mode. The subclock is generated by the subclock oscillator circuit that uses a 32.768 kHz crystal resonator. A variable resistor is connected to analog input pin 0 (AN0) and A/D conversion is carried out every 0.5 seconds, with the results of the A/D conversion being stored in the on-chip RAM. The 0.5-second periodic interrupt function of the RTC is used to provide the 0.5-second periodic timing.

2.1.1 A/D Converter Function

The H8/38602R includes a successive approximation type 10-bit A/D converter that allows up to six analog input channels to be selected. A block diagram of the A/D converter is shown in figure 2.

- A/D Result Register (ADRR)
  ADRR is a 16-bit read-only register that stores the result of A/D conversion. The upper 10 bits of the data are stored in ADRR. ADRR can be read by the CPU at any time, but the ADRR value during A/D conversion is undefined. When A/D conversion is completed, the conversion result is stored as 10-bit data, and this data is retained until the next conversion starts. The initial value of ADRR is undefined. ADRR must be read in a word unit.
- A/D Mode Register (AMR)
  AMR specifies the A/D conversion time, and selects the external trigger and analog input pins.
- A/D Start Register (ADSR)
  ADSR controls the start/stop of A/D conversion, and selects whether ladder resistor operates or is halted.

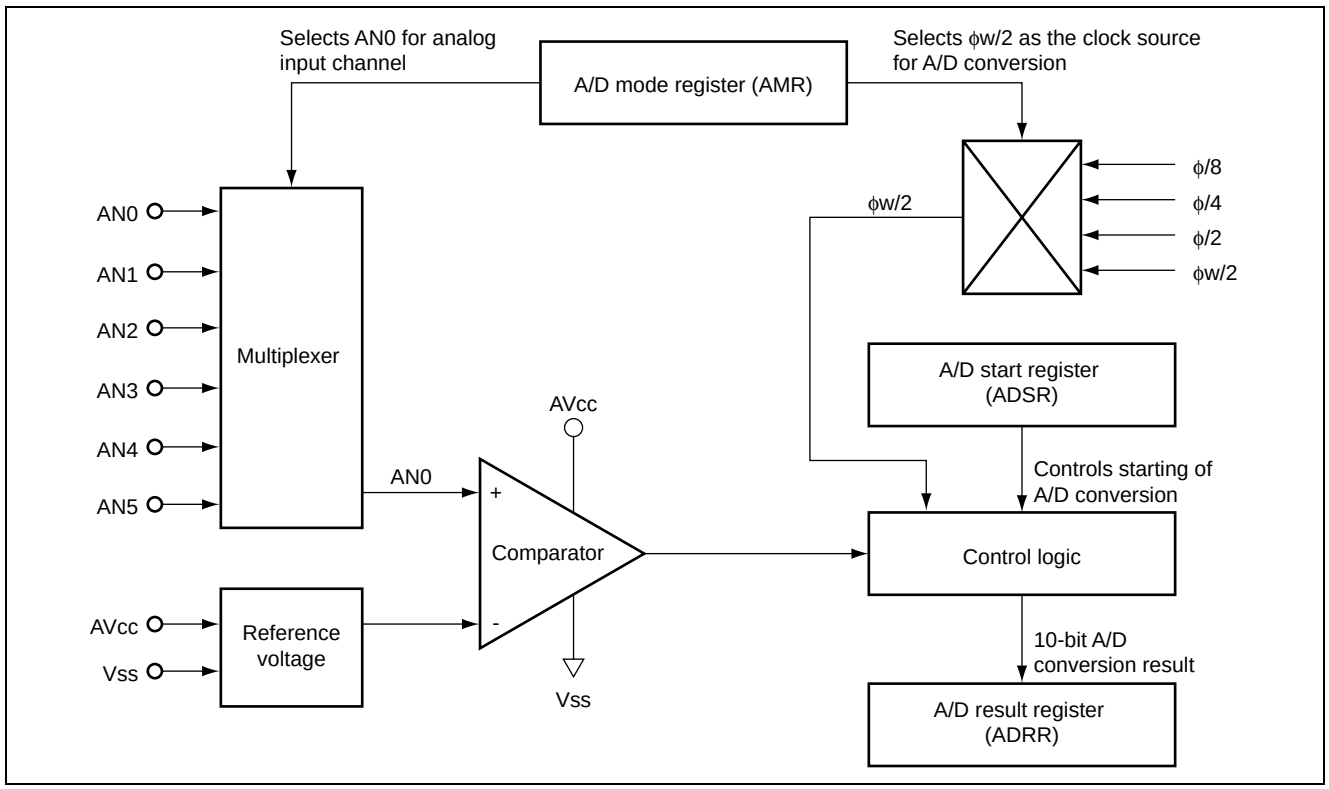


Figure 2 Block Diagram of A/D Converter

2.1.2 Module Standby Function

The module standby function places the A/D converter in the module standby mode after the reset is released. The module standby mode of the A/D converter can be cleared by setting the ADCKSTP bit in clock halt register 1 (CKSTPR1) to 1.

- Clock Halt Register 1 (CKSTPR1)
  CKSTPR1 allows the on-chip peripheral modules to enter standby mode in module units.

2.1.3 Watchdog Timer Function

The H8/38602R includes a watchdog timer. The watchdog timer is active after reset. The timer counter WD (TCWD) is incremented and, if the TCWD overflows, the H8/38602R is internally reset. This sample task does not use the watchdog timer function, and thus stops this timer.

- Timer Control/Status Register WD1 (TCSRWD1)
  TCSRWD1 controls writing to TCSRWD1 and TCWD. TCSRWD1 also controls the watchdog timer operation and indicates the operating status. TCSRWD1 must be rewritten by using the MOV instruction. Bit manipulation instructions cannot be used to change the setting value.

2.1.4 Power-Down Mode (Subactive Mode) Function

In subactive mode, the system clock oscillator stops but on-chip peripheral modules except for the IIC2 operate. As long as a required voltage is applied, the contents of some registers of the on-chip peripheral modules are retained.

Subactive mode is cleared by the SLEEP instruction. When subactive mode is cleared, a transition to subsleep mode, active mode, or watch mode is made, depending on the combination of bits SSBY, LSON, and TMA3 in SYSCR1 and bits MSON and DTON in SYSCR2. Subactive mode will not be cleared if the I bit in CCR is set to 1 or the associated interrupt is disabled by the interrupt enable register.

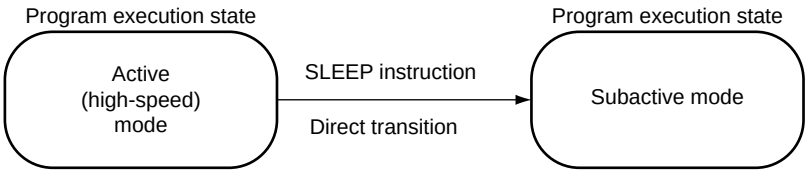
The operating frequency of subactive mode is selected from among ϕw (watch clock), $\phi w/2$, $\phi w/4$, and $\phi w/8$ by the SA1 and SA0 bits in SYSCR2. After the SLEEP instruction is executed, the operating frequency changes to the frequency that is set before the execution.

In this sample task, a direct transition is made from active (high-speed) mode to subactive mode. The CPU can execute programs in two modes: active and subactive mode. A direct transition is a transition between these two modes without stopping program execution. A direct transition is made by executing a SLEEP instruction while the DTON bit in SYSCR2 is set to 1. The direct transition can also be used to change the operating frequency in active or subactive mode. After the mode transition, direct transition interrupt exception handling starts. Note that if a direct transition is attempted while the I bit in CCR is set to 1, sleep or watch mode will be entered, and the resulting mode cannot be cleared by means of an interrupt.

When a SLEEP instruction is executed in active (high-speed) mode while the SSBY, TMA3, and LSON bits in SYSCR1 are set to 1 and the DTON bit in SYSCR2 is set to 1, a transition is made to subactive mode via watch mode.

Figure 3 shows a block diagram of direct transition from active (high-speed) mode to subactive mode.

- System Control Register 1 (SYSCR1)
  SYSCR1 controls the power-down modes, in combination with SYSCR2.
- System Control Register 2 (SYSCR2)
  SYSCR2 controls the power-down modes, in combination with SYSCR1.



Mode transition conditions

LSON	MSON	SSBY	TMA3	DTON
1	X	1	1	1

[Legend] X: Don't care

Figure 3 Direct Transition from Active (High-Speed) Mode to Subactive Mode

2.1.5 RTC Clock Output Function

This sample task uses the 0.5-second periodic interrupts generated by the RTC to perform A/D conversion with use of subclock.

- RTC Control Register 1 (RTCCR1)
  RTCCR1 controls the start/stop of the clock timer, selects 12-hour/24-hour mode, controls reset of the RTC, and sets the interrupt generation timing.
- RTC Control Register 2 (RTCCR2)
  RTCCR2 controls the RTC's periodic interrupts which are generated at intervals of a week, day, hour, minute, one second, 0.5 seconds, and 0.25 seconds. If these interrupts are enabled, the corresponding flag in the RTC interrupt flag register (RTCFLG) is set to 1 when the interrupt occurs.
- Clock Source Select Register (RTCCSR)
  RTCCSR selects the clock source.
- RTC Interrupt Flag Register (RTCFLG)
  When an RTC interrupt occurs, the corresponding flag in this register is set. Each flag is not cleared automatically even if the interrupt is accepted. To clear the flag, 0 should be written to the flag.

2.1.6 Exception Handling Function

In this sample task, A/D conversion with subclock takes place as the interrupt service processing for the 0.5-second periodic interrupt from the RTC.

- Interrupt Enable Register 1 (IENR1)
  IENR1 enables the RTC interrupts.

2.2 Assignment of Functions

Table 1 lists the function assignment for this sample task. By assigning the functions as shown in table 1, the H8/38602R performs A/D conversion with use of a subclock.

Table 1 Assignment of Functions

Register	Description
ADRR	Stores 10-bit A/D conversion result.
AMR	Selects AN0 as the analog input channel and ϕw/2 as the clock source for A/D conversion.
ADSR	Starts/stops the A/D conversion.
CKSTPR1	Clears module standby mode of the A/D converter.
TCSRWD1	Stops the watchdog timer.
SYSCR1	Controls direct transition to subactive mode in combination with SYSCR2.
SYSCR2	Controls direct transition to subactive mode in combination with SYSCR1.
RTCCR1	Controls the start/stop and reset of the clock timer.
RTCCR2	Enables 0.5-second periodic interrupt requests.
RTCCSR	Selects 32.768-kHz RTC operation.
RTCFLG	Register containing the status flag for the 0.5-second periodic interrupt request
IENR1	Enables RTC interrupt requests.

3. Principles of Operation

This sample task performs A/D conversion in subactive mode. The subclock is generated by the subclock oscillator circuit that uses a 32.768-kHz crystal resonator. A variable resistor is connected to analog input pin 0 (AN0) and A/D conversion is carried out every 0.5 seconds, with the results of A/D conversion being stored in on-chip RAM. The 0.5-second periodic interrupt function of the RTC is used to provide the 0.5-second periodic timing. Figure 4 illustrates the A/D conversion operation with use of subclock.

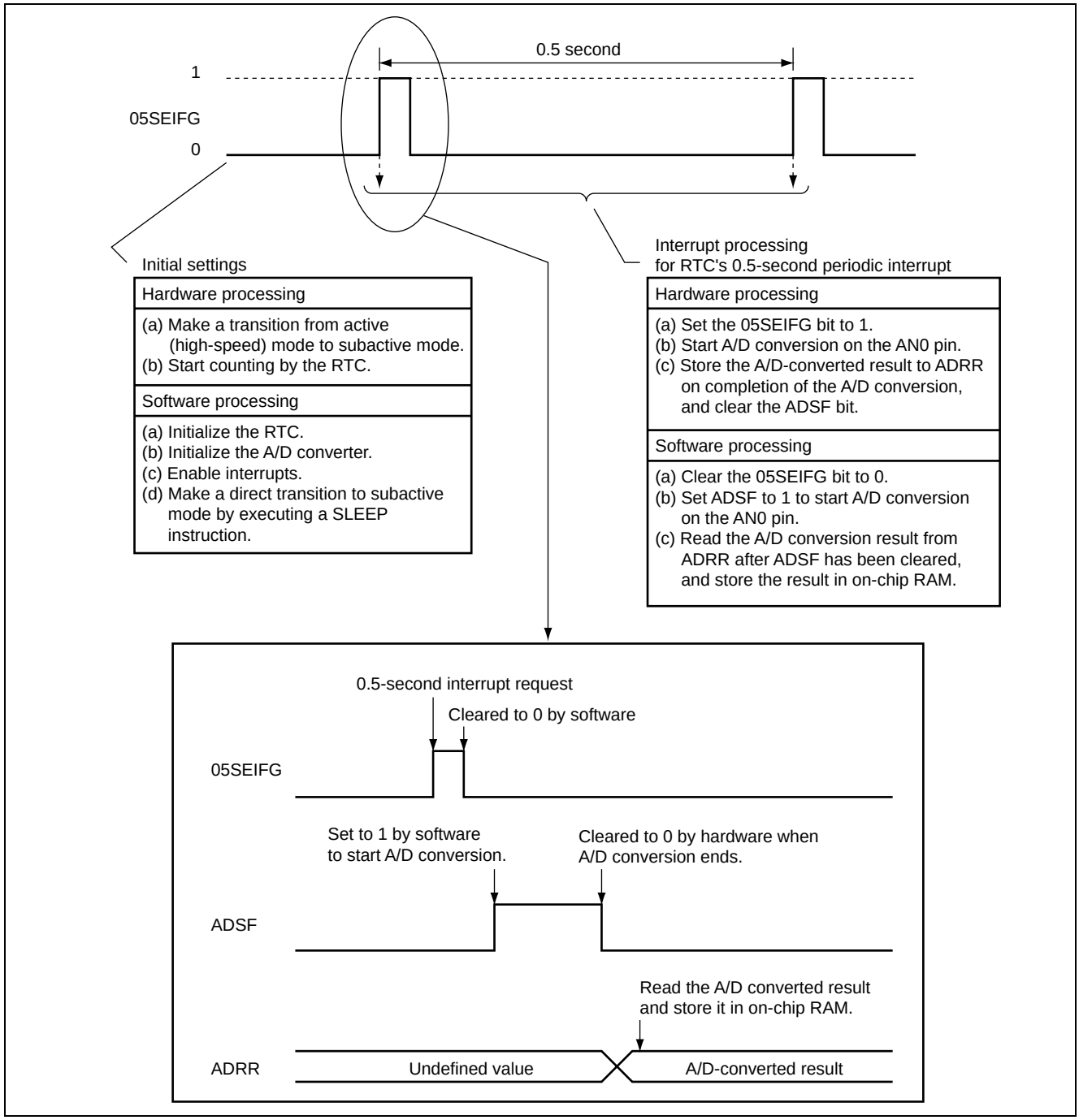


Figure 4 Principles of Operation

4. Description of Software

4.1 Modules

Table 2 describes the modules of this sample task.

Table 2 Description of Modules

Function Name	Description
main	Stops the watchdog timer, clears A/D converter module standby mode, configures the RTC and A/D converter, enables interrupts, and makes a direct transition to subactive mode.
int_rtc	0.5-second periodic interrupt processing: starts A/D conversion on the AN0 pin and stores the A/D converted-result in on-chip RAM.
int_sleep	Direct transition interrupt processing

4.2 Arguments

This sample task does not use arguments.

4.3 Internal Registers

The following describes internal registers used in this sample task.

- A/D Result Register (ADRR) Address H'FFBC

Bit	Bit Name	Setting	R/W	Function
15	ADR9	—	R	ADRR is a 16-bit read-only register that stores the result of A/D conversion. The upper 10 bits of the data are stored in ADRR. ADRR can be read by the CPU at any time, but the ADRR value during A/D conversion is undefined. When A/D conversion is completed, the conversion result is stored as 10-bit data, and this data is retained until the next conversion is started. The initial value of ADRR is undefined. This register must be read in a word unit.
14	ADR8	—	R	
13	ADR7	—	R	
12	ADR6	—	R	
11	ADR5	—	R	
10	ADR4	—	R	
9	ADR3	—	R	
8	ADR2	—	R	
7	ADR1	—	R	
6	ADR0	—	R	

- A/D Mode Register (AMR) Address H'FFBE

Bit	Bit Name	Setting	R/W	Function
5	CKS1	1	R/W	Clock Select
4	CKS0	1	R/W	These bits select the clock source for A/D conversion. 00: ϕ/8 (conversion time = 124 states (Max) (reference clock = ϕ) 01: ϕ/4 (conversion time = 62 states (Max) (reference clock = ϕ) 10: ϕ/2 (conversion time = 31 states (Max) (reference clock = ϕ) 11: ϕw/2 (conversion time = 31 states (Max) (reference clock = ϕ_{SUB}) In subactive or subsleep mode with CKS1 and CKS0 set to b'11, the A/D converter can only be used when the CPU operating clock is ϕw.
3	CH3	0	R/W	Channel Select 3 to 0
2	CH2	1	R/W	These bits select the analog input channel.
1	CH1	0	R/W	00xx: No channel selected
0	CH0	0	R/W	0100: AN0 0101: AN1 0110: AN2 0111: AN3 1000: AN4 1001: AN5 101x: No channel selected 11xx: No channel selected The channel selection should be changed while the ADSF bit is 0.

[Legend] x: Don't care.

- A/D Start Register (ADSR) Address H'FFBF

Bit	Bit Name	Setting	R/W	Function
7	ADSF	1	R/W	When this bit is set to 1, A/D conversion is started. When conversion is completed, the result of conversion is stored to ADRR and at the same time this bit is cleared to 0. A/D conversion can be forcibly terminated by writing 0 to this bit.
6	LADS	0	R/W	Ladder Resistor Select 0: Ladder resistor is connected while the A/D converter is idle. 1: Ladder resistor is disconnected while the A/D converter is idle. The ladder resistor is always disconnected in standby mode, watch mode, or module standby mode, and during a reset.

- Clock Halt Register 1 (CKSTPR1) Address H'FFFA

Bit	Bit Name	Setting	R/W	Function
4	ADCKSTP	1	R/W	A/D Converter Module Standby A/D converter enters standby mode when this bit is cleared to 0.

- Timer Control/Status Register WD1 (TCSRWD1) Address H'FFB1

Bit	Bit Name	Setting	R/W	Function
7	B6WI	1	R/W	Bit 6 Write Disable Writing to the TCWE bit is only enabled when 0 is written to the B6WI bit. This bit is always read as 1.
6	TCWE	0	R/W	Timer Counter WD Write Enable Writing to the timer counter WD (TCWD) is enabled when the TCWE bit is set to 1. When writing to this bit, 0 must be written to the B6WI bit.
5	B4WI	1	R/W	Bit 4 Write Disable Writing to the TCSRWE bit is only enabled when 0 is written to the B4MI bit. The B4WI bit is always read as 1.
4	TCSRWE	0	R/W	Timer Control/Status Register WD1 Write Enable Writing to the WDON and WRST bits are enabled when the TCSRWE bit is set to 1. When writing to this bit, 0 must be written to the B4WI bit.
3	B2WI	1	R/W	Bit 2 Write Disable Writing to the WDON is only enabled when 0 is written to the B2WI bit. This bit is always read as 1.
2	WDON	0	R/W	Watchdog Timer On The TDWD starts counting up when the WDON bit is set to 1 and stops counting when the WDON bit is cleared to 0. [Setting condition] • If 0 is written to the B2WI bit and 1 to the WDON bit while the TCSRWE bit is 1. • Reset [Clearing condition] • If 0 is written to the B2WI and WDON bits while the TCSRWE bit is 1.
1	B0WI	1	R/W	Bit 0 Write Disable Writing to the WRST bit is only enabled when 0 is written to the B0WI bit. This bit is always read as 1.
0	WRST	0	R/W	Watchdog Timer Reset [Setting condition] • When the TCWD overflows and an internal reset signal is generated. [Clearing condition] • Reset by the $\overline{\text{RES}}$ pin • If 0 is written to both the BOWI and WRST bits while the TCSRWE bit is 1.

- System Control Register 1 (SYSCR1) Address H'FFF0

Bit	Bit Name	Setting	R/W	Function
7	SSBY	1	R/W	Software Standby Selects the mode to which the transition is made after the SLEEP instruction is executed. 0: Transition is made to sleep mode or subsleep mode. 1: Transition is made to standby mode or watch mode.
3	LSON	1	R/W	Low Speed on Flag Selects the system clock (ϕ) or subclock (ϕSUB) as the CPU operating clock after watch mode is cleared. 0: The CPU operates on the system clock (ϕ). 1: The CPU operates on the subclock (ϕSUB).
2	TMA3	1	R/W	Selects the mode to which the transition is made after the SLEEP instruction is executed, in combination with bits SSBY and LSON in SYSCR1 and bits DTON and MSON in SYSCR2.

- System Control Register 2 (SYSCR2) Address H'FFF1

Bit	Bit Name	Setting	R/W	Function
3	DTON	1	R/W	Direct Transfer ON Flag Selects the mode to which the transition is made after the SLEEP instruction is executed, in combination with bits SSBY, TMA3, and LSON in SYSCR1 and bit MSON in SYSCR2.
2	MSON	0	R/W	Medium Speed ON Flag Selects whether the chip operates in active (high-speed) or active (medium-speed) mode after standby, watch, or sleep mode is cleared. 0: Active (high-speed) mode 1: Active (medium-speed) mode
1	SA1	1	R/W	Subactive Mode Clock Select 1 and 0
0	SA0	1	R/W	These bits select the operating clock frequency in subactive and subsleep modes. The operating clock frequency changes to the set frequency after the SLEEP instruction is executed. 00: ϕw/8 01: ϕw/4 10: ϕw/2 11: ϕw

- RTC Control Register 1 (RTCCR1) Address H'F06C

Bit	Bit Name	Setting	R/W	Function
7	RUN	1	R/W	RTC Operation Start 0: Stops RTC operation. 1: Starts RTC operation.
4	RST	0	R/W	Reset 0: Normal operation 1: Resets all the registers and control circuits of the RTC except RTCCSR and this bit. This bit must be cleared to 0 after set to 1.

- RTC Control Register 2 (RTCCR2) Address H'F06D

Bit	Bit Name	Setting	R/W	Function
1	05SEIE	1	R/W	0.5-Second Periodic Interrupt Enable 0: Disables 0.5-second periodic interrupts. 1: Enables 0.5-second periodic interrupts.

- Clock Source Select Register (RTCCSR) Address H'F06F

Bit	Bit Name	Setting	R/W	Function
3	RCS3	1	R/W	Clock Source Selection
2	RCS2	0	R/W	0000: ϕ/8 (Free running counter operation)
1	RCS1	0	R/W	0001: ϕ/32 (Free running counter operation)
0	RCS0	0	R/W	0010: ϕ/128 (Free running counter operation) 0011: ϕ/256 (Free running counter operation) 0100: ϕ/512 (Free running counter operation) 0101: ϕ/2048 (Free running counter operation) 0110: ϕ/4096 (Free running counter operation) 0111: ϕ/8192 (Free running counter operation) 1xxx: 32.768 kHz (RTC operation)

[Legend] x: Don't care.

- RTC Interrupt Flag Register (RTCFLG) Address H'F067

Bit	Bit Name	Setting	R/W	Function
1	05SEIFG	0	R/(W)*	[Setting condition] When a 0.5-second periodic interrupt occurs. [Clearing condition] 0 is written to 05SEIFG when 05SEIFG = 1

Note: * Only 0 can be written to clear the flag.

- Interrupt Enable Register 1 (IENR1) Address H'FFF3

Bit	Bit Name	Setting	R/W	Function
7	IENRTC	1	R/W	RTC Interrupt Request Enable RTC interrupt requests are enabled when this bit is set to 1.

4.4 RAM Usage

Table 3 describes the RAM usage in this sample task.

Table 3 Description of RAM

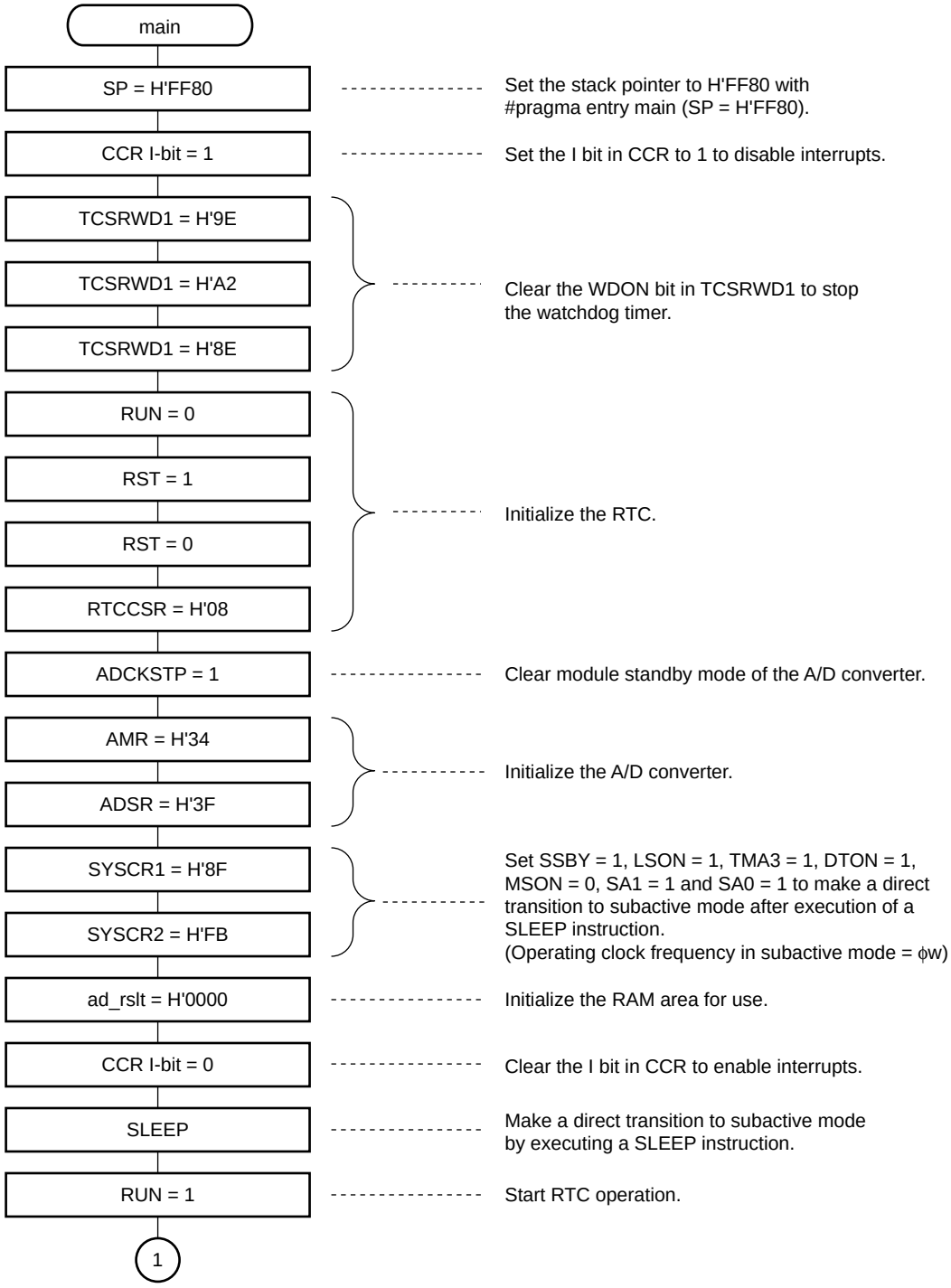
Label Name	Function	Size	Used In
ad_rslt	Stores the A/D-converted result as 10-bit data	1 word	main, int_rtc

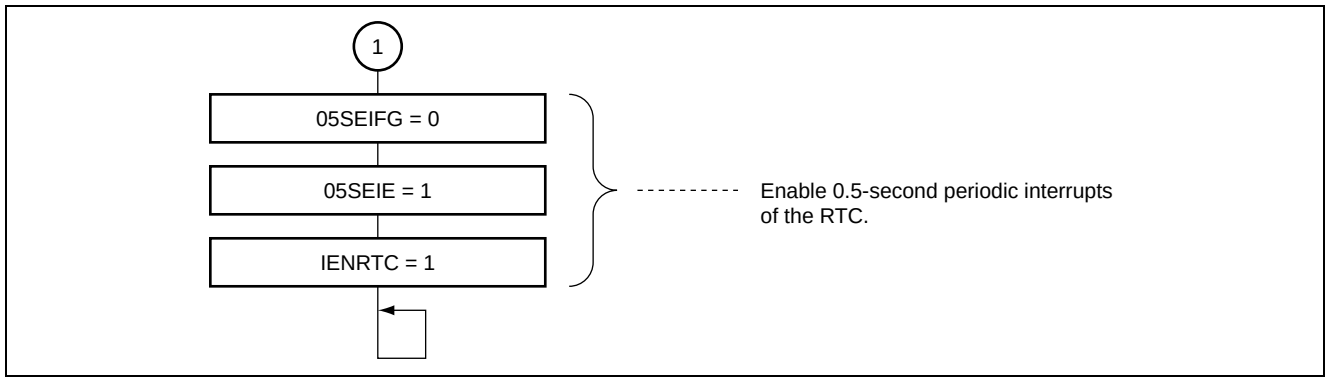
- A/D Conversion Result (ad_rslt) Address H'FB80

Bit	Bit Name	Setting	Function
15	ad_rslt9	0	Result of A/D Conversion
14	ad_rslt8	0	Stores the A/D-converted result as 10-bit data
13	ad_rslt7	0	
12	ad_rslt6	0	
11	ad_rslt5	0	
10	ad_rslt4	0	
9	ad_rslt3	0	
8	ad_rslt2	0	
7	ad_rslt1	0	
6	ad_rslt0	0	
5 to 0	—	0	Not used

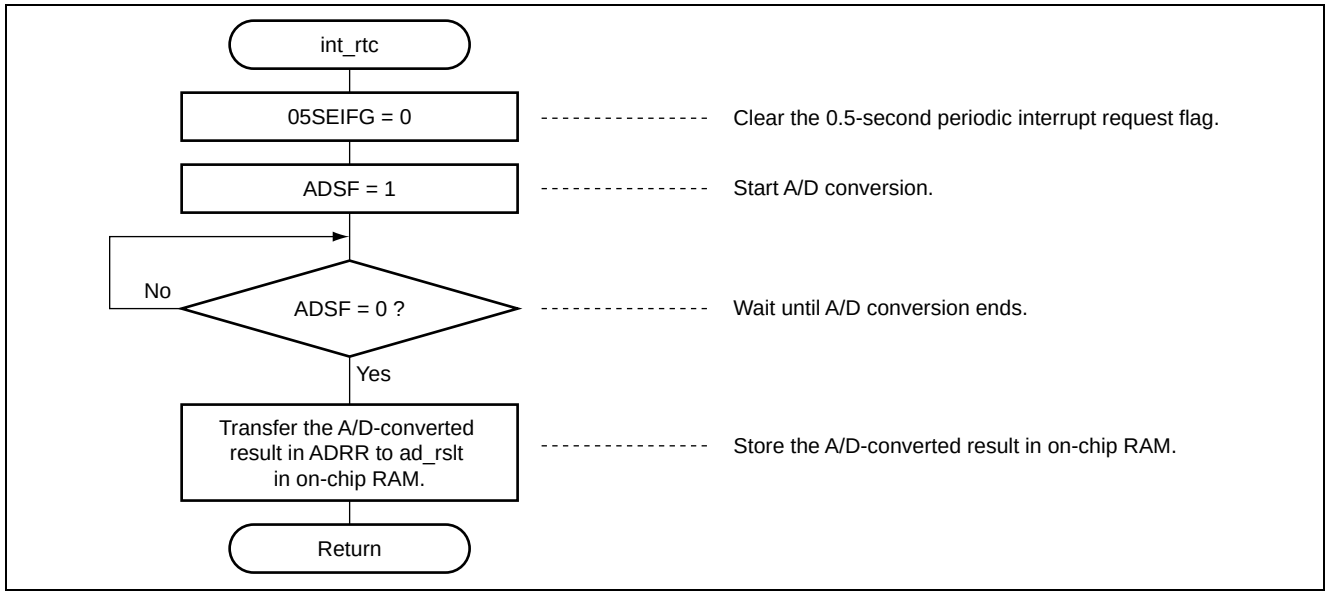
5. Flowchart

5.1 main

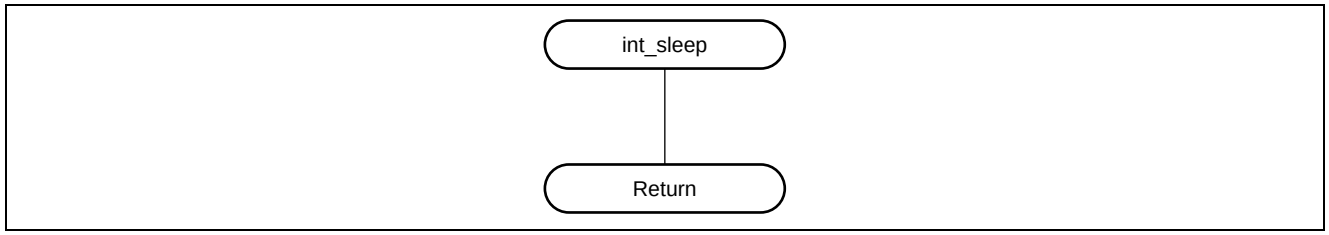




5.2 int_rtc



5.3 int_sleep



5.4 Link Address Specification

Section Name	Address
CVECT	H'0000
P	H'0100
B	H'FB80

Revision Record

		Description	
Rev.	Date	Page	Summary
1.00	Mar.18.05	—	First edition issued

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