To our customers,

Old Company Name in Catalogs and Other Documents

On April 1st, 2010, NEC Electronics Corporation merged with Renesas Technology Corporation, and Renesas Electronics Corporation took over all the business of both companies. Therefore, although the old company name remains in this document, it is a valid Renesas Electronics document. We appreciate your understanding.

Renesas Electronics website: http://www.renesas.com

April 1st, 2010
Renesas Electronics Corporation

Issued by: Renesas Electronics Corporation (http://www.renesas.com)

Send any inquiries to http://www.renesas.com/inquiry.

Notice

1. All information included in this document is current as of the date this document is issued. Such information, however, is subject to change without any prior notice. Before purchasing or using any Renesas Electronics products listed herein, please confirm the latest product information with a Renesas Electronics sales office. Also, please pay regular and careful attention to additional and different information to be disclosed by Renesas Electronics such as that disclosed through our website.
2. Renesas Electronics does not assume any liability for infringement of patents, copyrights, or other intellectual property rights of third parties by or arising from the use of Renesas Electronics products or technical information described in this document. No license, express, implied or otherwise, is granted hereby under any patents, copyrights or other intellectual property rights of Renesas Electronics or others.
3. You should not alter, modify, copy, or otherwise misappropriate any Renesas Electronics product, whether in whole or in part.
4. Descriptions of circuits, software and other related information in this document are provided only to illustrate the operation of semiconductor products and application examples. You are fully responsible for the incorporation of these circuits, software, and information in the design of your equipment. Renesas Electronics assumes no responsibility for any losses incurred by you or third parties arising from the use of these circuits, software, or information.
5. When exporting the products or technology described in this document, you should comply with the applicable export control laws and regulations and follow the procedures required by such laws and regulations. You should not use Renesas Electronics products or the technology described in this document for any purpose relating to military applications or use by the military, including but not limited to the development of weapons of mass destruction. Renesas Electronics products and technology may not be used for or incorporated into any products or systems whose manufacture, use, or sale is prohibited under any applicable domestic or foreign laws or regulations.
6. Renesas Electronics has used reasonable care in preparing the information included in this document, but Renesas Electronics does not warrant that such information is error free. Renesas Electronics assumes no liability whatsoever for any damages incurred by you resulting from errors in or omissions from the information included herein.
7. Renesas Electronics products are classified according to the following three quality grades: “Standard”, “High Quality”, and “Specific”. The recommended applications for each Renesas Electronics product depends on the product’s quality grade, as indicated below. You must check the quality grade of each Renesas Electronics product before using it in a particular application. You may not use any Renesas Electronics product for any application categorized as “Specific” without the prior written consent of Renesas Electronics. Further, you may not use any Renesas Electronics product for any application for which it is not intended without the prior written consent of Renesas Electronics. Renesas Electronics shall not be in any way liable for any damages or losses incurred by you or third parties arising from the use of any Renesas Electronics product for an application categorized as “Specific” or for which the product is not intended where you have failed to obtain the prior written consent of Renesas Electronics. The quality grade of each Renesas Electronics product is “Standard” unless otherwise expressly specified in a Renesas Electronics data sheets or data books, etc.

   “Standard”: Computers; office equipment; communications equipment; test and measurement equipment; audio and visual equipment; home electronic appliances; machine tools; personal electronic equipment; and industrial robots.

   “High Quality”: Transportation equipment (automobiles, trains, ships, etc.); traffic control systems; anti-disaster systems; anti-crime systems; safety equipment; and medical equipment not specifically designed for life support.

   “Specific”: Aircraft; aerospace equipment; submersible repeaters; nuclear reactor control systems; medical equipment or systems for life support (e.g. artificial life support devices or systems), surgical implantations, or healthcare intervention (e.g. excision, etc.), and any other applications or purposes that pose a direct threat to human life.
8. You should use the Renesas Electronics products described in this document within the range specified by Renesas Electronics, especially with respect to the maximum rating, operating supply voltage range, movement power voltage range, heat radiation characteristics, installation and other product characteristics. Renesas Electronics shall have no liability for malfunctions or damages arising out of the use of Renesas Electronics products beyond such specified ranges.
9. Although Renesas Electronics endeavors to improve the quality and reliability of its products, semiconductor products have specific characteristics such as the occurrence of failure at a certain rate and malfunctions under certain use conditions. Further, Renesas Electronics products are not subject to radiation resistance design. Please be sure to implement safety measures to guard them against the possibility of physical injury, and injury or damage caused by fire in the event of the failure of a Renesas Electronics product, such as safety design for hardware and software including but not limited to redundancy, fire control and malfunction prevention, appropriate treatment for aging degradation or any other appropriate measures. Because the evaluation of microcomputer software alone is very difficult, please evaluate the safety of the final products or system manufactured by you.
10. Please contact a Renesas Electronics sales office for details as to environmental matters such as the environmental compatibility of each Renesas Electronics product. Please use Renesas Electronics products in compliance with all applicable laws and regulations that regulate the inclusion or use of controlled substances, including without limitation, the EU RoHS Directive. Renesas Electronics assumes no liability for damages or losses occurring as a result of your noncompliance with applicable laws and regulations.
11. This document may not be reproduced or duplicated, in any form, in whole or in part, without prior written consent of Renesas Electronics.
12. Please contact a Renesas Electronics sales office if you have any questions regarding the information contained in this document or Renesas Electronics products, or if you have any other inquiries.

(Note 1) “Renesas Electronics” as used in this document means Renesas Electronics Corporation and also includes its majority-owned subsidiaries.

(Note 2) “Renesas Electronics product(s)” means any product developed or manufactured by or for Renesas Electronics.

H8/38076R

Master-Slave Communication Using I^2C Clock-Synchronous Serial Format

Introduction

In this example the I^2C2 (Inter IC Bus Interface 2) module of the H8/38076R is used for master-slave communication in I^2C clock-synchronous serial format.

Target Device

H8/38076R

Contents

1. Specifications

- The I^2C clock-synchronous serial format of the H8/38076R is used for communication between microcomputers as shown in figure 1.
- In this sample task 4 bytes of data are transmitted from an H8/38076R operating in the master mode and received by an H8/38076R operating in the slave mode.
- The slave H8/38076R then transmits the receive data to the master H8/38076R.
- The transfer clock frequency is 100 kHz.

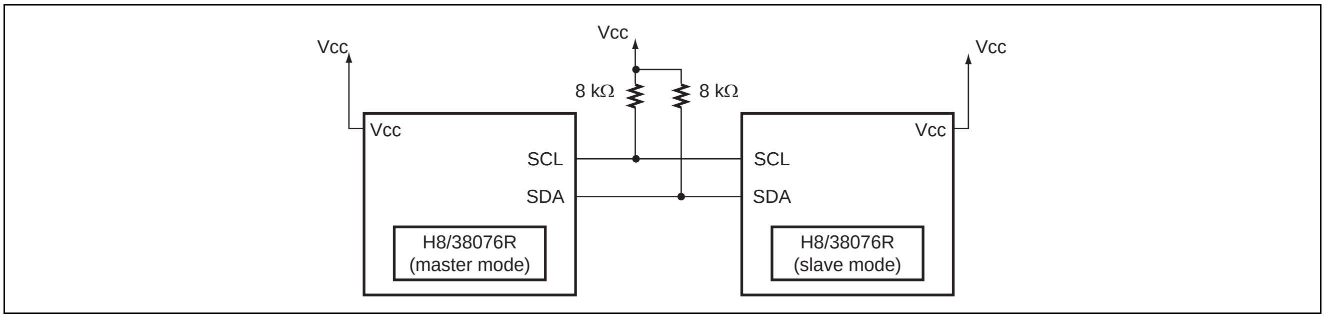


Figure 1 Connection Diagram for Master-Slave Communication Using the I^2C Clock-Synchronous Serial Format

2. Description of Functions

2.1 Functions Used

In this sample task the I^{2}C clock-synchronous serial format is used to implement master-slave communication. A block diagram of the I^{2}C bus interface 2 is shown in figure 2, and its functions are described below.

1. I^{2}C Bus Interface 2 Functions
   The I^{2}C bus interface 2 conforms to and provides a subset of the Philips I^{2}C bus (Inter IC Bus) interface functions.

- I^{2}C bus control register 1 (ICCR1)
  ICCR1 enables or disables the I^{2}C bus interface 2, controls transmission and reception, and selects the master mode or the slave mode, transmission or reception, and the transfer clock frequency in the master mode. In this sample task the transfer clock frequency is set to 100 kHz.

- I^{2}C bus control register 2 (ICCR2)
  ICCR2 manipulates the SDA pin, monitors the SCL pin state, and controls resets of the control block of the I^{2}C bus interface 2.

- I^{2}C bus mode register (ICMR)
  ICMR selects whether the MSB or LSB is transferred first and selects the transfer bit count. Note that BC (bit counter) must not be overwritten when using the clock-synchronous serial format.

- I^{2}C bus status register (ICSR)
  ICSR confirms interrupt request flags and status.

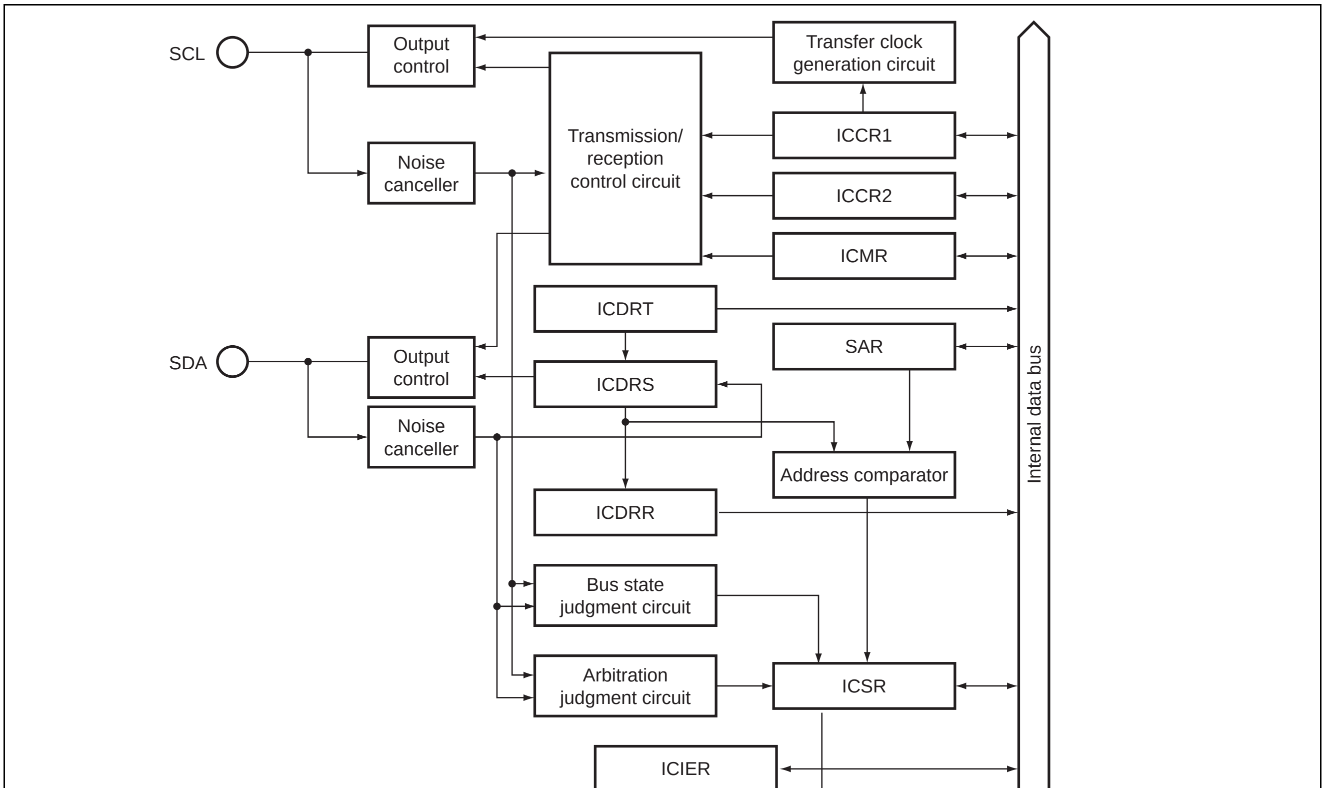
- I^{2}C bus interrupt enable register (ICIER)
  ICIER enables interrupt sources.

- I^{2}C bus transmit data register (ICDRT)
  ICDRT is an 8-bit readable/writable register that stores transmit data. When ICDRT detects space in the shift register (ICDRS) it transfers the transmit data which was written to ICDRT to ICDRS and starts transmitting data. Continuous transmission is possible if the next transmit data is written to ICDRT while data transfer to ICDRS is in progress. If the MLS bit of ICMR is set to 1, MSB/LSB inverted data is read after the data is written to ICDRT.

- I^{2}C bus receive data register (ICDRR)
  ICDRR is an 8-bit register that stores receive data. After one byte of data is received, ICDRR transfers the receive data from ICDRS to ICDRR and the next data can be received. ICDRR is a receive-only register, so the CPU cannot write to it.

- I^{2}C bus shift register (ICDRS)
  ICDRS is a register that is used to transmit and receive data. In transmission, data is transferred from ICDRT to ICDRS and the data is sent from the SDA pin. In reception, data is transferred from ICDRS to ICDRR after one byte of data is received. This register cannot be read directly from the CPU.

- Slave address register (SAR)
  SAR selects the communication format.



<Legend>
ICCR1: I^2C bus control register 1
ICCR2: I^2C bus control register 2
ICMR: I^2C bus mode register
ICSR: I^2C bus status register
ICIER: I^2C bus interrupt enable register
ICDRT: I^2C bus transmit data register
ICDRR: I^2C bus receive data register
ICDRS: I^2C bus shift register
SAR: Slave address register

Figure 2 Block Diagram of I^2C Bus Interface 2

2.2 Assignment of Functions

Table 1 shows the assignment of functions in this sample task.
Master-slave communication using the I^{2}C clock-synchronous serial format is implemented using functions assigned as shown in table 1. Figure 3 shows the transfer format for clock-synchronous serial communication.

Table 1 Assignment of Functions

Elements	Classification	Description
SCL	Pin	I^{2}C serial clock I/O pin
SDA	Pin	I^{2}C serial data I/O pin
ICRR1	I^{2}C2	Starts and stops operation of I^{2}C bus interface 2, controls transmission and reception, selects the master mode or the slave mode, selects master mode transfer clock frequency
ICRR2	I^{2}C2	Manipulates SDA pin
ICMR	I^{2}C2	Selects MSB or LSB first
ICSR	I^{2}C2	Status flag indicating the I^{2}C operation state
ICIER	I^{2}C2	Enables various interrupt sources
ICDRT	I^{2}C2	Register for storing transmit data
ICDRR	I^{2}C2	Register for storing receive data
ICDRS	I^{2}C2	Register for transmitting and receiving data
SAR	I^{2}C2	Selects format

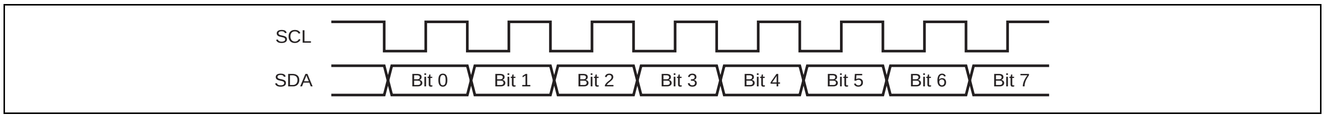


Figure 3 Clock-Synchronous Serial Transfer Format

3. Sequence Diagram

Figure 4 is a sequence diagram of this sample task.

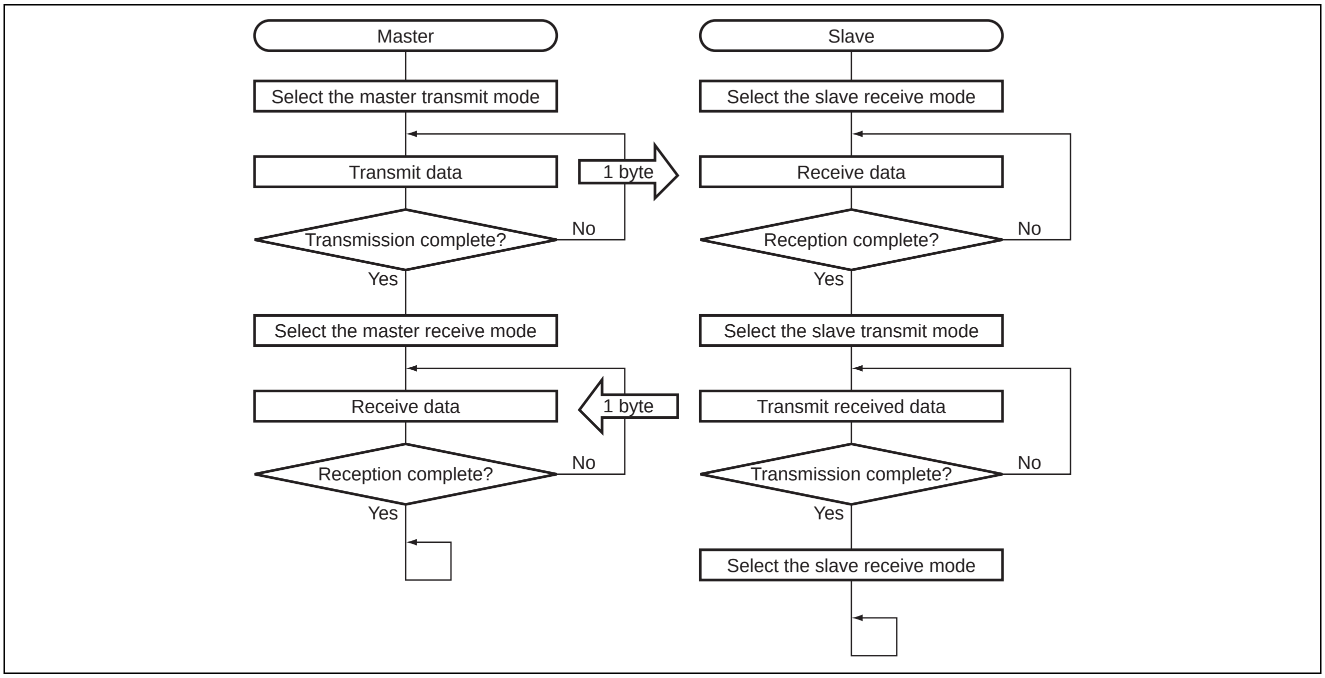
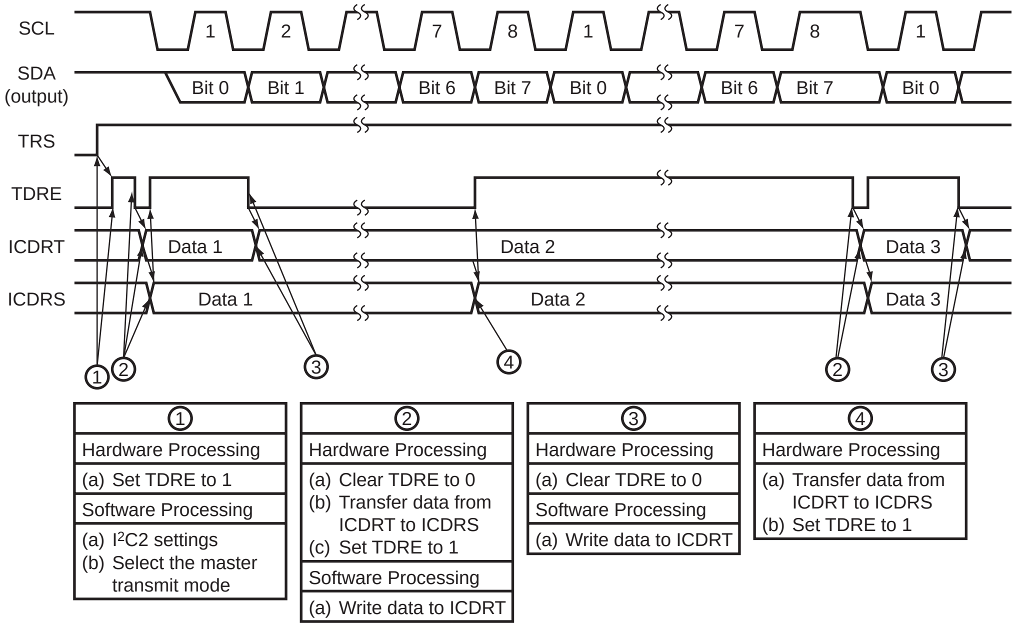


Figure 4 Sequence Diagram

4. Principles of Operation

4.1 Transmit Mode

The operation timing in the transmit mode for this sample task is illustrated in figure 5. Furthermore, details of the hardware and software processings are shown.



①
Hardware Processing
(a) Set TDRE to 1
Software Processing
(a) I^{2}C2 settings
(b) Select the master transmit mode

②
Hardware Processing
(a) Clear TDRE to 0
(b) Transfer data from ICDRT to ICDRS
(c) Set TDRE to 1
Software Processing
(a) Write data to ICDRT

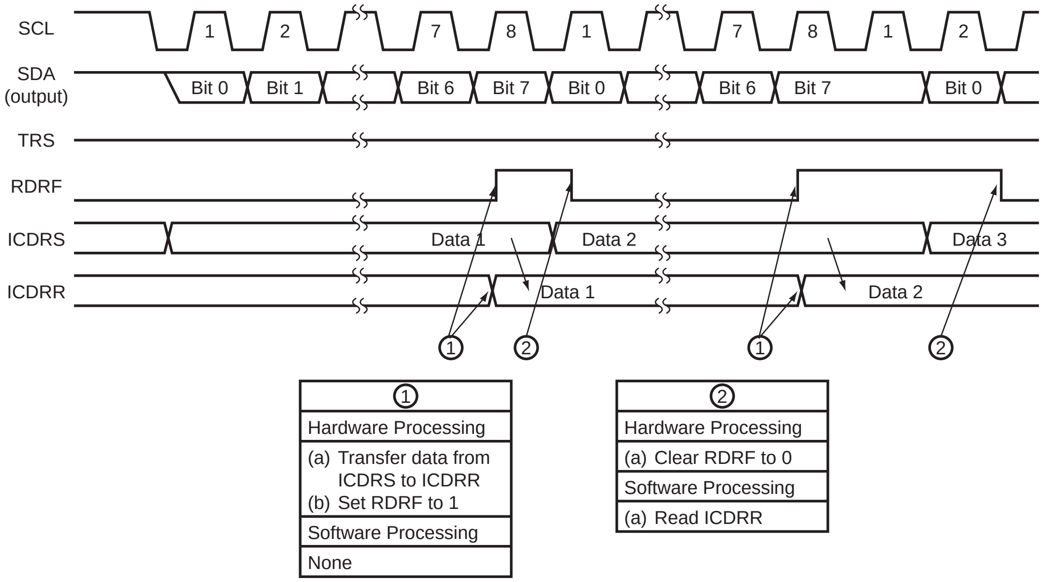
③
Hardware Processing
(a) Clear TDRE to 0
Software Processing
(a) Write data to ICDRT

④
Hardware Processing
(a) Transfer data from ICDRT to ICDRS
(b) Set TDRE to 1

Figure 5 Transmit Mode Operation Timing

4.2 Receive Mode

The operation timing in the receive mode for this sample task is illustrated in figure 6. Furthermore, details of the hardware and software processings are shown.



①
Hardware Processing
(a) Transfer data from ICDRS to ICDRR
(b) Set RDRF to 1
Software Processing
None

②
Hardware Processing
(a) Clear RDRF to 0
Software Processing
(a) Read ICDRR

Figure 6 Receive Mode Operation Timing

5. Description of Software (Master)

In this sample task I^{2}C clock-synchronous serial format initialization, master transmit, and master receive operations are performed. The functions used by the master programs are described below.

5.1 Functions

Table 2 List of Master Program Functions

Function Name	Description
main	Controls master communication
Clock_init	Initializes the I^{2}C clock-synchronous serial format
master_trs	Master transmission
master_rcv	Master reception

5.2 Constants

Table 3 shows the constants used in this sample task.

Table 3 Constants

Label Name	Constant Value	Description	Used in
SIZE	4	Transmit/receive data size	master_trs master_rcv

5.3 RAM Usage

Table 4 shows the RAM used in this sample task.

Table 4 RAM Usage

Label Name	Description	Amount of Memory Used	Used in
m_trs[SIZE]	Buffer for storing transmit data	4 bytes	master_trs
m_rcv[SIZE]	Buffer for storing receive data	4 bytes	master_rcv

5.4 Modules

5.4.1 main() Function

1. Module Specifications

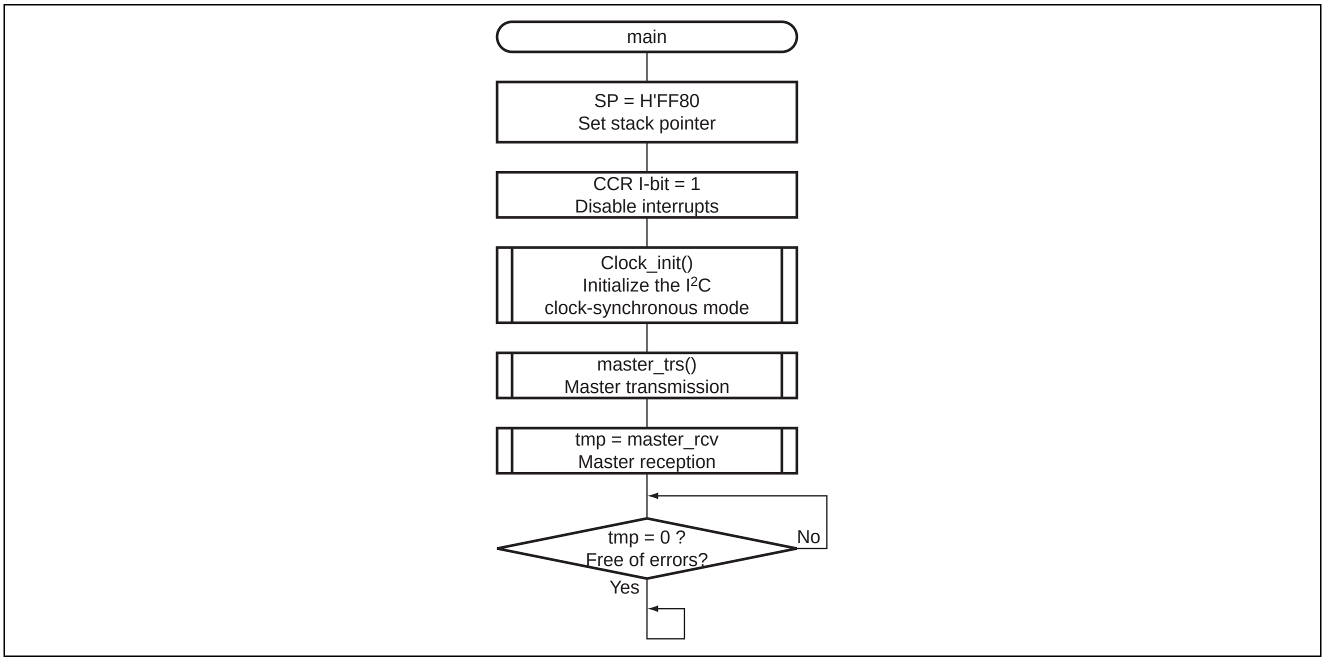
- Controls master communication

Table 5 Module Specifications

Item	Type	Variable	Description
Arguments	None	None	None

2. Internal Registers Used
   None

3. Flowchart



5.4.2 Clock_init() Function

1. Module Specifications

- Initializes the I^2C clock-synchronous serial format

Table 6 Module Specifications

Item	Type	Variable	Description
Arguments	None	None	None

2. Internal Registers Used

The internal registers used in this sample task are shown below. The set values shown are those used in the sample task and differ from the initial values.

- ICCR1 I^2C bus control register 1 Address: H'F078

Bit	Bit Name	Set Value	R/W	Description
7	ICE	1	R/W	I^2C bus interface 2 enable 0: The module is halted. (SCL and SDA pins are set to the port/serial function.) 1: The module is enabled for transfer operations. (SCL and SDA pins are bus drive state.)
6	RCVD	0	R/W	Reception disable This bit enables or disables the next operation when TRS is 0 and ICDRR is read. 0: Enables next reception 1: Disables next reception
5	MST	1	R/W	Master/slave selection
4	TRS	1	R/W	Transmit/receive selection The value of the TRS bit should be changed between transfer frames. The following operation modes can be selected by the MST and TRS bits in combination. 00: Slave receive mode 01: Slave transmit mode 10: Master receive mode 11: Master transmit mode
3	CKS3	0	R/W	Transfer clock select 3 to 0 These bits are valid only in the master mode and should be set according to the necessary transfer clock frequency. In this sample task the operating frequency ϕ is 10 MHz. For details on the transfer clock frequency see table 7.
2	CKS2	1	R/W	
1	CKS1	0	R/W	
0	CKS0	1	R/W	

Table 7 Transfer Clock Frequency

Bit 3	Bit 2	Bit 1	Bit 0		Transfer Clock Frequency
CKS3	CKS2	CKS1	CKS0	Clock	ϕ = 10 MHz
0	1	0	1	ϕ /100	100 kHz

- ICCR2 I^2C bus control register 2 Address: H'F079

Bit	Bit Name	Set Value	R/W	Description
5	SDAO	1	R/W	SDA output value control This bit is used with SDAOP (bit 4) for modifying the output level of SDA. This bit should not be manipulated when a transfer is in progress. • When 0 is read, SDA pin outputs a low level • When 0 is written, SDA pin changes to low level output • When 1 is read, SDA pin outputs a high level • When 1 is written, SDA pin changes to Hi-Z output (high output by external pull-up resistor)
4	SDAOP	0	R/W	SDAO write protection This bit controls changes in the output level of the SDA pin by changing the SDAO bit value. To change the output level, use the MOV instruction to clear SDAO and SDAOP to 0 or set SDAO to 1 and clear SDAOP to 0. This bit is always read as 1.

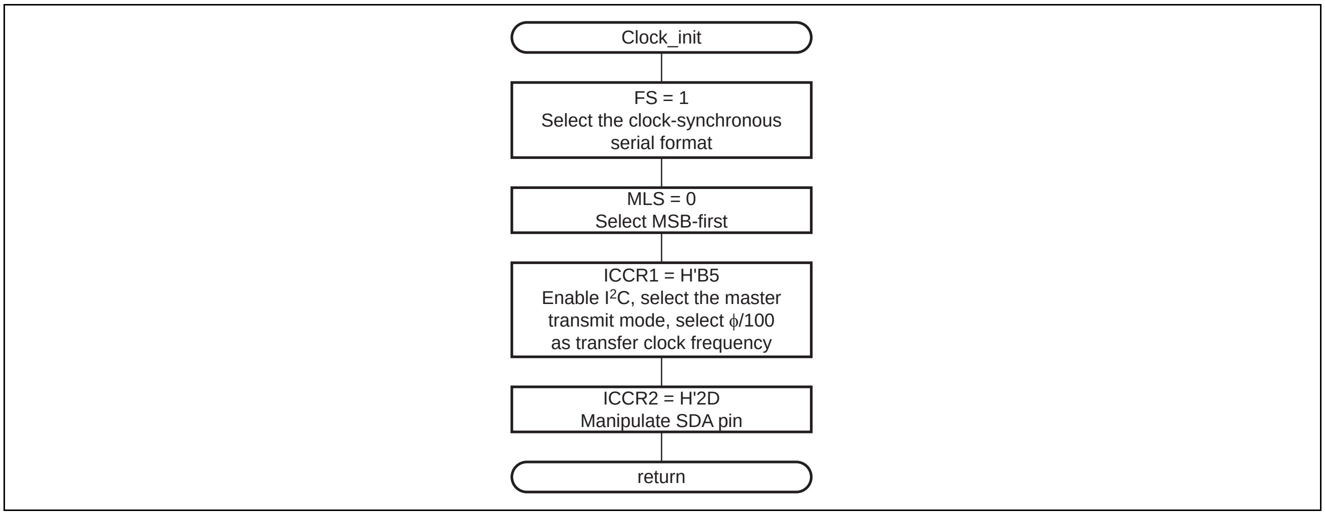
- ICMR I^2C bus mode register Address: H'F07A

Bit	Bit Name	Set Value	R/W	Description
7	MLS	0	R/W	MSB-first/LSB-first selection 0: MSB-first 1: LSB-first

- SAR Slave address register Address: H'F07D

Bit	Bit Name	Set Value	R/W	Description
0	FS	1	R/W	Format selection 0: I^2C bus format selected 1: Clock-synchronous serial format selected

3. Flowchart


Clock_init
FS = 1
Select the clock-synchronous serial format
MLS = 0
Select MSB-first
ICCR1 = H'B5
Enable I²C, select the master transmit mode, select φ/100 as transfer clock frequency
ICCR2 = H'2D
Manipulate SDA pin
return

5.4.3 master_trs() Function

1. Module Specifications

- Master transmit operation

Table 8 Module Specifications

Item	Type	Variable	Description
Arguments	None	None	None

2. Internal Registers Used

The internal registers used in this sample task are shown below. The set values shown are those used in the sample task and differ from the initial values.

- ICCR1 I^{2}C bus control register 1 Address: H'F078

Bit	Bit Name	Set Value	R/W	Description
5	MST	1	R/W	Master/slave selection
4	TRS	1	R/W	Transmit/receive selection The value of the TRS bit should be changed between transfer frames. The following operation modes can be selected by the MST and TRS bits in combination. 00: Slave receive mode 01: Slave transmit mode 10: Master receive mode 11: Master transmit mode

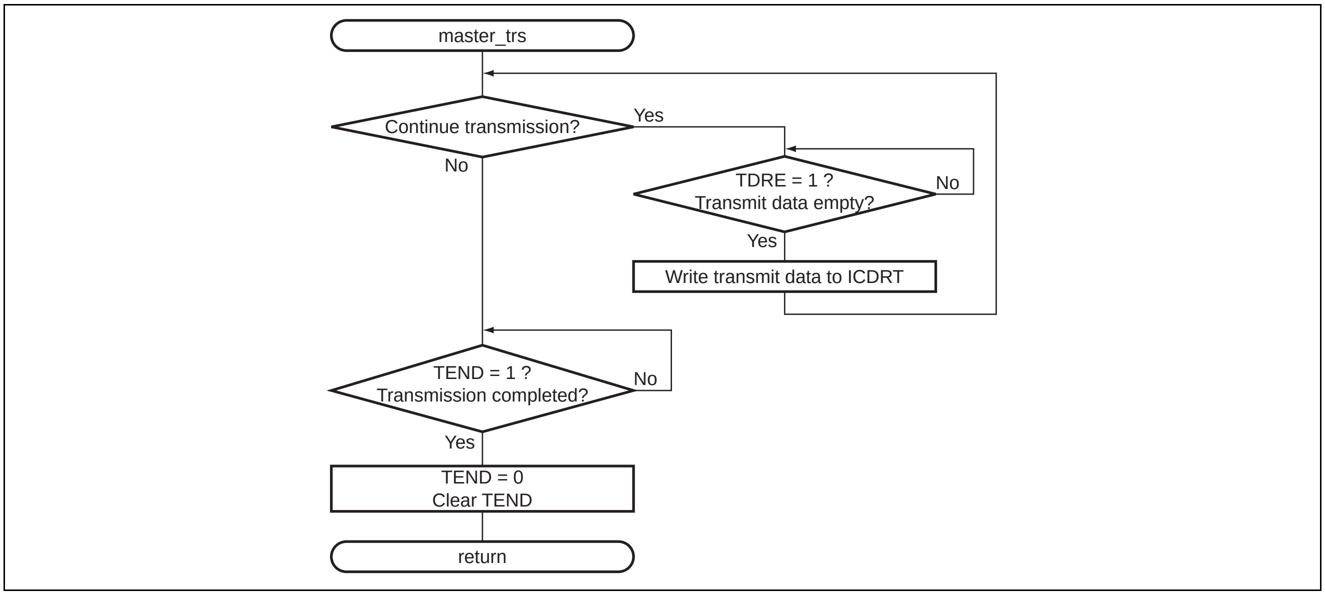
- ICSR I^{2}C bus status register Address: H'F07C

Bit	Bit Name	Set Value	R/W	Description
7	TDRE	Undefined	R/W	Transmit data register empty [Setting conditions] • When data is transferred from ICDRT to ICDRS and ICDRT becomes empty • When the TRS bit is set to 1 [Clearing conditions] • When 0 is written to TDRE after it was read as 1 • When data is written to ICDRT with an instruction
6	TEND	Undefined	R/W	Transmit end [Setting condition] • When the rising edge of the ninth clock cycle of SCL is detected while the value of TDRE is 1 [Clearing conditions] • When 0 is written in TEND after it was read as 1 • When data is written to ICDRT with an instruction

- ICDRT I^{2}C bus transmit data register Address: H'F07E

Bit	Bit Name	Set Value	R/W	Description
7	Bit 7	Undefined	R/W	I^{2}C bus transmit data register
6	Bit 6	Undefined	R/W	ICDRT is an 8-bit readable/writable register that stores transmit data. When ICDRT detects space in the I^{2}C bus shift register (ICDRS) it transfers the transmit data which has been written to ICDRT to ICDRS and starts transferring data. Continuous transfer is possible if the next transmit data is written to ICDRT while data transfer to ICDRS is in progress. The initial value of ICDRT is H'FF.
5	Bit 5	Undefined	R/W	
4	Bit 4	Undefined	R/W	
3	Bit 3	Undefined	R/W	
2	Bit 2	Undefined	R/W	
1	Bit 1	Undefined	R/W	
0	Bit 0	Undefined	R/W	

3. Flowchart



5.4.4 master_rcv() Function

1. Module Specifications

- Master receive operation

Table 9 Module Specifications

Item	Type	Variable	Description
Arguments	None	None	None
Return value	unsigned char	-	0: No error 1: Error

2. Internal Registers Used

The internal registers used in this sample task are shown below. The set values shown are those used in the sample task and differ from the initial values.

- ICCR1 I²C bus control register 1 Address: H'F078

Bit	Bit Name	Set Value	R/W	Description
6	RCVD	0	R/W	Reception disabled This bit enables or disables the next operation when TRS is 0 and ICDRR is read. 0: Enables next reception 1: Disables next reception
5	MST	1	R/W	Master/slave selection
4	TRS	0	R/W	Transmit/receive selection In the master mode with the I²C bus format, MST and TRS are both reset by hardware when arbitration is lost, causing a transition to the slave receive mode. The value of the TRS bit should be changed between transfer frames. The following operation modes can be selected by the MST and TRS bits in combination. 00: Slave receive mode 01: Slave transmit mode 10: Master receive mode 11: Master transmit mode

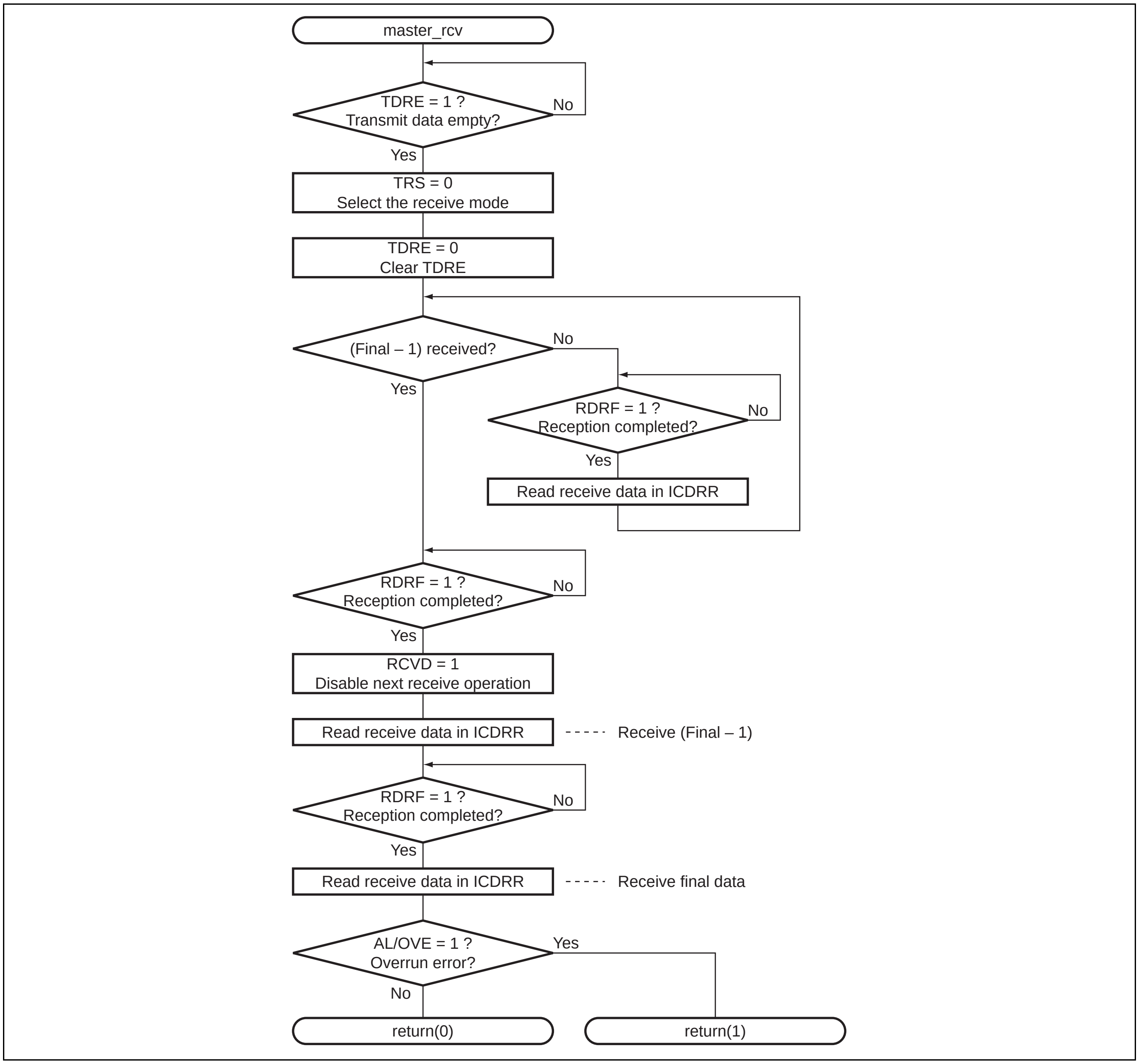
- ICSR I^{2}C bus status register Address: H'F07C

Bit	Bit Name	Set Value	R/W	Description
7	TDRE	Undefined	R/W	Transmit data register empty [Setting conditions] • When data is transferred from ICDRT to ICDRS and ICDRT becomes empty • When the TRS bit is set to 1 • When a start condition (including re-transfer) has been issued [Clearing conditions] • When 0 is written to TDRE after it was read as 1 • When data is written to ICDRT with an instruction
5	RDRF	Undefined	R/W	Receive data register full [Setting condition] • When receive data is transferred from ICDRS to ICDRR [Clearing conditions] • When 0 is written to RDRF after it was read as 1 • When ICDRR is read with an instruction
2	AL/OVE	Undefined	R/W	Arbitration lost flag/overrun error flag In the clock-synchronous serial format this flag indicates that the final bit has been received while RDRF remains 1. [Setting condition] • When the final bit is received while RDRF remains 1 [Clearing condition] • When 0 is written to AL/OVE after it was read as 1

- ICDRR I^{2}C bus receive data register Address: H'F07F

Bit	Bit Name	Set Value	R/W	Description
7	Bit 7	Undefined	R	I^{2}C bus receive data register ICDRR is an 8-bit register that stores receive data. After one byte of data is received, ICDRR transfers the receive data from ICDRS to ICDRR and the next data can be received. ICDRR is a receive-only register, so the CPU cannot write to it. The initial value of ICDRR is H'FF.
6	Bit 6	Undefined	R	
5	Bit 5	Undefined	R	
4	Bit 4	Undefined	R	
3	Bit 3	Undefined	R	
2	Bit 2	Undefined	R	
1	Bit 1	Undefined	R	
0	Bit 0	Undefined	R	

3. Flowchart



5.5 Link Address Specifications

Section Name	Address
CVECT	H'0000
P	H'0100
D, B	H'F780

6. Description of Software (Slave)

In this sample task I^{2}C bus interface module initialization, slave receive, and slave transmit operations are performed. The functions used by the slave program are described below.

6.1 Functions

Table 10 List of Slave Program Functions

Function Name	Description
main	Controls slave communication
IIC2_init	Initializes the I^{2}C clock-synchronous serial format
slave_rcv	Slave receive operation
slave_trs	Slave transmit operation

6.2 Constants

Table 11 shows the constants used in this sample task.

Table 11 Constants

Label Name	Constant Value	Description	Used in
SIZE	4	Transmit/receive data size	slave_trs slave_rcv

6.3 RAM Usage

Table 12 shows the RAM used in this sample task.

Table 12 RAM Usage

Label Name	Description	Memory Consumption	Used in
s_data[SIZE]	Buffer for storing transmit/receive data	4 bytes	slave_trs slave_rcv

6.4 Modules

6.4.1 main() Function

1. Module Specifications

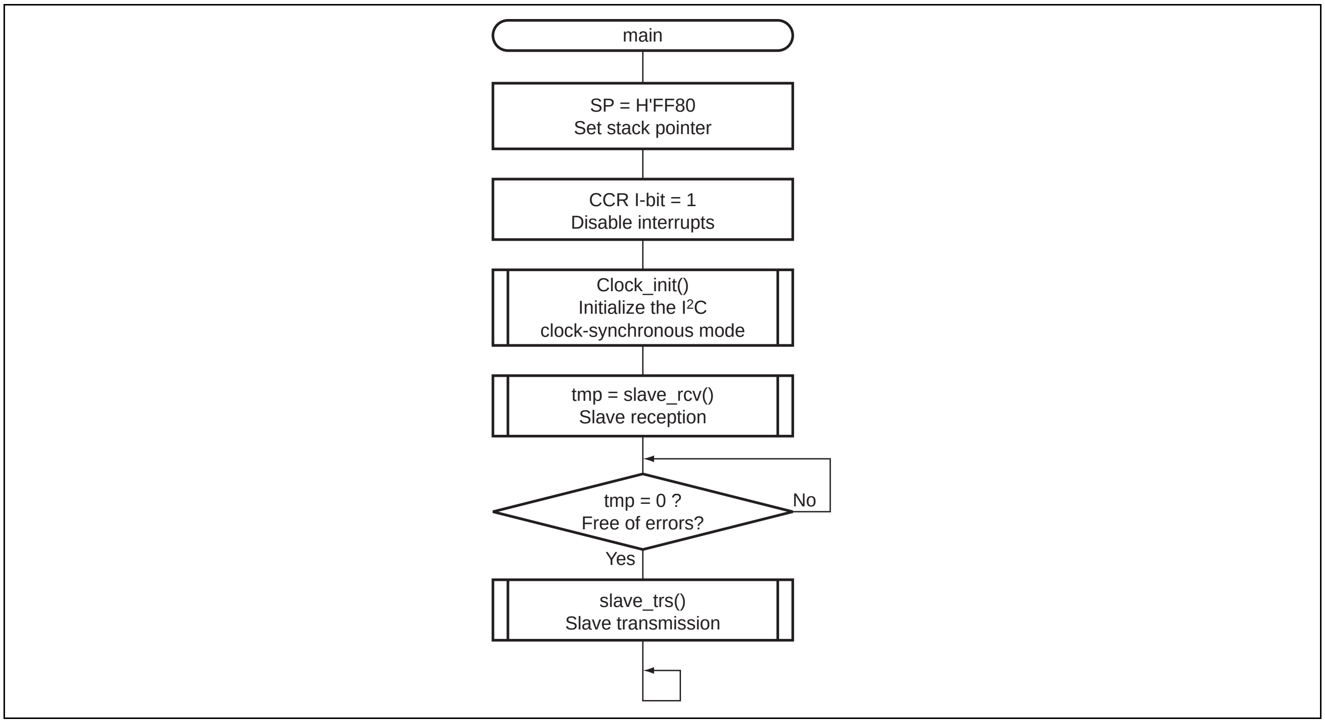
- Controls slave communication

Table 13 Module Specifications

Item	Type	Variable	Description
Arguments	None	None	None

2. Internal Registers Used
   None

3. Flowchart



6.4.2 Clock_init() Function

1. Module Specifications

- Initializes the I^{2}C clock-synchronous serial format

Table 14 Module Specifications

Item	Type	Variable	Description
Arguments	None	None	None

2. Internal Registers Used

The internal registers used in this sample task are shown below. The set values shown are those used in the sample task and differ from the initial values.

- ICCR1 I^{2}C bus control register 1 Address: H'F078

Bit	Bit Name	Set Value	R/W	Description
7	ICE	1	R/W	I^{2}C bus interface 2 enabled 0: The module is halted. (SCL and SDA pins are set to the port/serial function.) 1: The module is enabled for transfer operations. (SCL and SDA pins are bus drive state.)
6	RCVD	0	R/W	Reception disabled This bit enables or disables the next operation when TRS is 0 and ICDRR is read. 0: Enables next reception 1: Disables next reception
5	MST	0	R/W	Master/slave selection
4	TRS	0	R/W	Transmit/receive selection In the master mode with the I^{2}C bus format, MST and TRS are both reset by hardware when arbitration is lost, causing a transition to the slave receive mode. The value of the TRS bit should be changed between transfer frames. The following operation modes can be selected by the MST and TRS bits in combination. 00: Slave receive mode 01: Slave transmit mode 10: Master receive mode 11: Master transmit mode

- ICCR2 I^{2}C bus control register 2 Address: H'F079

Bit	Bit Name	Set Value	R/W	Description
5	SDAO	1	R/W	SDA output value control This bit is used with SDAOP (bit 4) when changing the output level of SDA. This bit should not be manipulated when a transfer is in progress. • When 0 is read, SDA pin outputs a low level • When 0 is written, SDA pin changes to low level output • When 1 is read, SDA pin outputs a high level • When 1 is written, SDA pin changes to Hi-Z output (high output by external pull-up resistor)
4	SDAOP	0	R/W	SDAO write protection This bit controls changes in the output level of the SDA pin by modifying the SDAO bit. To change the output level, use the MOV instruction to clear SDAO and SDAOP to 0 or set SDAO to 1 and clear SDAOP to 0. This bit is always read as 1.

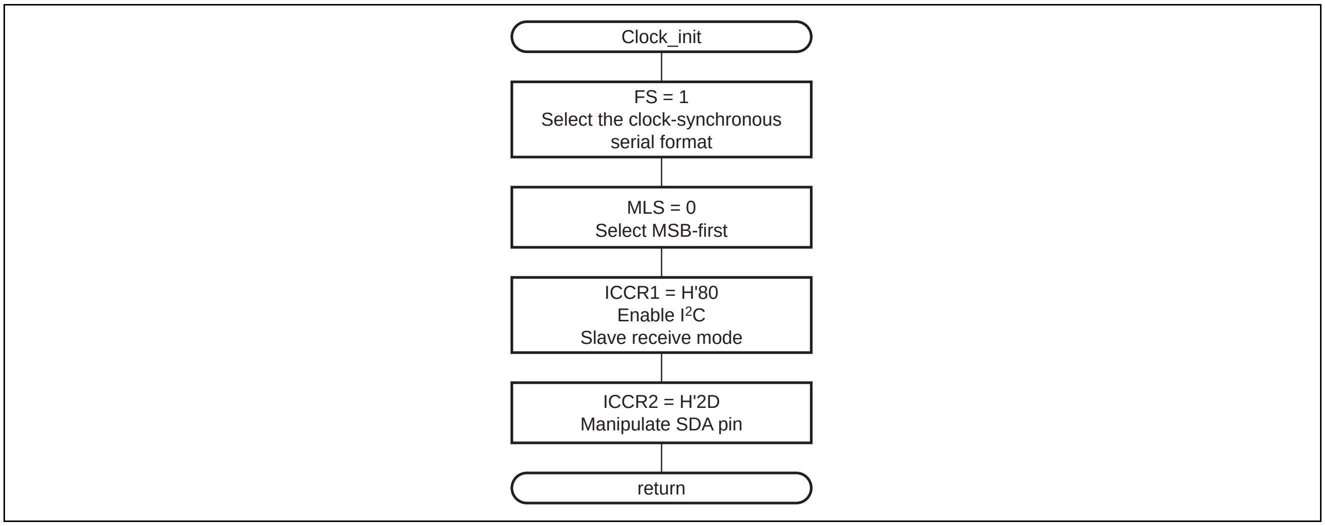
- ICMR I^{2}C bus mode register Address: H'F07A

Bit	Bit Name	Set Value	R/W	Description
7	MLS	0	R/W	MSB-first/LSB-first select 0: MSB-first 1: LSB-first

- SAR Slave address register Address: H'F07D

Bit	Bit Name	Set Value	R/W	Description
0	FS	1	R/W	Format selection 0: I^{2}C bus format selected 1: Clock-synchronous serial format selected

3. Flowchart



6.4.3 slave_rcv() Function

1. Module Specifications

- Slave receive operation

Table 15 Module Specifications

Item	Type	Variable	Description
Arguments	None	None	None

2. Internal Registers Used

   The internal registers used in this sample task are shown below. The set values shown are those used in the sample task and differ from the initial values.

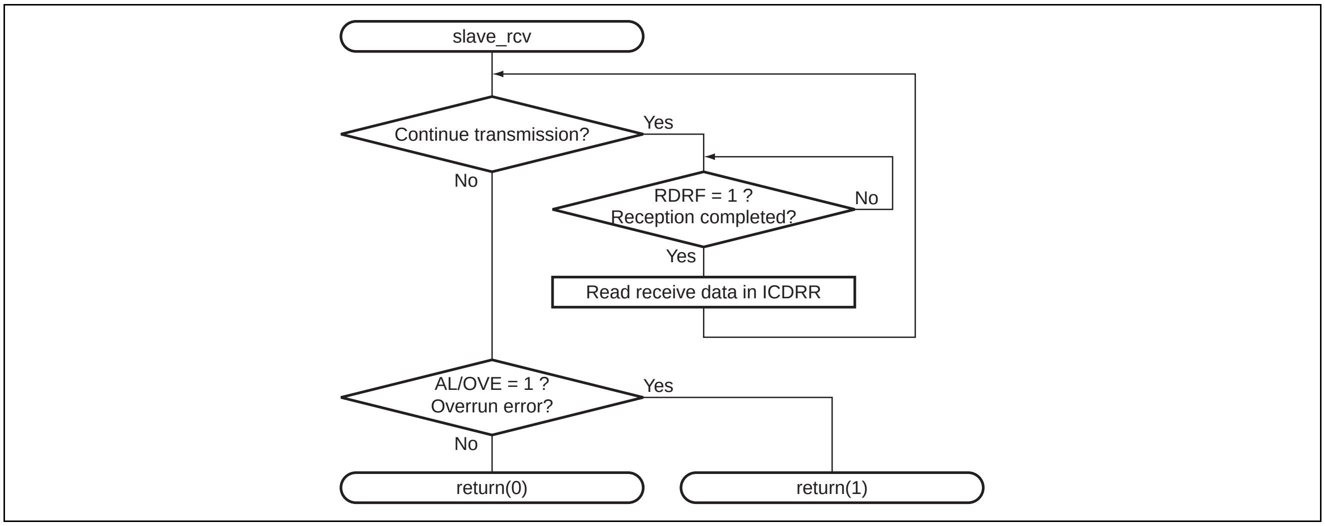
- ICSR I^{2}C bus status register Address: H'F07C

Bit	Bit Name	Set Value	R/W	Description
5	RDRF	Undefined	R/W	Receive data register full [Setting condition] • When receive data is transferred from ICDRS to ICDRR [Clearing conditions] • When 0 is written to RDRF after it was read as 1 • When ICDRR is read with an instruction
2	AL/OVE	Undefined	R/W	Arbitration lost flag/overrun error flag In the clock-synchronous serial format this flag indicates that the final bit has been received while RDRF remains 1. [Setting condition] • When the final bit is received while RDRF remains 1 [Clearing condition] • When 0 is written to AL/OVE after it was read as 1

- ICDRR I^{2}C bus receive data register Address: H'F07F

Bit	Bit Name	Set Value	R/W	Description
7	Bit 7	Undefined	R	I^{2}C bus receive data register ICDRR is an 8-bit register that stores receive data. After one byte of data is received, ICDRR transfers the receive data from ICDRS to ICDRR and the next data can be received. ICDRR is a receive-only register, so the CPU cannot write to it. The initial value of ICDRR is H'FF.
6	Bit 6	Undefined	R	
5	Bit 5	Undefined	R	
4	Bit 4	Undefined	R	
3	Bit 3	Undefined	R	
2	Bit 2	Undefined	R	
1	Bit 1	Undefined	R	
0	Bit 0	Undefined	R	

3. Flowchart


slave_rcv
Continue transmission?
Yes
No
RDRF = 1 ?
Reception completed?
No
Yes
Read receive data in ICDRR
AL/OVE = 1 ?
Overrun error?
Yes
No
return(0)
return(1)

6.4.4 slave_trs() Function

1. Module Specifications

- Slave transmit operation

Table 16 Module Specifications

Item	Type	Variable	Description
Arguments	None	None	None

2. Internal Registers Used
   The internal registers used in this sample task are shown below. The set values shown are those used in the sample task and differ from the initial values.

- ICCR1 I²C bus control register 1 Address: H'F078

Bit	Bit Name	Set Value	R/W	Description
5	MST	0	R/W	Master/slave selection
4	TRS	1	R/W	Transmit/receive selection The value of the TRS bit should be changed between transfer frames. The following operation modes can be selected by the MST and TRS bits in combination. 00: Slave receive mode 01: Slave transmit mode 10: Master receive mode 11: Master transmit mode

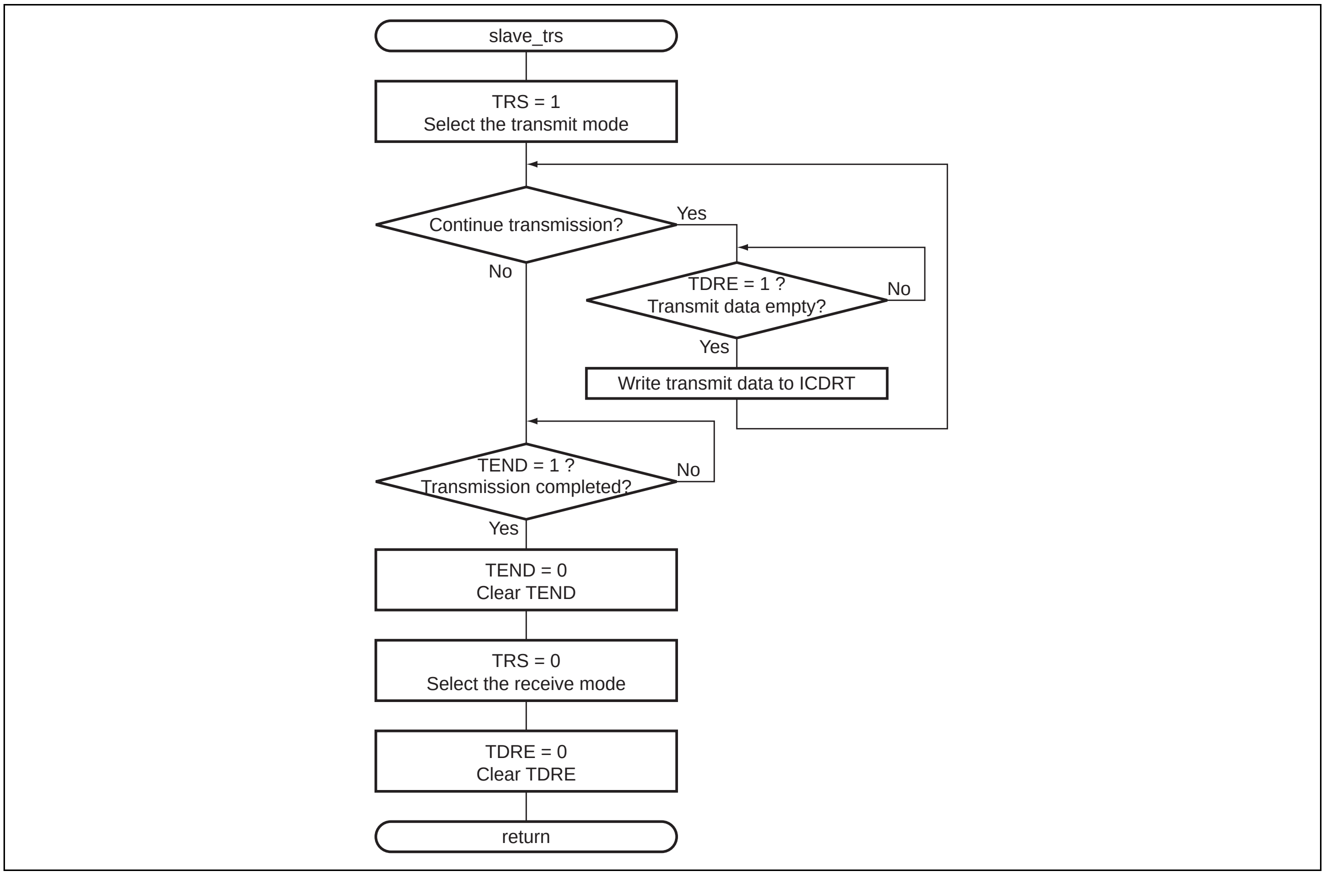
- ICSR I²C bus status register Address: H'F07C

Bit	Bit Name	Set Value	R/W	Description
7	TDRE	Undefined	R/W	Transmit data register empty [Setting conditions] • When data is transferred from ICDRT to ICDRS and ICDRT becomes empty • When the TRS bit is set to 1 [Clearing conditions] • When 0 is written to TDRE after it was read as 1 • When data is written to ICDRT with an instruction
6	TEND	Undefined	R/W	Transmit end [Setting condition] • When the rising edge of the ninth clock cycle of SCL is detected while the value of TDRE is 1 [Clearing conditions] • When 0 is written in TEND after it was read as 1 • When data is written to ICDRT with an instruction

- ICDRT I^{2}C bus transmit data register Address: H'F07E

Bit	Bit Name	Set Value	R/W	Description
7	Bit 7	Undefined	R/W	I^{2}C bus transmit data register ICDRT is an 8-bit readable/writable register that stores transmit data. When ICDRT detects space in the I^{2}C bus shift register (ICDRS) it transfers the transmit data which was written to ICDRT to ICDRS and starts transferring data. Continuous transfer is possible if the next transmit data is written to ICDRT while data transfer to ICDRS is in progress. The initial value of ICDRT is H'FF.
6	Bit 6	Undefined	R/W	
5	Bit 5	Undefined	R/W	
4	Bit 4	Undefined	R/W	
3	Bit 3	Undefined	R/W	
2	Bit 2	Undefined	R/W	
1	Bit 1	Undefined	R/W	
0	Bit 0	Undefined	R/W	

3. Flowchart



6.5 Link Address Specifications

Section Name	Address
CVECT	H'0000
P	H'0100
B	H'F780

Revision Record

Rev.	Date	Description Page	Summary
1.00	Mar.18.05	—	First edition issued

Keep safety first in your circuit designs!

1. Renesas Technology Corp. puts the maximum effort into making semiconductor products better and more reliable, but there is always the possibility that trouble may occur with them. Trouble with semiconductors may lead to personal injury, fire or property damage.
   Remember to give due consideration to safety when making your circuit designs, with appropriate measures such as (i) placement of substitutive, auxiliary circuits, (ii) use of nonflammable material or (iii) prevention against any malfunction or mishap.

Notes regarding these materials

1. These materials are intended as a reference to assist our customers in the selection of the Renesas Technology Corp. product best suited to the customer's application; they do not convey any license under any intellectual property rights, or any other rights, belonging to Renesas Technology Corp. or a third party.
2. Renesas Technology Corp. assumes no responsibility for any damage, or infringement of any third-party's rights, originating in the use of any product data, diagrams, charts, programs, algorithms, or circuit application examples contained in these materials.
3. All information contained in these materials, including product data, diagrams, charts, programs and algorithms represents information on products at the time of publication of these materials, and are subject to change by Renesas Technology Corp. without notice due to product improvements or other reasons. It is therefore recommended that customers contact Renesas Technology Corp. or an authorized Renesas Technology Corp. product distributor for the latest product information before purchasing a product listed herein.
   The information described here may contain technical inaccuracies or typographical errors. Renesas Technology Corp. assumes no responsibility for any damage, liability, or other loss rising from these inaccuracies or errors.
   Please also pay attention to information published by Renesas Technology Corp. by various means, including the Renesas Technology Corp. Semiconductor home page (http://www.renesas.com).
4. When using any or all of the information contained in these materials, including product data, diagrams, charts, programs, and algorithms, please be sure to evaluate all information as a total system before making a final decision on the applicability of the information and products. Renesas Technology Corp. assumes no responsibility for any damage, liability or other loss resulting from the information contained herein.
5. Renesas Technology Corp. semiconductors are not designed or manufactured for use in a device or system that is used under circumstances in which human life is potentially at stake. Please contact Renesas Technology Corp. or an authorized Renesas Technology Corp. product distributor when considering the use of a product contained herein for any specific purposes, such as apparatus or systems for transportation, vehicular, medical, aerospace, nuclear, or undersea repeater use.
6. The prior written approval of Renesas Technology Corp. is necessary to reprint or reproduce in whole or in part these materials.
7. If these products or technologies are subject to the Japanese export control restrictions, they must be exported under a license from the Japanese government and cannot be imported into a country other than the approved destination.
   Any diversion or reexport contrary to the export control laws and regulations of Japan and/or the country of destination is prohibited.
8. Please contact Renesas Technology Corp. for further details on these materials or the products contained therein.