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H8/38076R

Asynchronous Serial Data Reception

Introduction

Serial data is received using the asynchronous mode of the serial communication interface 3 (SCI3).

Target Device

H8/38076R

Contents

1. Specifications

- Asynchronous serial data transfer is employed to receive 4 bytes of 8-bit data using channel 1.
- The format of the receive data is set to 8-bit data length, odd parity, and 1 stop bit.
- The bit rate is 31,250 bps. The task finishes after 4 bytes of data have been received.
- Figure 1 shows a connection diagram for serial data reception in the asynchronous mode.
- Figure 2 shows the data format for serial data reception in the asynchronous mode.

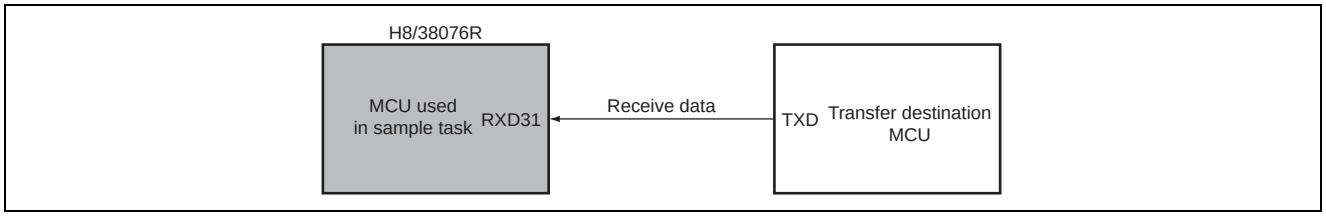


Figure 1 Serial Data Reception in the Asynchronous Mode

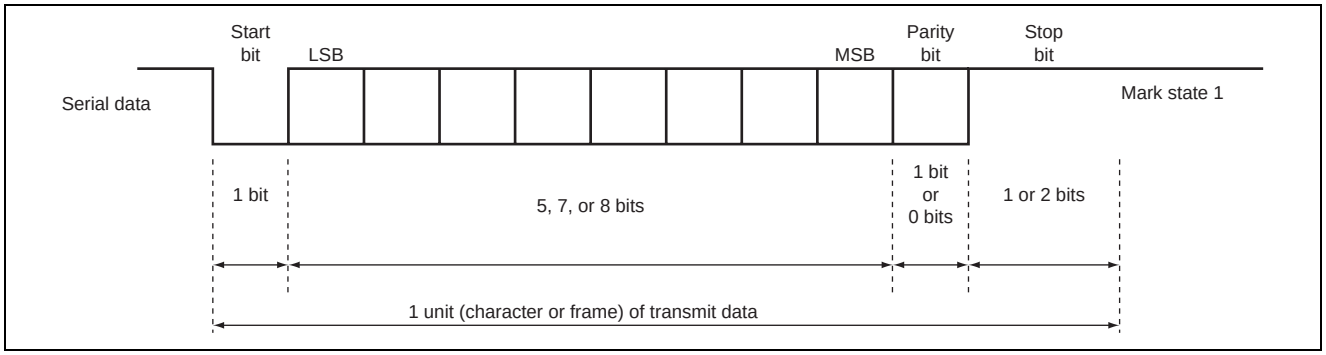


Figure 2 Data Format for Serial Data Transmission in the Asynchronous Mode

2. Description of Functions

2.1 Functions Used

In this sample task serial data is transmitted using the asynchronous mode of the serial communication interface 3 (SCI3). A block diagram of the serial communication interface 3 is shown in figure 3, and the functions used in this sample task are described below.

1. System Clock (ϕ)
   This 10-MHz oscillation clock is the reference clock for operation of the CPU and peripheral functions.

2. SCI3 Asynchronous Mode
   Each character of transfer data consists of a start bit (low level), followed by transmit/receive data (in LSB-first order), a parity bit, and finally a stop bit (high level). In the asynchronous mode, synchronization is performed on the falling edge of the start bit during reception. The data is sampled on the 8th pulse of a clock with a frequency 16 times the bit period, so the transfer data is fetched at the center of each bit. The transmitter and receiver are independent units inside the SCI3, enabling full duplex operation. Both the transmitter and the receiver also have a double-buffered structure, so the next data can be written while transmission is in progress and the preceding data can be read while reception is in progress, enabling continuous data transfer.

- Receive shift register 3 (RSR3)
  RSR3 is a shift register that receives serial data input from the RXD31 or RXD32 pin and converts it into parallel data. When one frame of data has been received, it is transferred automatically to RDR3. RSR3 cannot be directly accessed by the CPU.

- Receive data register 3 (RDR3)
  RDR3 is an 8-bit register that stores receive data. When one frame of data has been received, it is transferred from RSR3 to RDR3, enabling RSR3 to receive the next frame of data. RSR3 and RDR3 have a double-buffered structure, so continuous reception is possible. Read RDR3 only once, after confirming that the RDRF bit in SSR3 is set to 1. RDR3 cannot be written by the CPU. The initial value of RDR3 is H'00.
  RDR3 is initialized to H'00 at a reset, in the standby mode, watch mode, or module standby mode.

- Serial mode register 3 (SMR3)
  SMR3 is a register for selecting the serial communication format and the clock source for the internal baud rate generator. In this sample task the asynchronous mode is selected and n = 0 is selected as the clock source.

- Serial control register 3 (SCR3)
  SCR3 is a register that controls transmission, reception, and interrupts, and selects the clock source.

- Serial status register 3 (SSR3)
  SSR3 consists of status flags and multiprocessor bits for transmission and reception. In this sample task the RDRF bit is polled and the receive data is read in after the preceding frame has been transferred from RSR3 to RDR3.

- Serial port control register (SPCR)
  SPCR switches the functions of the TXD32 and TXD31 pins and controls data inversion of the transmit and receive pins. In this sample task the TXD31 pin is selected and data is input unmodified (without inversion).

- Bit rate register 3 (BRR3)
  BRR3 sets the bit rate. In this sample task it is set to N = 9 (10 MHz, n = 0) to obtain a bit rate of 250 Kbps. The equation used to calculate the setting is shown below.

$$N \text{ (set value of BRR3)} = \frac{\phi}{32 \times 2^{2n} \times \text{bit rate}} - 1$$

$$= \frac{10 \text{ MHz}}{32 \times 2^{2 \times 0} \times 31250} - 1$$

$$= 9$$

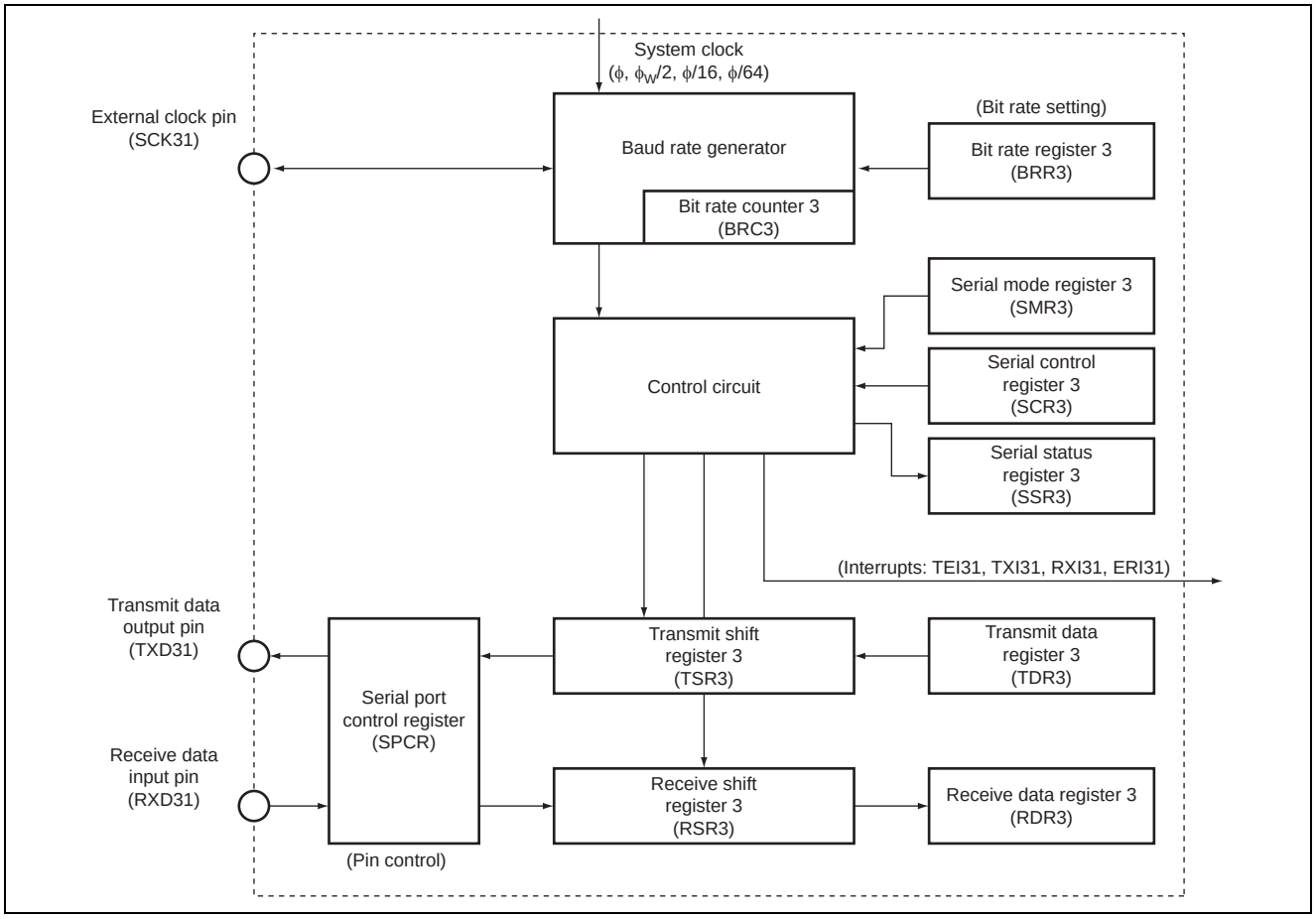


Figure 3 Block Diagram of SCI3

2.2 Assignment of Functions

Table 1 shows the assignment of functions in this sample task. Serial data reception in the asynchronous mode is performed using functions assigned as shown in table 1.

Table 1 Assignment of Functions

Elements	Description
RDR3	8-bit register for storing receive data
SMR3	Sets the asynchronous mode and selects ϕ as clock source for baud rate generator
SCR3	Enables reception, sets internal clock as clock source
SSR3	Status flag showing the operating status of the SCI3
BRR3	Sets the bit rate (31,250 bps)
SPCR	Specifies the data is input to the RXD31 pin unmodified (without inversion)
RXD31	Receive data input pin of SCI3

3. Principles of Operation

The principles of operation for this sample task are illustrated in figure 4. Serial data reception in the asynchronous mode is implemented using the software and hardware processing shown below.

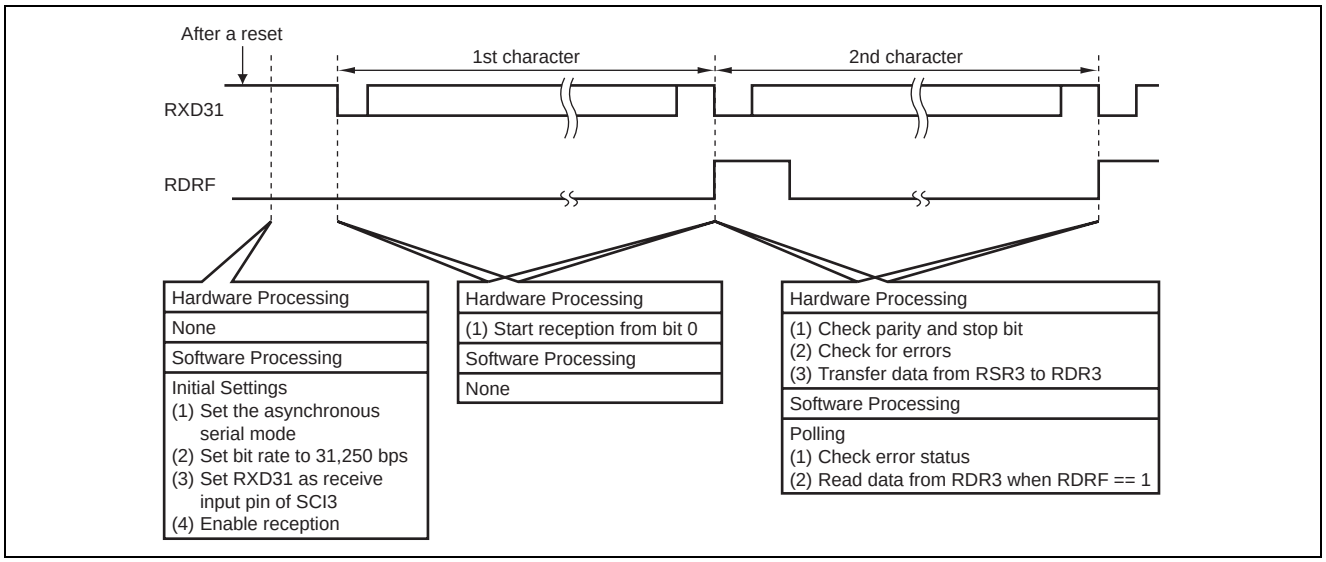


Figure 4 Principles of Operation for Serial Data Reception in the Asynchronous Mode

4. Description of Software

In this sample task serial data is received in the asynchronous mode. The functions used are listed below.

4.1 Functions

Table 2 List of Functions

Function Name	Description
main	Controls serial data reception in the asynchronous mode, sets receive buffer
init_sci3	Initializes SCI3
recv_sci3	Receives serial data in the asynchronous mode
stop_sci3	Ends the asynchronous mode

4.2 Constants

The constants used in this sample task are listed in table 3.

Table 3 Constants

Label Name	Constant Value	Description	Used in
DATA_NUM	4	Receive data size	main

4.3 RAM Usage

No RAM is used in this sample task.

4.4 Modules

4.4.1 main() Function

1. Module Specifications

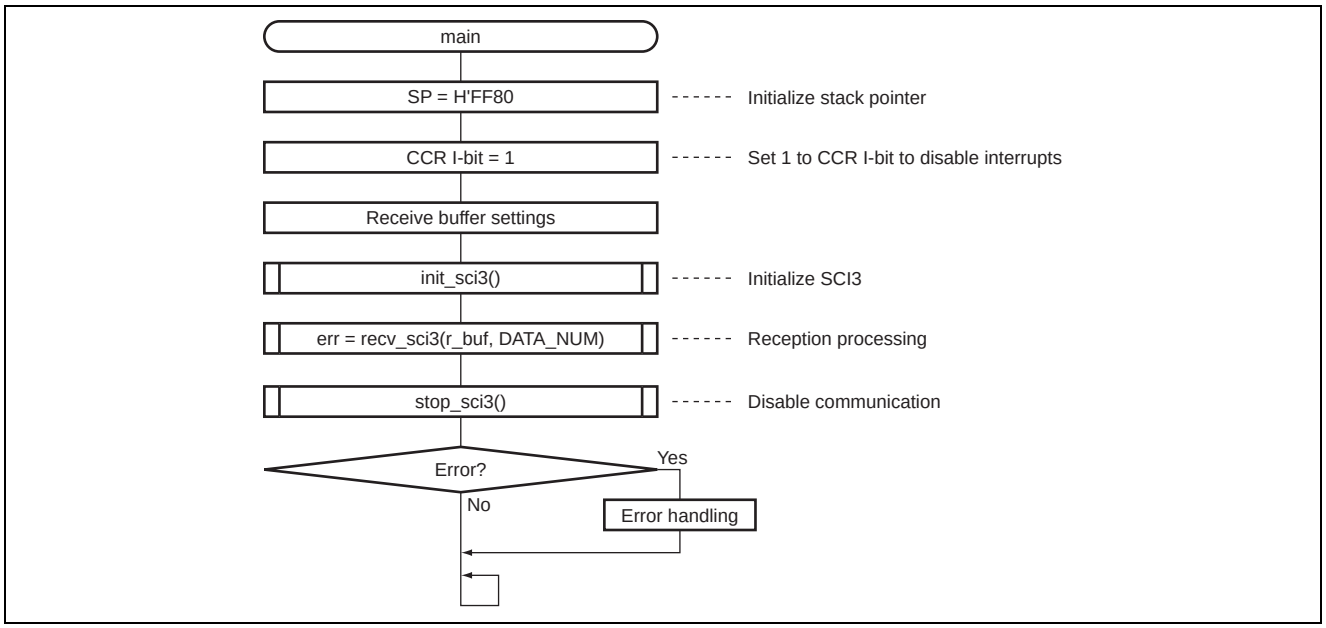
- Controls serial data reception in the asynchronous mode, sets receive buffer

Table 4 Module Specifications

Item	Type	Variable	Description
Arguments	None	None	None

2. Internal Registers Used
   None

3. Flowchart



4.4.2 init_sci3 Function

1. Module Specifications

- Initializes the asynchronous mode

Table 5 Module Specifications

Item	Type	Variable	Description
Arguments	None	None	None

2. Internal Registers Used

The internal registers used in this sample task are shown below. The set values shown are those used in the sample task and differ from the initial values.

- SPCR Serial Port Control Register Address: H'FF91

Bit	Bit Name	Set Value	R/W	Description
0	SCINV0	0	R/W	RXD31 Pin Input Data Inversion Switch Specifies whether data input to the RXD31 pin is inverted or not. 0: RXD31 input data not inverted 1: RXD31 input data inverted

- SMR3 Serial Mode Register 3 Address: H'FF98

Bit	Bit Name	Set Value	R/W	Description
7	COM	0	R/W	Communication Mode 0: Asynchronous mode 1: Clock-synchronous mode
6	CHR	0	R/W	Character Length (enabled only in the asynchronous mode) 0: Data length of 8 or 5 bits used for transmission and reception 1: Data length of 7 or 5 bits used for transmission and reception When 7-bit data is selected, the MSB (bit 7) in TDR3 is not transmitted. To select 5 bits as the data length, set both the PE and MP bits to 1. In this case the three most significant bits (bits 7, 6, and 5) in TDR3 are not transmitted.
5	PE	1	R/W	Parity Enable (enabled only in the asynchronous mode) When this bit is set to 1, a parity bit is added to transmit data before transmission, and the parity bit is checked in reception.
4	PM	1	R/W	Parity Mode (enabled only when the PE bit is 1 in the asynchronous mode) 0: Even parity used for transmission 1: Odd parity used for transmission When even parity is selected, a parity bit is added in transmission so that the total number of 1 bits in the transmit data plus the parity bit is an even number. During reception the data is checked to confirm that the number of 1 bits in the receive data plus the parity bit is an even number. When odd parity is selected, a parity bit is added in transmission so that the total number of 1 bits in the transmit data plus the parity bit is an odd number. During reception the data is checked to confirm that the number of 1 bits in the receive data plus the parity bit is an odd number. Note that in the clock-synchronous mode, and in the asynchronous mode if parity bit addition and checking is disabled, the PM bit setting is invalid.
3	STOP	0	R/W	Stop Bit Length (enabled only in the asynchronous mode) Selects the stop bit length in transmission. 0: 1 stop bit 1: 2 stop bits Only the first stop bit is checked during reception, regardless of the value of STOP. If the second stop bit is 0, it is treated as the start bit of the next transmit character.
2	MP	0	R/W	Multiprocessor Mode The multiprocessor communication function is enabled when this bit is set to 1. The PE and PM bit settings become invalid.
1	CKS1	0	R/W	Clock Select 0 and 1
0	CKS0	0	R/W	These bits select the clock source for the internal baud rate generator. 00: ϕ clock (n = 0) A set value of 0 is used for active (medium-speed/high-speed) mode.

- BRR3 Bit Rate Register 3 Address: H'FF99

Bit	Bit Name	Set Value	R/W	Description
7	bit7	0	R/W	BRR3 is an 8-bit readable/writable register that selects the bit rate. The initial value is H'FF. The bit rate is determined by the n setting of bits CKS1 and CKS0 in SMR3 in the asynchronous mode and combination with the N setting of BRR3. See the hardware manual for details. In this sample task BRR3 is set to 9 to obtain a bit rate of 31,250 bps.
6	bit6	0	R/W	
5	bit5	0	R/W	
4	bit4	0	R/W	
3	bit3	1	R/W	
2	bit2	0	R/W	
1	bit1	0	R/W	
0	bit0	1	R/W	

- SCR3 Serial Control Register 3 Address: H'FF9A

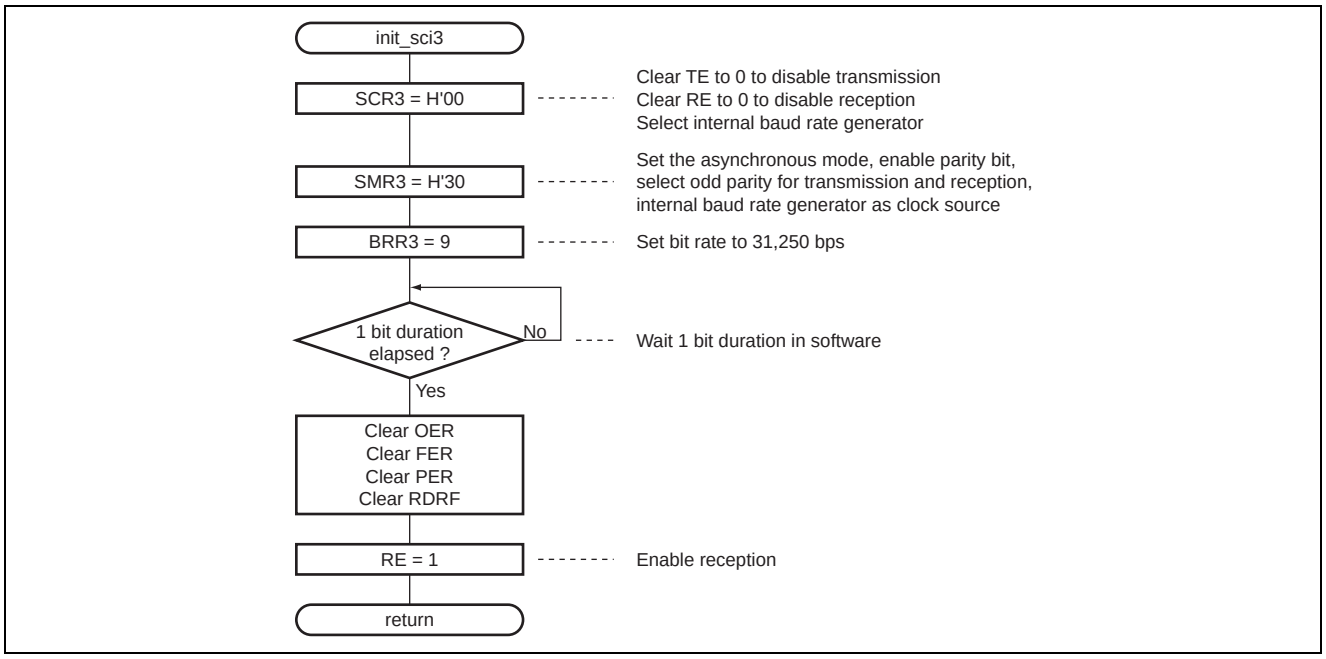
Bit	Bit Name	Set Value	R/W	Description
5	TE	0	R/W	Transmit Enable Transmission is enabled when this bit is set to 1. When TE is 0, the TDRE bit in SSR3 is fixed at 1. When transmit data is written to TDR3 while TE is 1, the TDRE bit in SSR3 is cleared to 0 and serial data transmission starts. Be sure to make SMR3 settings and set the SPC31 or SPC32 bit in SPCR to determine the transmission format before setting the TE bit to 1.
4	RE	1	R/W	Receive Enable Reception is enabled when this bit is set to 1. In this state serial data reception is started when serial clock input is detected in the asynchronous mode. Be sure to carry out SMR3 settings to decide the reception format before setting the RE bit to 1. Note that the RDRF, FER, PER, and OER flags in SSR3 are not affected when the RE bit is cleared to 0, and retain their previous state.
1	CKE1	0	R/W	Clock Enable 0 and 1
0	CKE0	0	R/W	Selects the clock source. Asynchronous mode 00: Internal baud rate generator (SCK31 or SCK32 pin functions as an I/O port)

- SSR3 Serial Status Register 3 Address: H'FF9C

Bit	Bit Name	Set Value	R/W	Description
6	RDRF	0	R/(W)*	Receive Data Register Full Indicates whether or not receive data is stored in RDR3. [Setting condition] • When reception ends normally and receive data is transferred from RSR3 to RDR3 [Clearing conditions] • When 0 is written to RDRF after it was read as 1 • When data is read from RDR3
5	OER	0	R/(W)*	Overrun Error [Setting condition] • When an overrun error occurs during reception [Clearing condition] • When 0 is written to OER after it was read as 1 When the RE bit in SCR3 is cleared to 0, the OER bit is not affected and retains its previous state. When an overrun error occurs, RDR3 retains the receive data it held before the overrun error occurred, and data received after the error is lost. Reception cannot be continued with the OER bit set to 1.
4	FER	0	R/(W)*	Framing Error [Setting condition] • When a framing error occurs during reception [Clearing condition] • When 0 is written to FER after it was read as 1 When the RE bit in SCR3 is cleared to 0, the FER bit is not affected and retains its previous state. Note that, in 2-stop-bit mode, only the first stop bit is checked for a value of 1; the second stop bit is not checked. If a framing error occurs, the receive data is transferred to RDR3 but the RDRF bit is not set. Reception cannot be continued with the FER bit set to 1.
3	PER	0	R/(W)*	Parity Error [Setting condition] • When a parity error is generated during reception [Clearing condition] • When 0 is written to PER after it was read as 1 When the RE bit in SCR3 is cleared to 0, the PER bit is not affected and retains its previous state. Receive data in which a parity error has occurred is still transferred to RDR3, but the RDRF bit is not set. Reception cannot be continued with the PER bit set to 1.

Note: * Only 0 can be written to clear the flag.

3. Flowchart


init_sci3
SCR3 = H'00
Clear TE to 0 to disable transmission
Clear RE to 0 to disable reception
Select internal baud rate generator
SMR3 = H'30
Set the asynchronous mode, enable parity bit,
select odd parity for transmission and reception,
internal baud rate generator as clock source
BRR3 = 9
Set bit rate to 31,250 bps
1 bit duration
elapsed ?
No
Wait 1 bit duration in software
Yes
Clear OER
Clear FER
Clear PER
Clear RDRF
RE = 1
Enable reception
return

4.4.3 rcv_sci3() Function

1. Module Specifications

- Receives serial data in the asynchronous mode

Table 6 Module Specifications

Item	Type	Variable	Description
Arguments	unsigned char *	r_ptr	Pointer to buffer for storing receive data
	unsigned char	num	Number of bytes of receive data
Return value	unsigned char	err	Indicates whether or not an error has occurred

2. Internal Registers Used

The internal registers used in this sample task are shown below. The set values shown are those used in the sample task and differ from the initial values.

- RDR3 Receive Data Register 3 Address: H'FF9D

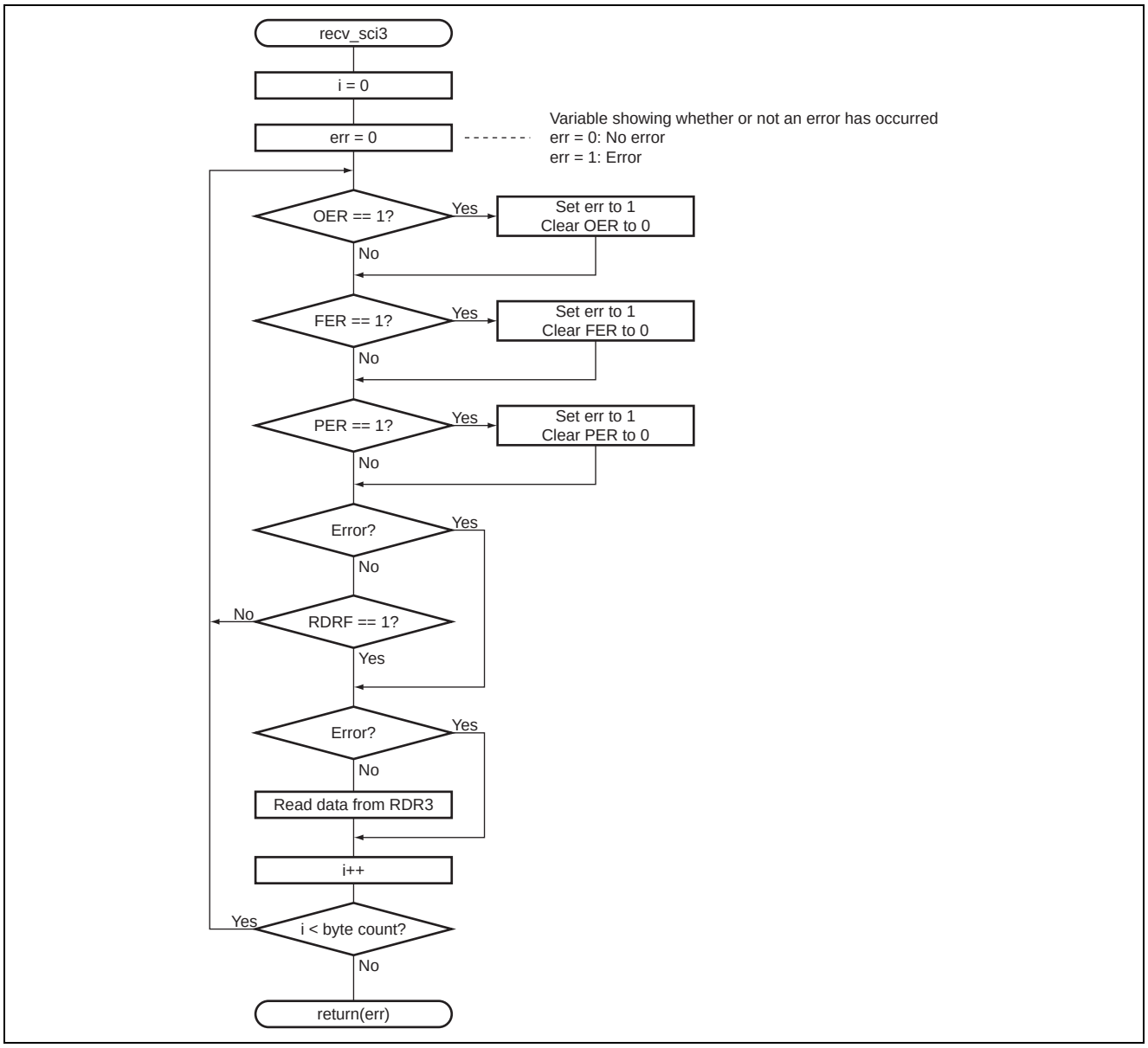
Bit	Bit Name	Set Value	R/W	Description
7	Bit 7	Undefined	R	RDR3 is an 8-bit register that stores receive data. When one frame of data has been received, it is transferred from RSR3 to this register, enabling RSR3 to receive the next frame of data. RSR3 and RDR3 have a double-buffered structure, so continuous reception is possible. Read RDR3 only once, after confirming that the RDRF bit in SSR3 is set to 1. RDR3 cannot be written to by the CPU. The initial value of RDR3 is H'00. RDR3 is initialized to H'00 at a reset, in the standby mode, watch mode, or module standby mode.
6	Bit 6	Undefined	R	
5	Bit 5	Undefined	R	
4	Bit 4	Undefined	R	
3	Bit 3	Undefined	R	
2	Bit 2	Undefined	R	
1	Bit 1	Undefined	R	
0	Bit 0	Undefined	R	

- SSR3 Serial Status Register 3 Address: H'FF9C

Bit	Bit Name	Set Value	R/W	Description
6	RDRF	Undefined	R/(W)*	Receive Data Register Full Indicates whether or not receive data is stored in RDR3. [Setting condition] • When reception ends normally and receive data is transferred from RSR3 to RDR3 [Clearing conditions] • When 0 is written to RDRF after it was read as 1 • When data is read from RDR3 If an error is detected during reception, or if the RE bit in SCR3 has been cleared to 0, RDR3 and the RDRF bit are not affected and retain their previous state. Note that if data reception is completed while bit RDRF is still set to 1, an overrun error (OER) will occur and the receive data will be lost.
5	OER	Undefined	R/(W)*	Overrun Error [Setting condition] • When an overrun error occurs during reception [Clearing condition] • When 0 is written to OER after it was read as 1 When the RE bit in SCR3 is cleared to 0, the OER bit is not affected and retains its previous state. When an overrun error occurs, RDR3 retains the receive data it held before the overrun error occurred, and data received after the error is lost. Reception cannot be continued with the OER bit set to 1.
4	FER	Undefined	R/(W)*	Framing Error [Setting condition] • When a framing error occurs during reception [Clearing condition] • When 0 is written to FER after it was read as 1 When the RE bit in SCR3 is cleared to 0, the FER bit is not affected and retains its previous state. Note that, in 2-stop-bit mode, only the first stop bit is checked for a value of 1; the second stop bit is not checked. If a framing error occurs, the receive data is transferred to RDR3 but the RDRF bit is not set. Reception cannot be continued with the FER bit set to 1.
3	PER	Undefined	R/(W)*	Parity Error [Setting condition] • When a parity error is generated during reception [Clearing condition] • When 0 is written to PER after it was read as 1 When the RE bit in SCR3 is cleared to 0, the PER bit is not affected and retains its previous state. Receive data in which a parity error has occurred is still transferred to RDR3, but the RDRF bit is not set. Reception cannot be continued with the PER bit set to 1.

Note: * Only 0 can be written to clear the flag.

3. Flowchart


recv_sci3
i = 0
err = 0
Variable showing whether or not an error has occurred
err = 0: No error
err = 1: Error
OER == 1?
Yes
Set err to 1
Clear OER to 0
No
FER == 1?
Yes
Set err to 1
Clear FER to 0
No
PER == 1?
Yes
Set err to 1
Clear PER to 0
No
Error?
Yes
No
No
RDRF == 1?
Yes
Error?
Yes
No
Read data from RDR3
i++
Yes
i < byte count?
No
return(err)

4.4.4 stop_sci3() Function

1. Module Specifications

- Ends the asynchronous mode

Table 7 Module Specifications

Item	Type	Variable	Description
Arguments	None	None	None

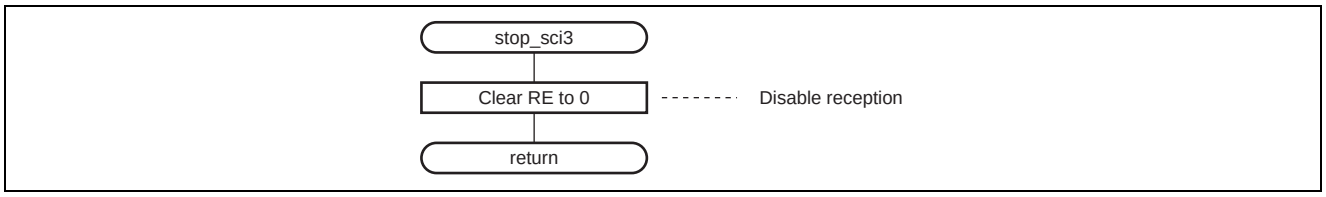
2. Internal Registers Used

The internal registers used in this sample task are shown below. The set values shown are those used in the sample task and differ from the initial values.

- SCR3 Serial Control Register 3 Address: H'FF9A

Bit	Bit Name	Set Value	R/W	Description
4	RE	0	R/W	Receive Enable Reception is enabled when this bit is set to 1. Serial data reception is started when a start bit is detected in the asynchronous mode. Be sure to carry out SMR3 settings to determine the reception format before setting the RE bit to 1. Note that the RDRF, FER, PER, and OER flags in SSR3 are not affected when the RE bit is cleared to 0, and retain their previous state.

3. Flowchart



4.5 Link Address Specifications

Section Name	Address
CVECT	H'0000
P	H'0100

Revision Record

Rev.	Date	Description	
		Page	Summary
1.00	Mar.18.05	—	First edition issued

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