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SH7780 Group

Example of TMU Operation (Generating 1 Second by Fixed Interval Timer)

Introduction

This document gives examples of setting the TMU (as a fixed-interval timer generating one-second intervals) of the SH7780 Group and describes a sample application for this purpose.

Target Device

SH7780 (MS7780SE03 Solution Engine by Hitachi ULSI Systems)

Contents

1. Preface

1.1 Specifications

- The timer unit (TMU channel 0) is used as a fixed-interval timer to measure 5-ms periods.
- The underflow interrupt (TUNI0) is used to drive counting-up every time it is generated, 1-s intervals are generated from the counter.

1.2 Module Used

- Timer unit (TMU channel 0)

1.3 Applicable Conditions

• MCU	SH7780	
• Operating frequency	Internal clock	: 400 MHz
	SuperHyway clock	: 200 MHz
	Peripheral clock	: 33 MHz
	DDR clock	: 160 MHz
	External clock	: 33 MHz
	PCI bus clock	: 33 MHz
• Clock operating mode	Mode 3 (MODE7 = low, MODE2 = low, MODE1 = high, MODE0 = high)	
• Data alignment	Little endian	
• Addressing mode	29-bit	
• C compiler	SuperHRISC Engine Family C/C++ Compiler Package Ver.9.1.0 (manufactured by Renesas Technology)	

1.4 Related Application Note

The operation of the reference program for this document was confirmed with the setting conditions described in the following application note: *SH7780 Initialization Example* (REJ06B0712-0100). Please refer to the application note in combination with this one.

2. Description of the Sample Application

This sample program uses the timer unit (TMU channel 0) to drive counting at a fixed interval.

2.1 Description of the Sample Program

This sample program consists of the following four source files.

(1) tmu.c
(2) main.c
(3) intprg.c
(4) vecttbl.src

(1) tmu.c describes the function used to set up TMU operations in this sample program.
This program code is not included in the application for *SH7780 Initialization Example*, which is used as its basis.

(2) main.c sets the status register (SR) and calls the function to set up the TMU operation.
Change main.c that was included with *SH7780 Initialization Example* as required to match main.c for this sample program.

(3) intprg.c describes the interrupt program called from the exception/interrupt handler.
Change intprg.c that was included with *SH7780 Initialization Example* as required to match intprg.c for this sample program.

(4) vecttbl.src describes the exception/interrupt vector table (including vector-table entries), and interrupt mask table.
To ensure that interrupts that have been accepted are not accepted again while they are being processed, the interrupt mask levels to be set in the IMASK bits of the status register should be described in the interrupt mask table.
Change vecttbl.src that was included with *SH7780 Initialization Example* as required to match vecttbl.src for this sample program.

2.2 Operational Overview of the Module Used

Each channel of the TMU has a 32-it timer counter (TCNT) and a 32-bit timer constant register (TCOR). Each TCNT performs count-down operation. The channels have an auto-reload function that allows a cyclic count operation, and can also perform external event counting. Channel 2 also has an input capture function.

When one of bits STR5 to STR0 in TSTR0 and TSTR1 is set to 1, the TCNT for the corresponding channel starts counting down. When the TCNT reaches 0, the underflow flag (UNF) in the corresponding timer control register (TCR) is set to 1. If the underflow interrupt control bit (UNIE) in the corresponding TCR is set to 1 at this time, an underflow interrupt (TUNI) is generated. At the same time, the value is copied from TCOR into TCNT, and the count-down continues (auto-reload function).

Table 1 gives an overview of the TMU.

Table 1 TMU Overview

Item	Overview
No. of channels available	6 (channels 0 to 5)
Counter	Auto-reload type 32-it counter (down-count only)
Pin function	TCLK (48-pin I/O): Channels 0, 1, and 2 external clock input pin/ Channel 2 input capture input pin/ RTC output pin (shared with the RTC)
Clock source	Pck/4, Pck/16, P/64, P/256, and Pck/1024 (Pck is the peripheral clock), On-chip RTC output clock: Selection of channels 0 to 5 External clock: Selection of channels 0 to 2 only
Boot method	Software boot (by writing the timer start register)
Trigger for underflow	An underflow is generated when the timer-counter counts down from 0.
Trigger of Input capture	Input capture proceeds when the edge specified by CKEG0 and CKEG1 in timer control register 2 (TCR2) is input to TCLK.
Interrupt requests	Underflow interrupt (TUNI): Channels 0 to 5 Input capture interrupt (TCPI): Channel 2 only

2.3 Procedure for Setting Module Used

This section describes the procedure for setting up the timer unit (TMU channel 0) for cyclic-counting operation.

In this program, the following initial settings are made at the beginning of the main function on the assumption that this is based on the program for *SH7780 Initialization Example*. Since operation in privileged mode is a precondition for the program doing this, take care with regard to the processing mode when you adapt this code for use with other programs etc.

Figure 1 shows an example of the sequence for setting the cyclic count operation of the TMU. For details on the settings of individual registers, see the *SH7780 Group Hardware Manual*.

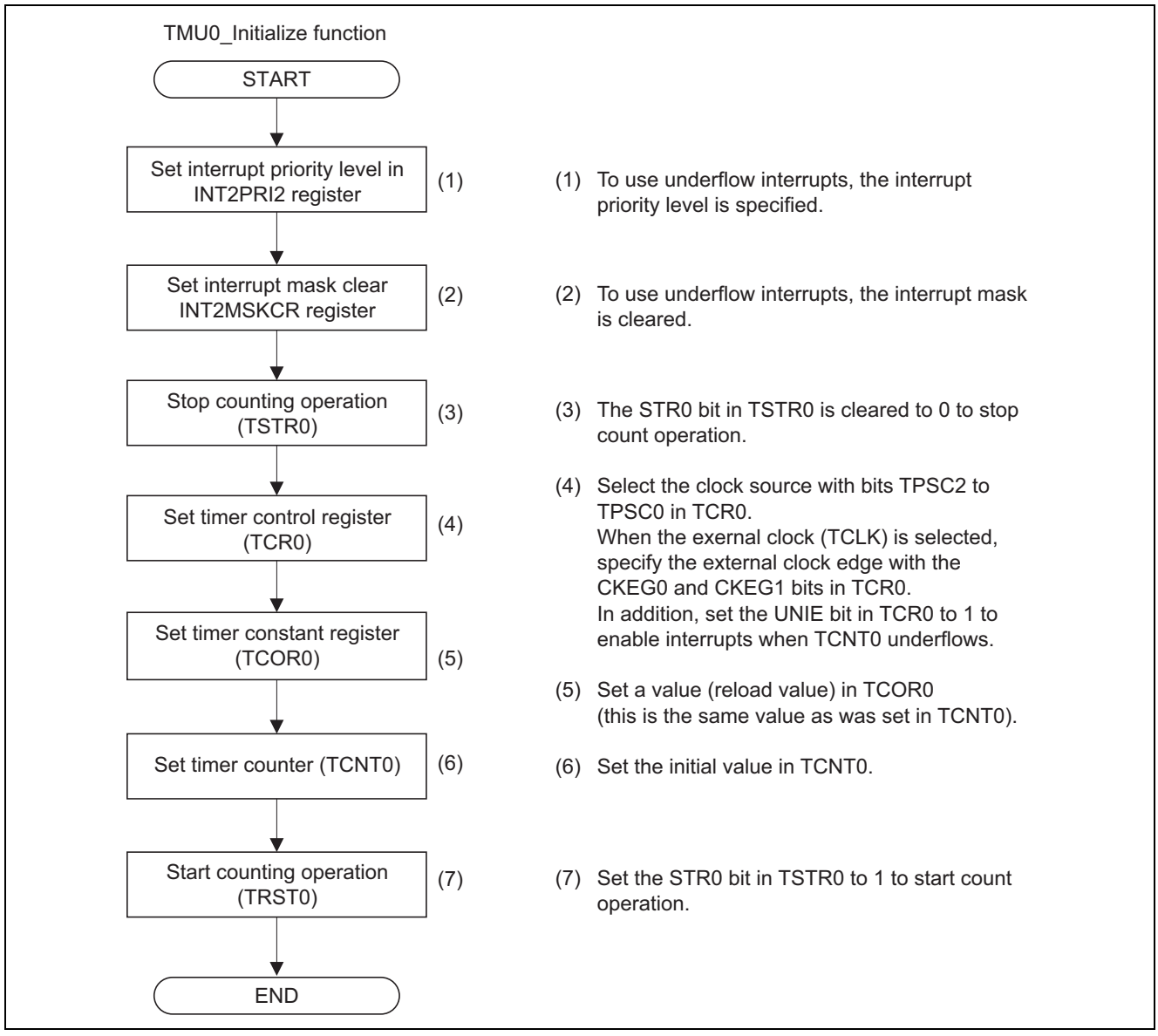


Figure 1 Flow of Setting TMU Cyclic Count Operation

2.4 Operation of the Sample Program

The sample program uses the timer unit (TMU channel 0) as a fixed-interval timer with an interval of 5 ms.

The underflow interrupt (TUNI) is used to drive counting up every 5 ms.

Figure 2 shows the timing of operations of the sample program.

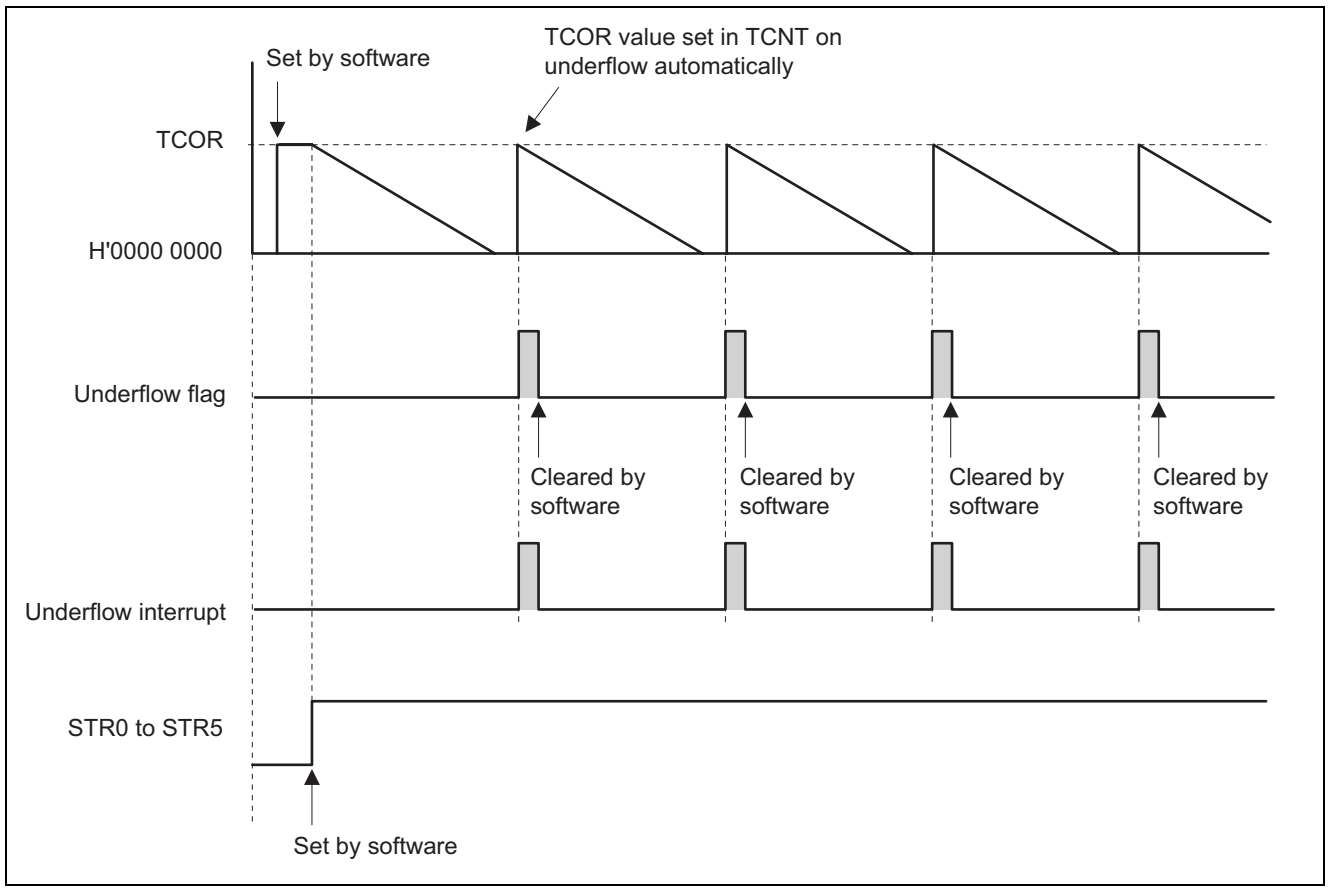


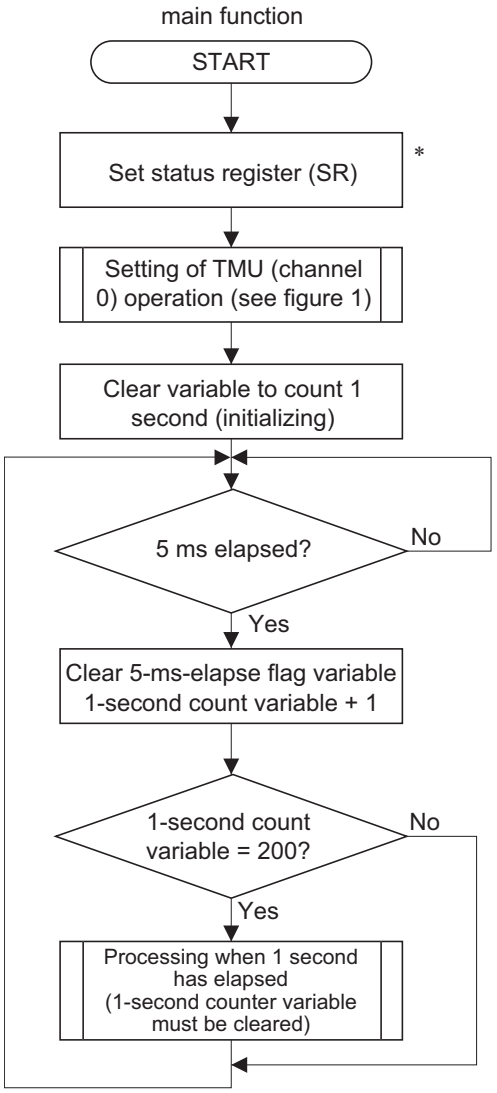
Figure 2 Timing of Operations of the Sample Program

2.5 Procedure for Processing the Sample Program

Table 2 gives examples for setting the TMU. Figures 3 and 4 provide sample flowcharts of the main function and underflow interrupt handling of the sample program.

Table 2 TMU Setting

Register Name	Address	Setting	Function
Interrupt priority register 0 (INT2PRI0)	H'FFD4 0000	H'1F00 0000	TMU-ch0 interrupt priority level: 31
Interrupt mask clear register (INT2MSKCR)	H'FFD4 003C	H'0000 0001	TMU-ch0 to ch2 interrupt mask clear
Timer start register 0 (TSTR0)	H'FFD8 0004	H'0000 0000	STR0 = 0: Stops counting
		H'0000 0001	STR0 = 1: Starts counting
Timer constant register 0 (TCOR0)	H'FFD8 0008	H'0000 A122	41250 times (H'A122): Approximately 5 ms
Timer counter 0 (TCNT0)	H'FFD8 000C	H'0000 A122	41250 times (H'A122): Approximately 5 ms
Timer control register 0 (TCR0)	H'FFD8 0010	H'0000 0020	TPSC0 to TPSC2: Pck/4 Enables underflow interrupts



MD: "1", privileged mode
BL: "0", exeptions and interrupts are not blocked.
IMASK: Interrupt mask level = 14

Note: * Since this program directly changes registers for peripheral functions, the MD bit (processing mode bit) is set to 1 (privileged mode). If this bit is changed to "0" (user mode) and the furnction for setting operations is called, access to the registers for peripheral functions leads to an address error.

Figure 3 Flow of Processing by the Main Function of the Sample Program (Generation of 1-Second Intervals by a Fixed-Interval Timer)

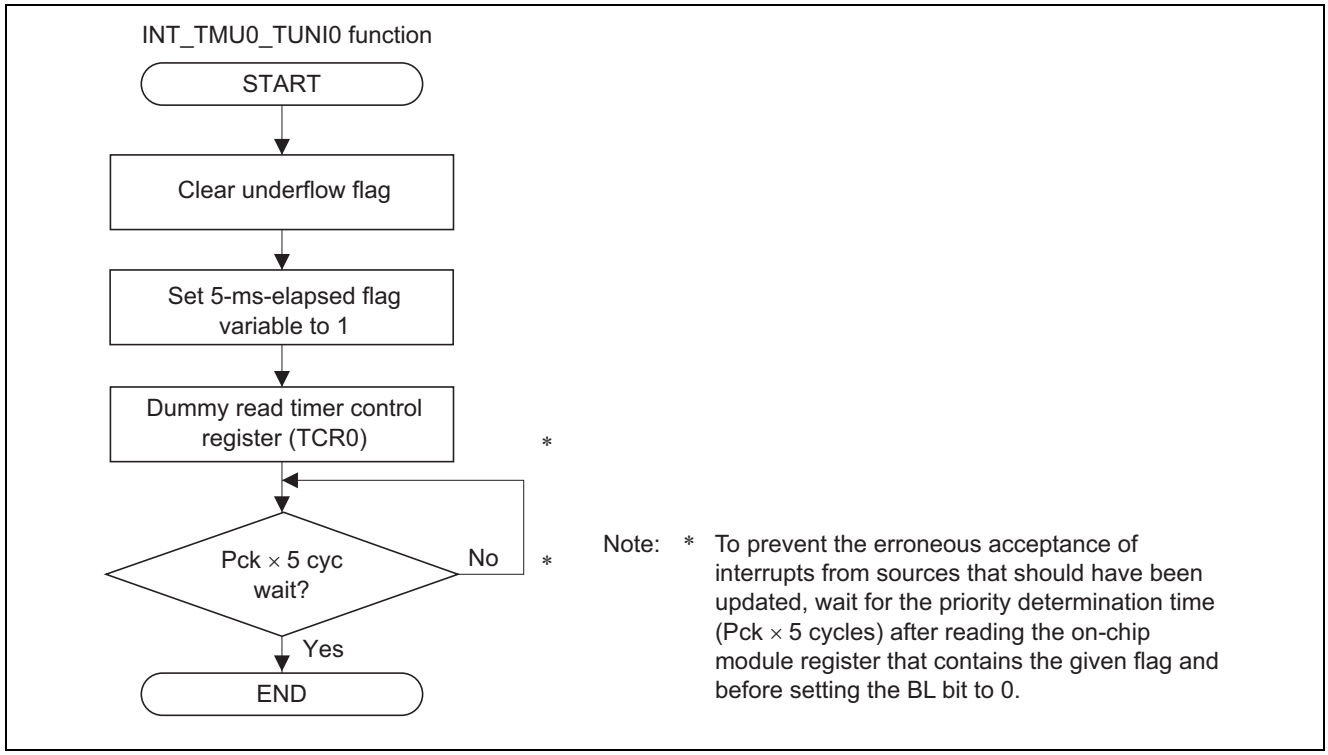


Figure 4 Flow of TUNI0 (Underflow) Interrupt Handling

3. Listing of Sample Program

1. Sample Program Listing: "main.c" (1)

```
1   /*""FILE COMMENT""*******************************************************************
2   *     System Name :   SH7780 Sample Program
3   *     File Name   :   main.c
4   *     Version     :   1.00.00
5   *     Contents    :   SH7780 Initialize Program
6   *     Model       :   Hitachi_ULSI_Systems SolutionEngine MS7780SE03
7   *     CPU         :   SH7780
8   *     Compiler    :   SHC.9.1.00
9   *     OS          :   none
10  *
11  *     note        :   < Caution >
12  *                     This sample program is provided simply as a reference and
13  *                     its operation is not guaranteed.
14  *                     Use this sample program as a technical reference when
15  *                     developing software.
16  *
17  * Copyright (C) 2007 Renesas Technology Corp. All Rights Reserved
18  *
19  *     History     :   2007/12/26 ver 1.00.00
20  *
21  ****************************************************************************************/
22  #include <machine.h>
23
24  /* --- Function Definition(internal) --- */
25
26  /* --- Symbol Definition --- */
27  #define  SR_Init        0x400000e0         /* Privileged mode, RB,BL=0, IMASK level 14 */
28
29  /* --- RAM allocation variable declaration --- */
30  volatile unsigned char u1Flg5ms;
31  volatile unsigned char u1Cnt1s;
```

2. Sample Program Listing: "main.c" (2)

```
/***** Function Comment ***************************************
* Outline          : main
*-------------------------------------------------------------
* Declaration  : void main(void)
*-------------------------------------------------------------
* Functional description:
*                  main function
*-------------------------------------------------------------
* Return Value : -
* Argument     : -
*-------------------------------------------------------------
* Input        : -
* Output           : -
*-------------------------------------------------------------
* Notes        : -
****** Function Comment End *********************************/
void main(void)
{
    set_cr(SR_Init);          /* Set SR "Privileged mode, RB,BL=0, IMASK level 14" */

    TMU0_Initialize();        /* TMU0 Initialize (additional part from Initialize program)*/

    while(1)
    {                         /* (start of additional part from Initialize program) */
        while(u1Flg5ms == 0x00)
        {
        }
        u1Flg5ms = 0;         /* clear 5ms flag */
        u1Cnt1s++;            /* 1s count +1 */

        if(u1Cnt1s == 0xc8)
        {
                              /* 1s fixed period routine */
            u1Cnt1s = 0;      /* clear 1s count */
        }
    }
}                                     /* (end of additional part from Initialize program) */
```

3. Sample Program Listing: "tmu.c" (1)

```
1   /*""FILE COMMENT""*****************************************************************
2   *       System Name :   SH7780 Sample Program
3   *       File Name   :   tmu.c
4   *       Version     :   1.00.00
5   *       Contents    :   SH7780 Initialize Program
6   *       Model       :   Hitachi_ULSI_Systems SolutionEngine MS7780SE03
7   *       CPU         :   SH7780
8   *       Compiler    :   SHC.9.1.00
9   *       OS          :   none
10  *
11  *       note        :   < Caution >
12  *                       This sample program is provided simply as a reference and
13  *                       its operation is not guaranteed.
14  *                       Use this sample program as a technical reference when
15  *                       developing software.
16  *
17  *   Copyright (C) 2007 Renesas Technology Corp. All Rights Reserved
18  *
19  *       History     :   2007/12/26  ver 1.00.00
20  *
21  ******************************************************************************/
22  /* --- Function Definition(internal) --- */
23  void TMU0_Initialize(void);
24
25  /* --- Symbol Definition --- */
26  struct st_tmu{                                          /* struct TMU0  */
27                unsigned int     TCOR;                    /*     TCOR      */
28                unsigned int     TCNT;                    /*    TCNT       */
29                union {                                   /*    TCR        */
30                      unsigned short WORD;                /*  Word Access  */
31                      struct {                            /*  Bit  Access  */
32                             unsigned short     :7;       /*               */
33                             unsigned short UNF :1;       /*    UNF        */
34                             unsigned short     :2;       /*               */
35                             unsigned short UNIE:1;       /*    UNIE       */
36                             unsigned short CKEG:2;       /*    CKEG       */
37                             unsigned short TPSC:3;       /*    TPSC       */
38                             }       BIT;                 /*               */
39                      }          TCR;                     /*               */
40  };
41
42  #define TSTR0  (*(volatile unsigned char  *)0xFFD80004)      /* TSTR0 Address*/
43  #define TMU0   (*(volatile struct st_tmu  *)0xFFD80008)      /* TMU0  Address*/
44  #define INT2MSKCR  (*(volatile unsigned int   *)0xFFD4003C)  /* INT2MSKCR Address */
45  #define INT2PRI0   (*(volatile unsigned int   *)0xFFD40000)  /* INTPRI0 Address */
46
```

4. Sample Program Listing: "tmu.c" (2)

```
47  /***** Function Comment ***************************************
48  * Outline      : TMU0_Initialize
49  *-------------------------------------------------------------
50  * Declaration  : void TMU0_Initialize(void)
51  *-------------------------------------------------------------
52  * Functional description:
53  *                TMU0 Initialize and count start
54  *-------------------------------------------------------------
55  * Return Value : -
56  * Argument     : -
57  *-------------------------------------------------------------
58  * Input        : -
59  * Output       : -
60  *-------------------------------------------------------------
61  * Notes        : -
62  ****** Function Comment End *********************************/
63  void TMU0_Initialize(void)
64  {
65      INT2PRI0 |= 0x1f000000;              /* TMU ch0 interrupt level 31 */
66      INT2MSKCR = 0x00000001;              /* TMU ch0 interrupt mask clear */
67
68      TMU0.TCR.WORD = 0x0020;              /* TUNI0 enable, count clock=Pck/4 */
69      TMU0.TCOR = 0x0000A122;              /* TMU ch0 5ms set */
70      TMU0.TCNT = 0x0000A122;
71
72      TSTR0 = 0x01;                        /* TMU ch0 count start */
73  }
```

5. Sample Program Listing: "intprg.c" (1)

```
1   /*""FILE COMMENT""*****************************************************************
2   *       System Name :   SH7780 Sample Program
3   *       File Name   :   intprg.c
4   *       Version     :   1.00.00
5   *       Contents    :   SH7780 Initialize Program
6   *       Model       :   Hitachi_ULSI_Systems SolutionEngine MS7780SE03
7   *       CPU         :   SH7780
8   *       Compiler    :   SHC.9.1.00
9   *       OS          :   none
10  *
11  *       note        :   < Caution >
12  *                       This sample program is provided simply as a reference and
13  *                       its operation is not guaranteed.
14  *                       Use this sample program as a technical reference when
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17  *   Copyright (C) 2007 Renesas Technology Corp. All Rights Reserved
18  *
19  *       History     :   2007/12/26  ver 1.00.00
20  *
21  ******************************************************************************/
22  #include <machine.h>
23
24  /* --- Function Definition(internal) --- */
25  static void int_responstime_wait(unsigned int wait_time);
26
27  /* --- Symbol Definition --- */
28  struct st_tmu{                                          /* struct TMU0  */
29                  unsigned int     TCOR;                  /*     TCOR      */
30                  unsigned int     TCNT;                  /*    TCNT       */
31                  union {                                 /*    TCR        */
32                        unsigned short WORD;              /*  Word Access */
33                        struct {                          /*  Bit  Access */
34                               unsigned short     :7;     /*              */
35                               unsigned short UNF :1;     /*    UNF       */
36                               unsigned short     :2;     /*              */
37                               unsigned short UNIE:1;     /*    UNIE      */
38                               unsigned short CKEG:2;     /*    CKEG      */
39                               unsigned short TPSC:3;     /*    TPSC      */
40                               }       BIT;               /*              */
41                        }          TCR;                   /*              */
42  };
43
44  #define TMU0    (*(volatile struct st_tmu  *)0xFFD80008)  /* TMU0  Address */
45
46  #define INTC_RESPONSEWAIT  (0x00000014)       /* INT response wait Pck 5cycle
                                                     H'14 = (1/Pck*5cyc) / (1/Ick*3cyc) */
```

6. Sample Program Listing: "intprg.c" (2)

```
216 /* H'580 TMU ch-0 underflow interrupt */
217 void INT_TMU0_TUNI0(void)
218 {                               /* (start of additional part from Initialize program) */
219   volatile unsigned short dummy;
220
221   TMU0.TCR.BIT.UNF = 0;      /* TMU ch0 UNF flag clear */
222   u1Flg5ms = 1;              /* set 5ms flag */
223   dummy = TMU0.TCR.WORD;     /* dummy read */
224
225   int_responstime_wait(INTC_RESPONSEWAIT);  /* 5cyc(Pck=33MHz) wait */
226 }                                   /* (end of additional part from Initialize program) */
227


503   #pragma inline_asm(int_responstime_wait)
504   static void int_responstime_wait(unsigned int wait_time)
505   {
506   ?0001:
507                 DT          R4
508                 BF          ?0001
509                 NOP
510   }
```

7. Sample Program Listing: "vecttbl.src"

```
1     ;*""FILE COMMENT""*********************************************************************
2     ;       System Name :   SH7780 Sample Program
3     ;       File Name   :   vecttbl.src
4     ;       Version     :   1.00.00
5     ;       Contents    :   SH7780 Initialize Program
6     ;       Model       :   Hitachi_ULSI_Systems SolutionEngine MS7780SE03
7     ;       CPU         :   SH7780
8     ;       Compiler    :   SHC.9.1.00
9     ;       OS          :   none
10    ;
11    ;       note        :   < Caution >
12    ;                       This sample program is provided simply as a reference and
13    ;                       its operation is not guaranteed.
14    ;                       Use this sample program as a technical reference when
15    ;                       developing software.
16    ;
17    ;   Copyright (C) 2007 Renesas Technology Corp. All Rights Reserved
18    ;
19    ;       History     :   2007/12/26  ver 1.00.00
20    ;
21    ;*****************************************************************************************/
22
23                    .include    "vect.inc"
24
25                    .section    VECTTBL,data
26                    .export     _RESET_VECTORS

305   ;TMU-ch0
306                   ;H'580      TMU_TUNI0
307                   .data.b      H'F0        /* (change part from Initialize program) */
308   ;TMU-ch1
309                   ;H'5A0      TMU_TUNI1
310                   .data.b      H'00
311   ;TMU-ch2
312                   ;H'5C0      TMU_TUNI2
313                   .data.b      H'00
314                   ;H'5E0      TMU_TICPI2
315                    .data.b     H'00
316                   ;H'600      _INT_H_UDII
317                    .data.b     H'00
318                   ;H'620      reserve
319                    .data.b     H'00
```

4. Documents for Reference

- Hardware Manual
  SH7780 Hardware Manual
  The most up-to-date version of this document is available on the Renesas Technology Website.
- Software Manual
  SH-4A Software Manual
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   (2) surgical implantations
   (3) healthcare intervention (e.g., excision, administration of medication, etc.)
   (4) any other purposes that pose a direct threat to human life

   Renesas shall have no liability for damages arising out of the uses set forth in the above and purchasers who elect to use Renesas products in any of the foregoing applications shall indemnify and hold harmless Renesas Technology Corp., its affiliated companies and their officers, directors, and employees against any and all damages arising out of such applications.
9. You should use the products described herein within the range specified by Renesas, especially with respect to the maximum rating, operating supply voltage range, movement power voltage range, heat radiation characteristics, installation and other product characteristics. Renesas shall have no liability for malfunctions or damages arising out of the use of Renesas products beyond such specified ranges.
10. Although Renesas endeavors to improve the quality and reliability of its products, IC products have specific characteristics such as the occurrence of failure at a certain rate and malfunctions under certain use conditions. Please be sure to implement safety measures to guard against the possibility of physical injury, and injury or damage caused by fire in the event of the failure of a Renesas product, such as safety design for hardware and software including but not limited to redundancy, fire control and malfunction prevention, appropriate treatment for aging degradation or any other applicable measures. Among others, since the evaluation of microcomputer software alone is very difficult, please evaluate the safety of the final products or system manufactured by you.
11. In case Renesas products listed in this document are detached from the products to which the Renesas products are attached or affixed, the risk of accident such as swallowing by infants and small children is very high. You should implement safety measures so that Renesas products may not be easily detached from your products. Renesas shall have no liability for damages arising out of such detachment.
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