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SH7720/SH7721 Group

Example of Setting LCD Controller

Introduction

This application note provides an example of setting the LCD controller (LCDC) incorporated in the SH7720 and SH7721 (hereafter referred to as SH7720).

Target Device

- Microcontroller: SH7720
  Operation frequency: Internal clock: 133 MHz
  Bus clock: 66 MHz
  Peripheral clock: 33 MHz
- Flash memory: 16 MB
- SDRAM: 32 MB × 2
- LCD panel interface: TFT color LCD 240 (H) × 320 (V) dots
  C compliler: Renesas Technology SuperH RISC engine family C/C++ compiler package Ver.9.00

Preface

The reference program described in this application note has been evaluated on the SH7720 Solution Engine with its initial settings. Check that the settings match.

This application note also makes basic settings for SH7720 peripheral functions as required for execution.

Use this sample program as a technical reference in the development of user software.

Contents

1. Specifications

This sample program displays a sample image on an LCD display by using the SH7720 LCDC.

2. Description of Modules Used

2.1 Overview of the LCDC

The SH7720 incorporates an LCD control function capable of connection to a color TFT/STN, since synchronous DRAM is used for the display buffer (VRAM), drawing processing can be performed directly from the CPU. The LCDC includes a line buffer, and data are read in bursts of bus cycles so that displayed images don't flicker because of other processing.

Table 1 Functions of LCDC

Item	Description	Remarks
Panel interface	Serial interface method	
LCD type	STN/Dual-STN/TFT	
Panel data format	8, 12, 16, or 18-bit bus width	When connecting the LCDC to a TFT panel with an 18-bit bus, the non-connected lower-order bit lines should be connected to GND or to the lowest bit for which data are output.
Color mode	4, 8, 15, or 16 bpp (bits per pixel)	
Grayscale mode	1, 2, 4, or 6 bpp	
Panel size	16 × 1 to 1024 × 1024 dots	See section 26.4.1 in the SH7720 manual. Note that the actual panel size is limited to the VGA size (approximately) in 16-bpp color mode due to the bus bandwidth of area 3 (used as VRAM) for synchronous DRAM
Color palette	24 bits	16 bits of the 24 bits are valid R: 5/G: 6/B: 5
STN/DSTN panel moderate color display	RGB 8 bits each, 24-bit space modulation FRC	Used to reduce flickers and shadowing of images with control of 65536 colors.
VRAM	Synchronous DRAM (area 3) connected to the CPU also serves as VRAM	Dedicated memory for the display is not necessary
Line buffer	2.4 kB	The display is stable
Signal polarity	Programmable	Supports the inversion of the output signal level
Data format	Capable of setting endian within a byte and selecting packed pixel method	
Hardware rotation mode	Supported	The horizontal width of the panel before rotation must be within 320 pixels
Interrupt	An interrupt can be generated at a user specified position	Used to avoid tearing images
Transfer of data from VRAM to line buffer	LCDC-internal circuit	

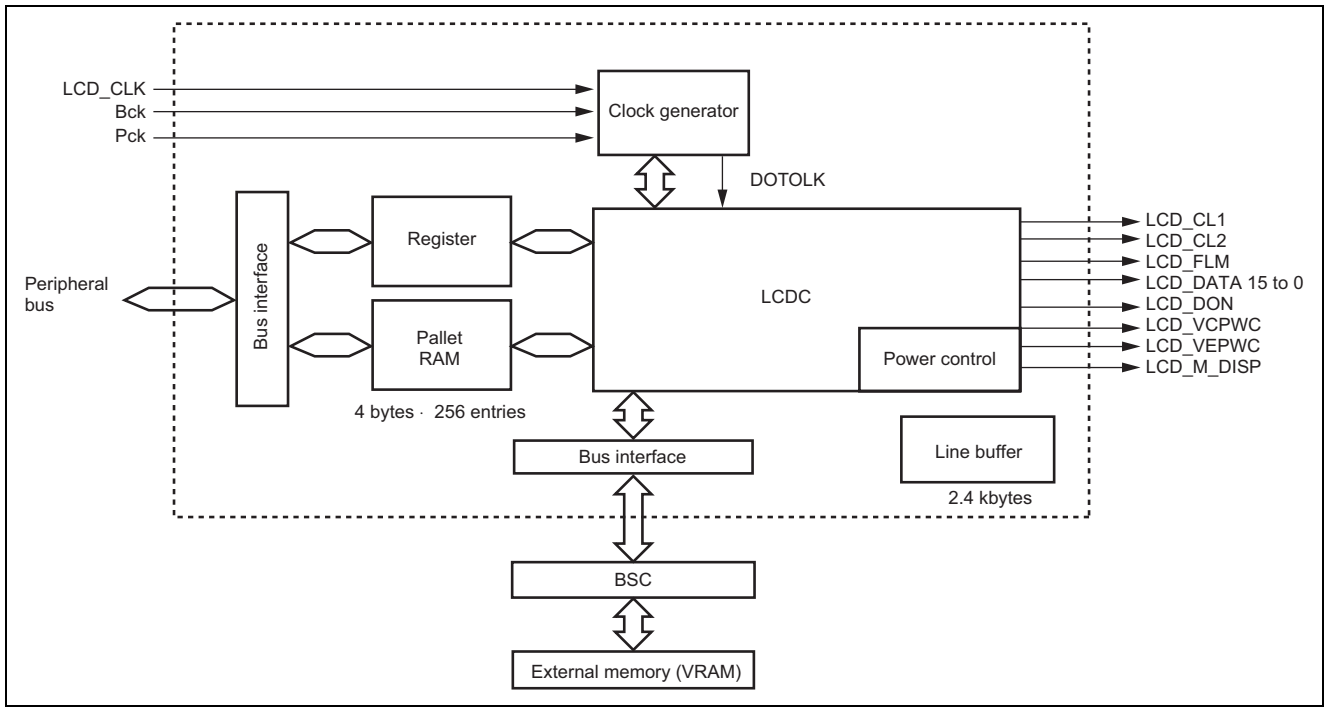


Figure 1 Block Diagram of LCDC

2.2 Specifications of LCD Board

This LCD board has a LCD panel (TFT LCD) that can display 16-bit RGB data at QVGA size (240 × 320). SDRAM allocated to area 3 (0X0c000000 to 0X0fffffff) is used as Video RAM for the LCD.

For more details, refer to MS7720RP02_MJ_1.0.pdf, the manual for SH7720 Solution Engine.

An example of connecting the LCD panel is provided in figure 2.

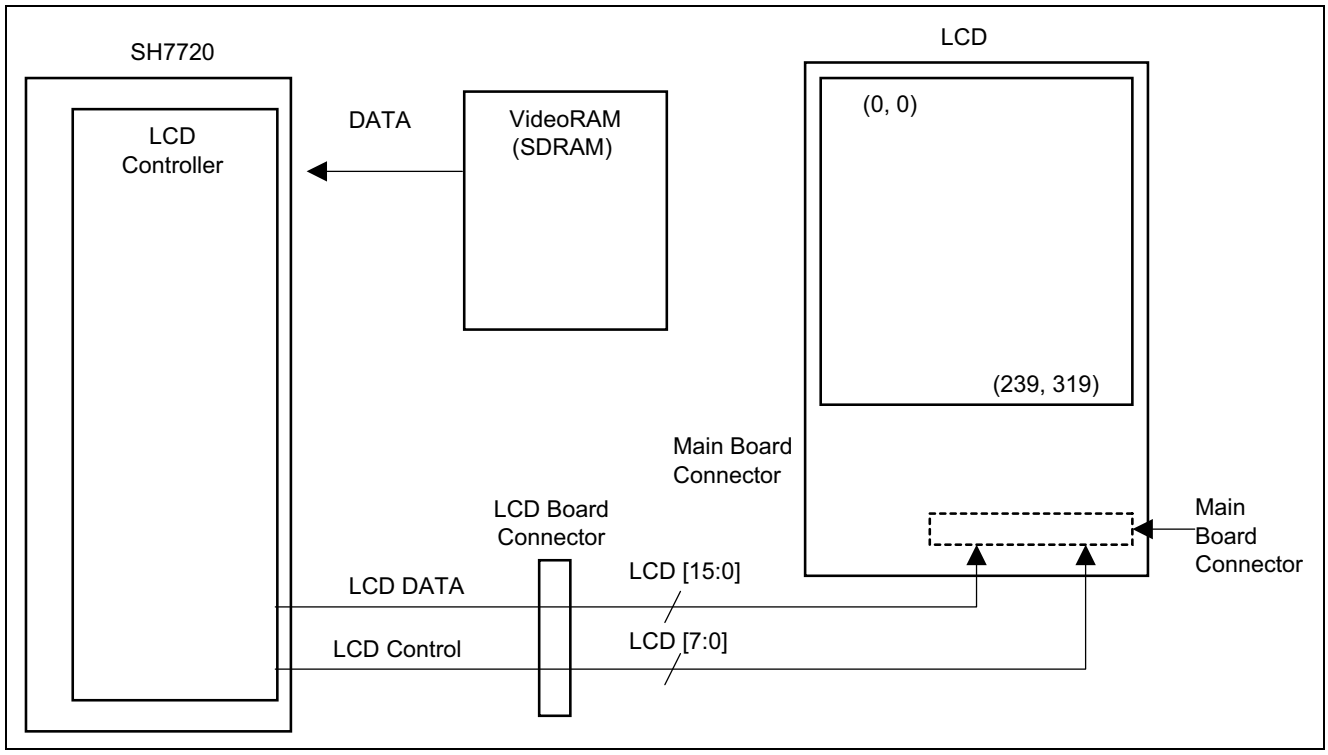


Figure 2 Example of Connecting LCD Panel

Data to be displayed are stored from the address specified by the SH7720 on-chip register for the LCD controller (LDSARU) in the order of coordinates, (0, 0), (1, 0) ... (239, 319). The data are then displayed on the LCD panel on the assumption that the top left is the origin (0, 0) and the bottom right is (239, 319).

The front light on the LCD panel can be turned on or off by using the power controller.

For more details, refer to MS7720RP02_MJ_1.0.pdf, the manual for the SH7720 Solution Engine.

The sample application employ the SH7720 to display data on a color TFT-LCD panel of QVGA size (240 × 320 dots) in 16-bit colors.

Table 2 LCDC registers

Name	Abbr.	Address	Access size
LCDC input clock register	LDICKR	H'A440 0400	16
LCDC module type register	LDMTR	H'A440 0402	16
LCDC data format register	LDDFR	H'A440 0404	16
LCDC scan mode register	LDSMR	H'A440 0406	16
LCDC data fetch start address register for upper display panel	LDSARU	H'A440 0408	32
LCDC data fetch start address register for lower display panel	LDSARL	H'A440 040C	32
LCDC fetch data line address offset register for display panel	LDLAOR	H'A440 0410	16
LCDC palette control register	LDPALCR	H'A440 0412	16
Palette data register 00 to FF	LDPR00 to FF	H'A440 0000 to H'A440 03FC	32
LCDC horizontal character number register	LDHCNR	H'A440 0414	16
LCDC horizontal synchronization signal register	LDHSYNR	H'A440 0416	16
LCDC vertical displayed line number register	LDVDLNR	H'A440 0418	16
LCDC vertical total line number register	LDVTLNR	H'A440 041A	16
LCDC vertical synchronization signal register	LDVSYNR	H'A440 041C	16
LCDC AC modulation signal toggle line number register	LDACLNR	H'A440 041E	16
LCDC interrupt control register	LDILNR	H'A440 0420	16
LCDC power management mode register	LDPMMR	H'A440 0424	16
LCDC power supply sequence period register	LDPSPR	H'A440 0426	16
LCDC control register	LDCNTR	H'A440 0428	16
LCDC memory access interval number register	LDLIRNR	H'A440 0440	16

3. Procedure for Specifying Settings

3.1 Settings for LCDC Registers

- Switch pins to the LCDC by the PFC.
- Then, initialize the LCDC according to the LCDC panel.
  Set the registers to suit the panel synchronization signal and the display area. The number of pixels in the horizontal direction must be specified in character units. A single character is 8 dots. The number in the vertical direction must be specified in horizontally displayed line units. SDRAM connected to area 3 is used as the display buffer (VRAM). Memory other than SDRAM cannot be used as VRAM. Even when the horizontal display width is 240 dots, set the number of horizontal characters (address along the Y axis) to a power of 2. For example, set this to 256 dots for a 240-dot display width.
- Take note of the following when setting the LCDC registers.
  1) Use a non-cached area for drawing processing. The LCD controller of the SH7720 only accesses SDRAM in area 3 and does not access the cache.
  2) The width of data processed by the SH7720 LCDC is 16 bits. When the LCDC is connected to a LCD module that has a 18-bit digital interface (R, G, B = 6, 6, 6), R, G, and B must be set to 5, 6, and 5, respectively, and the least significant bits of both R and B must be pulled up or down.
  3) Since the color mode is specified as 16 bpp (65536 colors) in this sample application and a single dot is 16-bit short type data, an array, unsigned short lcd [320] [256], is used.
- A description and notes on the routine for stopping the LCDC are provided below.
  Procedure for stopping access to the VRAM (synchronous DRAM in area 3) which holds the data to be displayed
  1. Make sure that the LPS1 and LPS0 bits in LDPMMR are 1.
  2. Set the DON bit in LDCNTR to 0 (display-off mode)
  3. Make sure that the LPS1 and LPS0 bits in LDPMMR are 0.
  4. Wait until a single frame has been displayed.

  This procedure must be applied before the VRAM enters self-refresh mode, or before standby mode or module standby mode is entered.

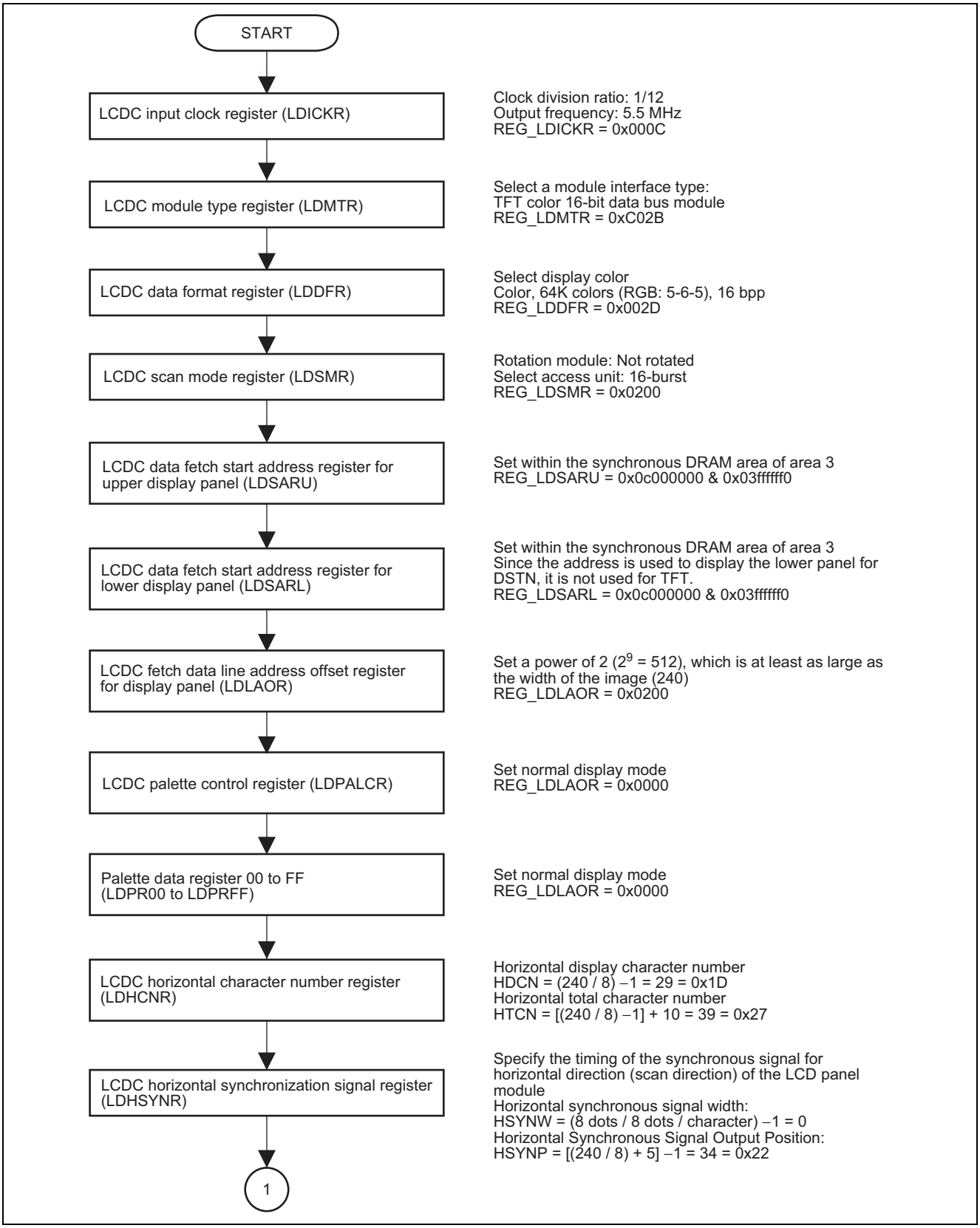


Figure 3 Flow of Setting LCDC Registers (1)

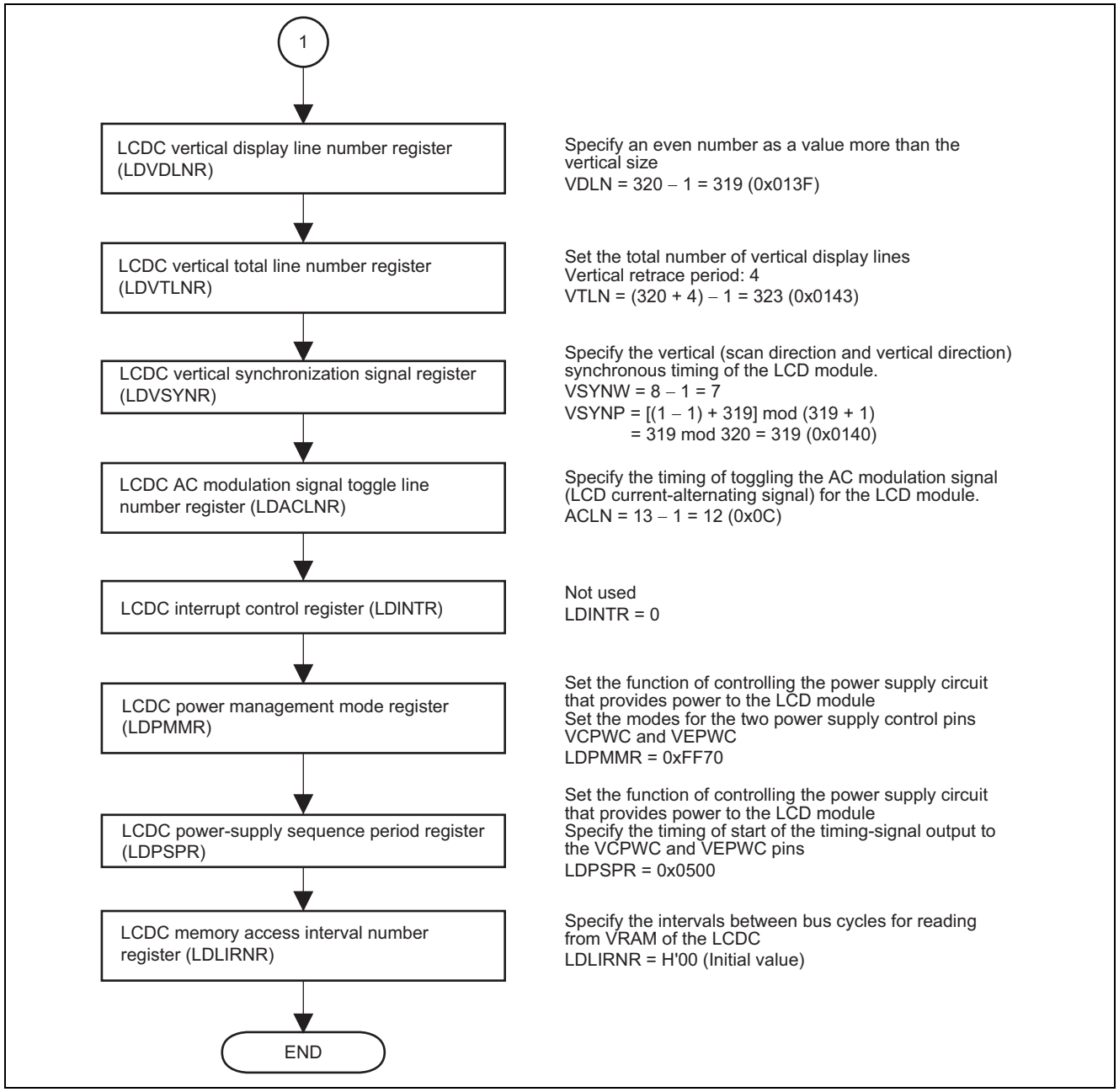


Figure 4 Flow of Setting LCDC Registers (2)

4. Description of Software

4.1 Descripsion of Modules

Module name	Function name	Description
Main Routione	main	Initializes, clears, and turns on the LCD, starts up the sample program
LCD Initialization	lcd_init	Specifies settings for the LCD, and clears LCDRAM
LCD Dot Data Program	lcd_dot_write	Program that creates dot data from the data for drawing
BSC Set	fmtool_r0k7720.hdc	Specifies settings for SDRAM in area 3

4.2 Description of Registers Used

The LCD controller (LCDC) is used to display images on the LCD panel.

Features of this system are as follows:

- Using the sample program provides a quick way of evaluating the LCD controller of the SH7720.
- The sample program supports control transfer for the LCD.

4.3 Register Settings for this Program

Table 3 Settings for LCDC Registers

Register Name	Bit Name	Settings	Address	Setting Value
LDICKR		LCDC Input Clock Register	H'A440 0400	
	ICKSEL1	Input Clock Select	Bit 13	ICKSEL1 = 0
	ICKSEL0	00: Bus clock is selected (Bck)	Bit 12	ICKSEL0 = 0
	DCDR5	Clock Division Ratio	Bit 5	DCDR5 = 0
	DCDR4	Clock Division Ratio: 1/12	Bit 4	DCDR4 = 0
	DCDR3	I/O clock frequency: 5.5 MHz	Bit 3	DCDR3 = 1
	DCDR2		Bit 2	DCDR2 = 1
	DCDR1		Bit 1	DCDR1 = 0
	DCDR0		Bit 0	DCDR0 = 0
LDMTR		LCDC Module Type Register	H'A440 0402	
	FLMPOL	FLM (Vertical Sync Signal) Polarity Select 1: LCD_FLM pulse is low active	Bit 15	FLMPOL = 1
	CL1POL	CL1 (Horizontal Sync Signal) Polarity Select 1: LCD_CL1 pulse is low active	Bit 14	CL1POL = 1
	DISPPOL	DISP (Display Enable) Polarity Select Selects the polarity of the LCD_M_DISP (display enable) for the LCD module. 0: LCD_M_DISP is high active	Bit 13	DISPPOL = 0
	DPOL	Display Data Polarity Select Selects the polarity of the LCD_DATA (display data) for the LCD module. 1: LCD_DATA is high active, transparent-type LCD panel	Bit 12	DPOL = 0
	MCNT	M Signal Control Sets whether or not to output the LCD's current-alternating signal of the LCD module. 0: M (AC line modulation) signal is output	Bit 10	MCNT = 0
	CL1CNT	CL1 (Horizontal Sync Signal) Control Sets whether or not to enable LCD_CL1 output during the vertical retrace period. 0: CL1 is output during vertical retrace period	Bit 9	CL1CNT = 0
	CL2CNT	CL2 (Dot Clock of LCD Module) Control Sets whether or not to enable LCD_CL2 output during the vertical and horizontal retrace period. 0: CL2 is output during vertical and horizontal retrace period	Bit 8	CL2CNT = 0
	MIFTYP5	Module Interface Type Select	Bit 5	MIFTYP5 = 1
	MIFTYP4	Set the LCD panel type and data bus width to be output to the LCD panel.	Bit 4	MIFTYP4 = 0
	MIFTYP3	101011: TFT color 16-bit data bus module	Bit 3	MIFTYP3 = 1
	MIFTYP2		Bit 2	MIFTYP2 = 0
	MIFTYP1		Bit 1	MIFTYP1 = 1
	MIFTYP0		Bit 0	MIFTYP0 = 1

Register Name	Bit Name	Settings	Address	Setting Value
LDDFR		LCDC Data Format Register	H'A440 0404	
	PABD	Byte Data Pixel Alignment Sets the pixel data alignment type in one byte of data. The contents of aligned data per pixel are the same regardless of this bit's setting. For example, data H'05 should be expressed as B'0101 which is the normal style handled by a MOV instruction of the this CPU, and should not be selected between B'0101 and B'1010. 0: Big endian for byte data	Bit 8	PABD = 0
	DSPCOLOR6	Display Color Select	Bit 6	DSPCOLOR6 = 0
	DSPCOLOR5	Set the number of display colors for the display	Bit 5	DSPCOLOR5 = 1
	DSPCOLOR4	0101101: Color, 64k colors (RGB: 565), 16 bpp	Bit 4	DSPCOLOR4 = 0
	DSPCOLOR3		Bit 3	DSPCOLOR3 = 1
	DSPCOLOR2		Bit 2	DSPCOLOR2 = 1
	DSPCOLOR1		Bit 1	DSPCOLOR1 = 0
	DSPCOLOR0		Bit 0	DSPCOLOR0 = 1
LDSMR		LCDC Scan Mode Register	H'A440 0406	
	ROT	Rotation Module Select Selects whether or not to rotate the display by hardware. 0: Not rotated	Bit 13	ROT = 0
	AU1	Access Unit Select	Bit 9	AU1 = 1
	AU0	Select access unit of VRAM. This bit is enabled when ROT = 1 (rotate the display). When ROT = 0, 16-burst memory read operation is performed regardless of the AU setting. 10: 16-burst	Bit 8	AU0 = 0
LDSARU		LCDC Start Address Register for Upper Display Data Fetch	H'A440 0408	
	SAU25 to SAU4	Start Address for Upper Display Data Fetch The start address for data fetch of the display data must be set within the synchronous DRAM area of area 3. LDSARU = 0xC3FFFFF0	Bit 25 to Bit 4	0xC3FFFFF0
LDSARL		LCDC Start Address Register for Lower Display Data Fetch	H'A440 040C	
	SAL25 to SAL4	Start Address for Lower Panel Display Data Fetch Only for DSTN, the start address for fetching data to be displayed on the lower panel must be set within the synchronous DRAM area of area 3. This setting is not required for STN and TFT. Since a TFT LCD is used in this example, this register is not set.	Bit 25 to Bit 4	—

Register Name	Bit Name	Settings	Address	Setting Value
LDLAOR		LCDC Line Address Offset Register for Display Data Fetch	H'A440 0410	
	LAO15 to LAO10	Line Address Offset Should be a power of 2 (512), which is at least as large as the horizontal width of the image (240). $240 \leq 2^9 = 512 = H'0200$	Bit 15 to Bit 10	LAO15 to LAO10 = 0
	LAO9		Bit 9	LAO9 = 1
	LAO8		Bit 8	LAO8 = 0
	LAO7		Bit 7	LAO7 = 0
	LAO6 to LAO0		Bit 6 to Bit 0	LAO6 to LAO0 = 0
LDPALCR		LCDC Palette Control Register	H'A440 0412	
	PALS	Palette State Indicates the access right state of the palette. 0: LCDC uses the palette. Normal display mode. (Initial value)	Bit 4	PALS = 0
	PALEN	Palette Read/Write Enable Requests the access right to the palette. 0: Request for transition to normal display mode (Initial value)	Bit 0	PALEN = 0
LDPR00 to LDPRFF		Palette Data Registers 00 to FF	H'A440 0000 to H'A440 03FC	
	PALDnn23 to PALDnn0	Palette Data Bits 18 to 16, 9, 8, and 2 to 0 are reserved within each RGB palette and cannot be set. However, these bits can be extended according to the upper bits. Since the palette is not used in this sample application, this register is not set.	—	—
LDHCNR		LCDC Horizontal Character Number Register	H'A440 0414	
	HDCN7 HDCN6 HDCN5 HDCN4 HDCN3 HDCN2 HDCN1 HDCN0	Horizontal Display Character Number Set the number of horizontal display characters (unit: character = 8 dots). Since the horizontal width is 240 pixels in this sample application, the following setting is applied: HDCN = (Display character number) – 1 = (240 / 8) – 1 = 29 = H'1D	Bit 15 to Bit 8	HDCN7 to HDCN0 = 0x1D
	HTCN7 HTCN6 HTCN5 HTCN4 HTCN3 HTCN2 HTCN1 HTCN0	Horizontal Total Character Number Set the number of total horizontal characters (unit: character = 8 dots). The minimum horizontal retrace period is three characters (24 dots). The horizontal retrace period is set to 10 characters (80 dots) in this sample application. HTCN = [(240 / 8) – 1] + 10 = 39 = H'27	Bit 7 to Bit 0	HTCN7 to HTCN0 = 0x27

Register Name	Bit Name	Settings	Address	Setting Value
LDHSYNR		LCDC Horizontal Sync Signal Register	H'A440 0416	
	HSYNW3 HSYNW2 HSYNW1 HSYNW0	Horizontal Sync Signal Width Set the width of the horizontal sync signals (CL1 and Hsync) (unit: character = 8 dots). HSYNW = (horizontal sync signal width) – 1 = (8dots/8dots/character) – 1 = 0	Bit15 to Bit 12	HSYNW3 to HSYNW0 = 0x00
	HSYNP7 HSYNP6 HSYNP5 HSYNP4 HSYNP3 HSYNP2 HSYNP1 HSYNP0	Horizontal Sync Signal Output Position Set the output position of the horizontal sync signals (unit: character = 8 dots). Must be set to (Horizontal sync signal output position) – 1. HSYNP = [(240 / 8) + 5] – 1 = H'22	Bit 7 to Bit 0	HSYNP7 to HSYNP0 = 0x22
LDVDLNR		LCDC Vertical Display Line Number Register	H'A440 0418	
	VDLN10 VDLN9 VDLN8 VDLN7 VDLN6 VDLN5 VDLN4 VDLN3 VDLN2 VDLN1 VDLN0	Vertical Display Line Number Set the number of vertical display lines (unit: line). Must be set to (number of display line) – 1. VDLN = 320 – 1 = 319 = H'013F	Bit 10 to Bit 0	VDLN10 to VDLN0 = 0x13F
LDVTLNR		LCDC Vertical Total Line Number Register	H'A440 041A	
	VTLN10 VTLN9 VTLN8 VTLN7 VTLN6 VTLN5 VTLN4 VTLN3 VTLN2 VTLN1 VTLN0	Vertical Total Line Number Set the total number of vertical display lines (unit: line). Must be set to (total line number) – 1. For the vertical retrace period of 4 lines: VTLN = (320 + 4) – 1 = 323 = H'0143	Bit 10 to Bit 0	VTLN10 to VTLN0 = 0x143

Register Name	Bit Name	Settings	Address	Setting Value
LDVSYNR		LCDC Vertical Sync Signal Register	H'A440 041C	
	VSYNW3 VSYNW2 VSYNW1 VSYNW0	Vertical Sync Signal Width Set the width of the vertical sync signals (FLM and Vsync) (unit: line). Must be set to (vertical sync signal width) – 1. For the vertical sync signal width of 8 lines: VSYNW = (8 – 1) = 7 = H'07	Bit 15 to Bit 12	VSYNW3 to VSYNW0 = 0x07
	VSYNP10 VSYNP9 VSYNP8 VSYNP7 VSYNP6 VSYNP5 VSYNP4 VSYNP3 VSYNP2 VSYNP1 VSYNP0	Vertical Sync Signal Output Position Set the output position of the vertical sync signals (FLM and Vsync) (unit: line). Must be set to (vertical sync signal output position) – 2. Since a LCD with 320 lines is used and the retrace period is 0 lines in this sample application, the vertical sync signal is activated at the first line with VTLN of 319. For a single display: VSYNP = [(1 – 1) + VTLN] mod (VTLN + 1) = [(1 – 1) + 319] mod (319 + 1) = 319 mod 320 = 319 = H'140	Bit 10 to Bit 0	VSYNP10 to VSYNP0 = 0x140
LDACLNR		LCDC AC Modulation Signal Toggle Line Number	H'A440 041E	
	ACLN4 ACLN3 ACLN2 ACLN1 ACLN0	AC Line Number Set the number of lines where the LCD current-alternating signal of the LCD module is toggled (unit: line). Must be set to (number of toggled lines) – 1 For toggling every 13 lines: ACLN = 13 – 1 = 12 = H'0C	Bit 4 to Bit 0	ACLN4 to ACLN0 = 0x000C
LDINTR	—	LCDC Interrupt Control Register Since this register is not used in this sample application, it is not set.	H'A440 0420	0

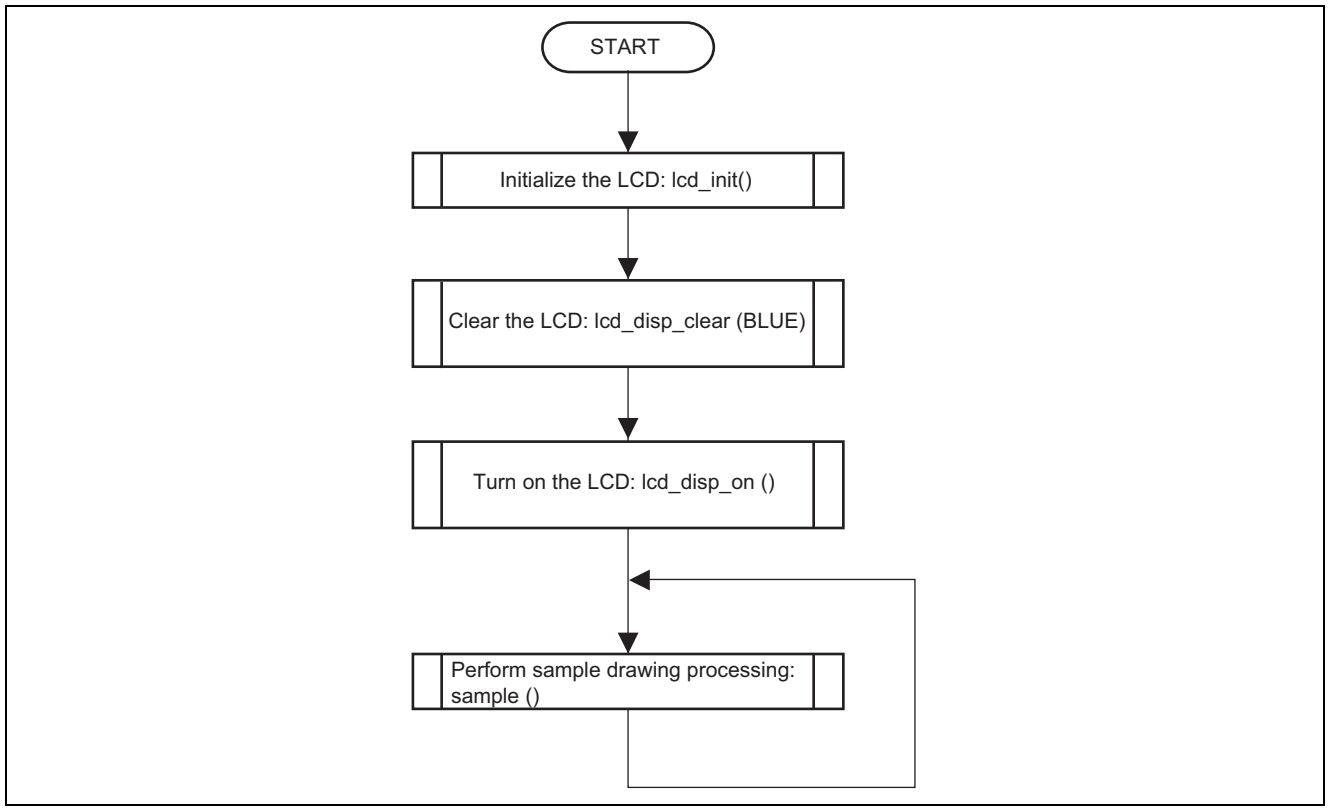
Register Name	Bit Name	Settings	Address	Setting Value
LDPMMR		LCDC Power Management Mode Register	H'A440 0424	
	ONC3 ONC2 ONC1 ONC0	LCDC Power-On Sequence Period Set the period from LCD_VEPWC assertion to LCD_DON assertion in the power-on sequence of the LCD module in frame units. Must be set to (period) – 1. This period is shown as (c) in figures 26.4 to 26.7 of the hardware manual, Power-Supply Control Sequence and States of the LCD Module. For details on setting this register, see table 26.5, Available Power-Supply Control- Sequence Periods at Typical Frame Rates. (The setting method is common for ONA, ONB, OFFD, OFFE, and OFFF.)	Bit 15 Bit 14 Bit 13 Bit 12	ONC3 = 1 ONC2 = 1 ONC1 = 1 ONC0 = 1
	OFFD3 OFFD2 OFFD1 OFFD0	LCDC Power-Off Sequence Period Set the period from LCD_DON negation to LCD_VEPWC negation in the power-off sequence of the LCD module in frame units. Must be set to (period) – 1. This period is shown as (d) in figures 26.4 to 26.7 of the hardware manual, Power-Supply Control Sequence and States of the LCD Module.	Bit 11 Bit 10 Bit 9 Bit 8	OFFD3 = 1 OFFD2 = 1 OFFD1 = 1 OFFD0 = 1
	VCPE	LCD_VCPWC Pin Enable Sets whether or not to enable a power-supply control sequence using the LCD_VCPWC pin. 1: Enabled: LCD_VCPWC pin output is asserted and negated according to the power-on or power-off sequence	Bit 6	VCPE = 1
	VEPE	LCD_VEPWC Pin Enable Sets whether or not to enable a power-supply control sequence using the LCD_VEPWC pin. 1: Enabled: LCD_VEPWC pin output is asserted and negated according to the power-on or power-off sequence	Bit 5	VEPE = 1
	DONE	LCD_DON Pin Enable Sets whether or not to enable a power-supply control sequence using the LCD_DON pin. 1: Enabled: LCD_DON pin output is asserted and negated according to the power-on or power-off sequence	Bit 4	DONE = 1
	LPS1 LPS0	LCD Module Power-Supply Input State Indicates the power-supply input state of the LCD module when using the power-supply control function. 00: LCD module power off	Bit 1 Bit 0	LPS1 = 0 LPS0 = 0

Register Name	Bit Name	Settings	Address	Setting Value
LDPSPR		LCDC Power-Supply Sequence Period Register	H'A440 0426	
	ONA3	LCDC Power-On Sequence Period	Bit 15	ONA3 = 0
	ONA2	Set the period from LCD_VCPWC assertion to starting output of the display data (LCD_DATA) and timing signals (LCD_FLM, LCD_CL1, LCD_CL2, and LCD_M_DISP) in the power-on sequence of the LCD module in frame units.	Bit 14	ONA2 = 0
	ONA1		Bit 13	ONA1 = 0
	ONA0	Must be set to (period) – 1.	Bit 12	ONA0 = 0
		This period is shown as (a) in figures 26.4 to 26.7 of the hardware manual, Power-Supply Control Sequence and States of the LCD Module.		
	ONB3	LCDC Power-On Sequence Period	Bit 11	ONB3 = 0
	ONB2	Set the period from starting output of the display data (LCD_DATA) and timing signals (LCD_FLM, LCD_CL1, LCD_CL2, and LCD_M_DISP) to the LCD_VEPWC assertion in the power-on sequence of the LCD module in frame units.	Bit 10	ONB2 = 1
	ONB1		Bit 9	ONB1 = 0
	ONB0	Must be set to (period) – 1.	Bit 8	ONB0 = 1
		This period is shown as (b) in figures 26.4 to 26.7 of the hardware manual, Power-Supply Control Sequence and States of the LCD Module.		
	OFFE3	LCDC Power-Off Sequence Period	Bit 7	OFFE3 = 0
	OFFE2	Set the period from LCD_VEPWC negation to stopping output of the display data (LCD_DATA) and timing signals (LCD_FLM, LCD_CL1, LCD_CL2, and LCD_M_DISP) in the power-off sequence of the LCD module in frame units.	Bit 6	OFFE2 = 0
	OFFE1		Bit 5	OFFE1 = 0
	OFFE0	Must be set to (period) – 1.	Bit 4	OFFE0 = 0
		This period is shown as (e) in figures 26.4 to 26.7 of the hardware manual, Power-Supply Control Sequence and States of the LCD Module.		
	OFFF3	LCDC Power-Off Sequence Period	Bit 3	OFFF3 = 0
	OFFF2	Set the period from stopping output of the display data (LCD_DATA) and timing signals (LCD_FLM, LCD_CL1, LCD_CL2, and LCD_M_DISP) to LCD_VCPWC negation to in the power-off sequence of the LCD module in frame units.	Bit 2	OFFF2 = 0
	OFFF1		Bit 1	OFFF1 = 0
	OFFF0	Must be set to (period) – 1.	Bit 0	OFFF0 = 0
		This period is shown as (f) in figures 26.4 to 26.7 of the hardware manual, Power-Supply Control Sequence and States of the LCD Module.		

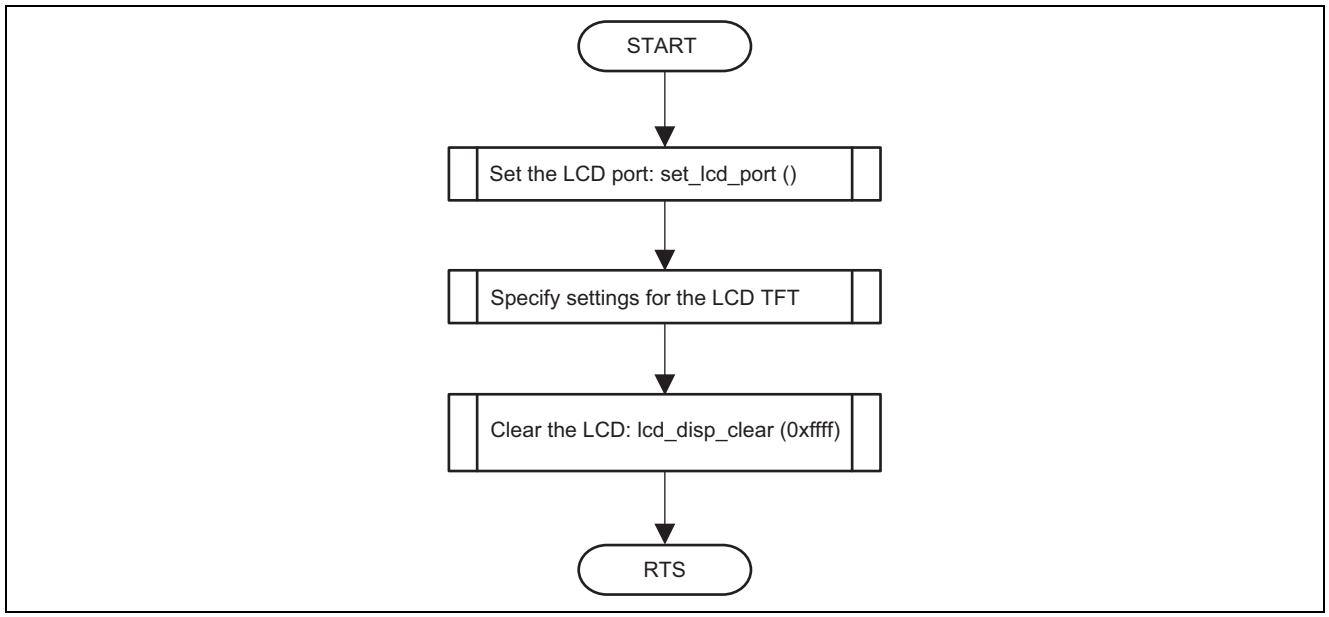
Register Name	Bit Name	Settings	Address	Setting Value
LDCNTR		LCDC Control Register	H'A440 0428	
	DON2	Display On 2 Specifies the start of the LCDC display operation. 0: LCDC is being operated or stopped 1: LCDC starts operation When this bit is read, always read as 0. Write 1 to this bit only when starting display. Do not write to this bit for other purposes.	Bit 4	—
	DON	Display On Specifies the start and stop of the LCDC display operation. The control sequence state can be checked by referencing the LPS[1:0] of LDPMMR. 0: Display-off mode: LCDC is stopped. 1: Display-on mode: LCDC operates.	Bit 0	—
LDLIRNR		LCDC Memory Access Interval Number Register	H'A440 0440	
	LIRN7 to LIRN0	VRAM Read Bus Cycle Interval Specifies the number of the CPU/DMAC/USBH bus cycles, which can be performed during burst bus cycles to read VRAM by LCDC. H'00: one bus cycle	Bit 7 to Bit 0	LIRN7 to LIRN0 = 0

5. Flowchart

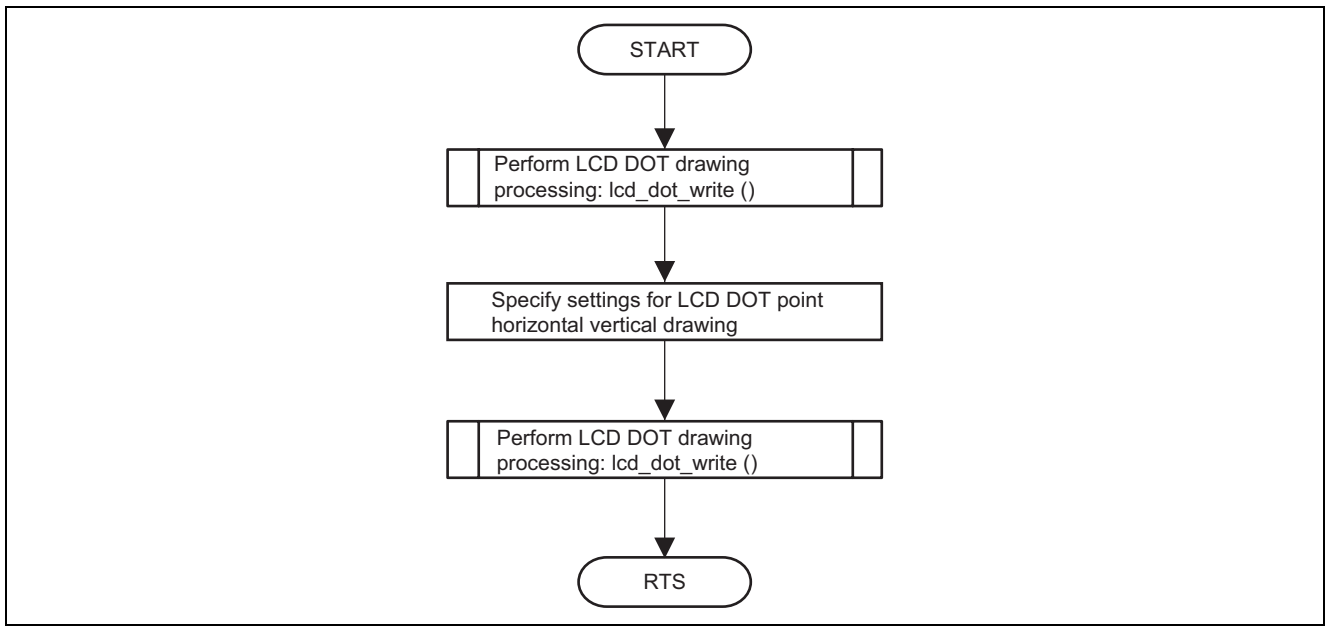
(1) **main Processing**



(2) **LCD Initialization Processing: lcd_init ()**



(3) **Sample Drawing Processing: sample3 ()**



6. Reference Program

1. Sample Program List "main.c" (1)

```
/*""FUNC
COMMENT""*************************************************************************
**********
* ID               :
* Module Overview  :  main function
*-------------------------------------------------------------------------------
-------------------
* Declaration      :  void main( void )
*-------------------------------------------------------------------------------
-------------------
* Description      :  Program that displays sample images
*                  :
*-------------------------------------------------------------------------------
-------------------
* Arguments        :  None
*-------------------------------------------------------------------------------
-------------------
* Return value     :  None
*-------------------------------------------------------------------------------
-------------------
* Notes            :
*                  :
*                  :
*""FUNC COPMMENT
END""*************************************************************************
***/
void  main( void )
{
  /* ==== Initialize LCD ==== */
  lcd_init();
  /* ==== Clear LCD ==== */
  lcd_disp_clear( BLUE );
  /* ==== Turn on LCD ==== */
  lcd_disp_on();  while( 1 )
  {
   /* ==== Sample drawing processing ==== */
   sample3();
  }
}
```

2. Sample Program List "main.c" (2)

```
/*""FUNC
COMMENT""*************************************************************************
**********
* ID               :
* Module Overview  :  sample3 function
*-------------------------------------------------------------------------------
-------------------
* Declaration      :  void sample3(void)
*-------------------------------------------------------------------------------
-------------------
* Description      :  Program that creates images by using the dot function.
*                  :
*-------------------------------------------------------------------------------
-------------------
* Arguments        :  None
*-------------------------------------------------------------------------------
-------------------
* Return value     :  None
*-------------------------------------------------------------------------------
-------------------
* Notes            :
*                  :
*                  :
*""FUNC COPMMENT
END""*************************************************************************
***/
void  sample3( void )
{
  LCD_DOT   dot;
  LCD_RECT  rect;
  int       i, ix, iy, dx, dy;
  int       Rx_size, Ry_size, color;
  color   = 0;
  dx      = 60;
  dy      = 80;
  ix      = /*(XMAX - Rx_size) / 2*/200;
  iy      = /*(YMAX - Ry_size) / 2*/280;

  /* ==== Specify the start point of dots ==== */
  dot.point.p_x = 0;
  dot.point.p_y = 0;
  dot.Color       = Color_Tbl[color];
  lcd_dot_write( dot );
  /* ==== Fill the image every x start point in 7 colors ==== */
  for( dot.point.p_x = 0;  dot.point.p_x  < XMAX ; dot.point.p_x ++  )
  {
   if( color == 7){
      color = 0;
   }
   else{
      color++;
   }
```

```
        /* ==== Set the dot color table ==== */
     dot.Color       = Color_Tbl[color];

     /* ==== Setting for dot display ==== */
     lcd_dot_write( dot );
     for( dot.point.p_y = 0;  dot.point.p_y  < YMAX ; dot.point.p_y ++ )
     {
        /* ==== Setting for dot display ==== */
        lcd_dot_write( dot );
     }
   }
   /* ==== Fill the image every y start point in 7 colors ==== */
   for( dot.point.p_y = 0;  dot.point.p_y  < YMAX ; dot.point.p_y ++  )
   {
     if( color == 7){
        color = 0;
     }
     else{
        color++;
     }
        /* ==== Set the dot color table ==== */
     dot.Color       = Color_Tbl[color];
     /* ==== Setting for dot display ==== */
     lcd_dot_write( dot );
     for( dot.point.p_x = 0;  dot.point.p_x  < YMAX ; dot.point.p_x ++ )
     {
        /* ==== Setting for dot display ==== */
        lcd_dot_write( dot );
     }
   }
   color = 0;
   dot.Color       = Color_Tbl[color];
   for( dot.point.p_x = dx;  dot.point.p_x  < (dx*3) ; dot.point.p_x ++  )
   {
     lcd_dot_write( dot );
     for( dot.point.p_y = dy;  dot.point.p_y  < (dy*3) ; dot.point.p_y ++ )
     {
        lcd_dot_write( dot );
     }
   }

}
```

3. Sample Program List "lcd.c" (1)

```
/*""FUNC
COMMENT""*************************************************************************
**********
* ID               :
* Module Overview  :  lcd_init function
*-------------------------------------------------------------------------------
-------------------
* Declaration      :  void lcd_init( void )
*-------------------------------------------------------------------------------
-------------------
* Description      :  Program that initializes the LCD.
*                  :
*-------------------------------------------------------------------------------
-------------------
* Arguments        :  None
*-------------------------------------------------------------------------------
-------------------
* Return value     :  None
*-------------------------------------------------------------------------------
-------------------
* Notes            :
*                  :
*                  :
*""FUNC COPMMENT
END""*************************************************************************
***/
void  lcd_init( void )
{
  set_lcd_port();

  REG_LDCNTR  = 0x0000;     /* disp Off */
  //TFT 240x320
  REG_LDICKR  = 0x000C;     /* input CKIO, CKIO/12 = 5.5MHz */
  REG_LDMTR   = 0xC02B;     /* TFT 16bit data bus */
REG_LDDFR   = 0x002D;       /* data 16bpp(RGB: 5-6-5) */
  REG_LDSMR   = 0x0200;     /* rotate disable, 16burst */
  REG_LDSARU  = VRAM_ST_ADDR & 0x03FFFFF0;
  REG_LDSARL  = VRAM_ST_ADDR & 0x03FFFFF0;    /* if TFT or STN, not use */
  REG_LDLAOR  = 0x0200;     /* X 256*2 byte */
  REG_LDPALCR = 0x0000;
  REG_LDHCNR  = 0x1D27;
  REG_LDHSYNR = 0x0022;
  REG_LDVDLNR = 0x013F;
  REG_LDVTLNR = 0x0143;
  REG_LDVSYNR = 0x7140;
  REG_LDACLNR = 0x000C;
  REG_LDINTR  = 0x0000;     /* Vsync Interrupt disable */
  REG_LDPMMR  = 0xFF70;
  REG_LDPSPR  = 0x0500;
  REG_LDLIRNR = 0x0000;
```

```
  lcd_disp_clear(0xffff);
}
```

4. Sample Program List "lcd.c" (2)

```
/*""FUNC
COMMENT""*************************************************************************
**********
* ID               :
* Module Overview  :  lcd_dot_write function
*-------------------------------------------------------------------------------
--------------------
* Declaration      :  void lcd_dot_write( LCD_DOT data )
*-------------------------------------------------------------------------------
--------------------
* Description      :  Program that displays dotted images.
*                  :
*-------------------------------------------------------------------------------
--------------------
* Arguments        :  None
*-------------------------------------------------------------------------------
--------------------
* Return value     :  None
*-------------------------------------------------------------------------------
--------------------
* Notes            :
*                  :
*                  :
*""FUNC COPMMENT
END""*************************************************************************
***/
void  lcd_dot_write( LCD_DOT data )
{
  unsigned short   *dot_ptr;
   /* ==== Dot color drawing processing ==== */
  dot_ptr = (unsigned short *)(VRAM_ST_ADDR + (data.point.p_y *
ONE_LINE_OFFSET) + (data.point.p_x * 2));
  *dot_ptr = data.Color;
}
```

5. Sample Program List "lcd.c" (3)

```
/*""FUNC
COMMENT""*************************************************************************
**********
* ID               :
* Module Overview  :  lcd_disp_clear function
*-------------------------------------------------------------------------------
--------------------
* Declaration      :  void lcd_disp_clear( short color )
*-------------------------------------------------------------------------------
--------------------
* Description      :  Program that clears the LCD.
*                  :
*-------------------------------------------------------------------------------
--------------------
* Arguments        :  short color
*-------------------------------------------------------------------------------
--------------------
* Return value     :  None
*-------------------------------------------------------------------------------
--------------------
* Notes            :
*                  :
*                  :
*""FUNC COPMMENT
END""*************************************************************************
***/
void  lcd_disp_clear( short color )
{
  long x, y;
  long save_addr = VRAM_ST_ADDR;
  short   *ptr = (short *)VRAM_ST_ADDR;

  for( y = 0 ;  y < YMAX ;  y++ )
  {
    for( x = 0 ;  x < XMAX ;  x++ )
    {
       *ptr++ = color;
    }
    save_addr += ONE_LINE_OFFSET;
    ptr = (short *)save_addr;
  }

}
```

6. Sample Program List "lcd.c" (4)

```
/*""FUNC
COMMENT""*************************************************************************
**********
* ID               :
* Module Overview  :  lcd_disp_on function
*-------------------------------------------------------------------------------
--------------------
* Declaration      :  void lcd_disp_on( void )
*-------------------------------------------------------------------------------
--------------------
* Description      :  Program that turns on the LCD front light.
*                  :
*-------------------------------------------------------------------------------
--------------------
* Arguments        :  None
*-------------------------------------------------------------------------------
--------------------
* Return value     :  None
*-------------------------------------------------------------------------------
--------------------
* Notes            :
*                  :
*                  :
*""FUNC COPMMENT
END""*************************************************************************
***/
void  lcd_disp_on( void )
{
  char data;

  /* Front Light On   */
  REG_LDCNTR  = 0x0011;
}
```

7. Sample Program List "back_fmtool_r0k57720.hdc"

```
/*""FUNC
COMMENT""*************************************************************************
**********
* File             :  back_fmtool_r0k57720.hdc
* Module Overview  :  Bus controller setting
*-------------------------------------------------------------------------------
--------------------
* Declaration      :  None *-----------------------------------------------------
-------------------------------------------
* Description      :  File for automatically activating the bus controller
*                  :
*-------------------------------------------------------------------------------
--------------------
* Arguments        :  None
*-------------------------------------------------------------------------------
--------------------
* Return value     :  None
*-------------------------------------------------------------------------------
--------------------
* Notes            :
*                  :
*                  :
*""FUNC COPMMENT
END""*************************************************************************
***/
! CS3BCR set Type =SDRAM,BSZ = 16bit   Settings for area 3
MF A4FD000C A4FD000F 36DB4600 LONG
! CS3WCR set WTRP=1/WTRCD=2/A3CL=2/TRWL=2/WTRC=5   Wait cycle setting
MF A4FD002C A4FD002F 00006D1B LONG
! SDCR set RFSH=1: Refresh/RMODE=0: Autorefresh/   SDRAM control register
!          BACTV=0; AutoPrecharge/A3ROW=12bit/
!          A3COL=9bit
MF A4FD0044 A4FD0047 00000011 LONG
! RTCSR set Initialization sequence start   Refresh timer control register
!           Clock select B-phy/16 = 240nsec
!           Refresh count : Once
MF A4FD0048 A4FD004B A55A0010 LONG
! RTCOR set 64(0x41)cycles per refresh   Refresh time constant register
MF A4FD0050 A4FD0053 A55A001F LONG
SLEEP D'200
! Written in SDRAM Mode Register CL=2 Burstlength=1
MF A4FD5440 A4FD5441 0000 WORD
!Cache set   Cache set
MF A40000B0 A40000B3 00000001 LONG
file_load Elf/Dwarf2 sh7720lcd.abs R
RS PC main
RS R15 D0000000
```

7. Documents for Reference

- Software Manual
  SH-3-DSP, Software Manual
  (The most up-to-date version of this document is available on the Renesas Technology Website.)
- Hardware Manual
  SH7720 Group Hardware Manual
  (The most up-to-date version of this document is available on the Renesas Technology Website.)
- Other Documents
  SH7720 Solution Engine (MS7720PR02) User's Manual
  SH7720 E10A Emulater User's Manual
  (The most up-to-date version of this document is available on the Renesas Technology Website.)

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