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SH7206 Group

Example of Setting the CPG to Enter Software Standby Mode

Introduction

This application note presents an example of configuration to enter and exit software standby mode to demonstrate the usage of the SH7206 's clock pulse generator (CPG).

Target Device

SH7206

Contents

1. Overview

1.1 Specifications

- The main program places the SH7206 in software standby mode.
- The watchdog timer (WDT) is used to count the clock oscillation settling time when canceling software standby mode.
- The SH7206 leaves software standby mode on the falling edge of the NMI interrupt signal.

1.2 MCU Functions Used

- Clock pulse generator (CPG)
- Watchdog timer (WDT)
- NMI interrupt

1.3 Conditions for Application

- MCU: SH7206 (R5S72060)
- Operating frequency: Internal clock: 200 MHz
  Bus clock: 66.67 MHz
  Peripheral clock: 33.33 MHz
- C compiler: SuperH RISC engine Family C/C++ Compiler Package: Version 9.00
  (from Renesas Technology Corp.)
- Compiler options: Default setting of HEW (-cpu=sh2a -debug -gbr=auto -global_volatile=0 -opt_range=all -infinite_loop=0 -del_vacant_loop=0 -struct_alloc=1)

1.4 Related Application Note

The operation of the sample program in this application note was confirmed with the configuration specified in the application note "Example of SH7206 Initial Configuration". Please refer to that note in combination with this one.

2. Description of Sample Application

In this sample application, software standby mode is entered and exited.

2.1 Summary of MCU Functions Used

Software standby mode is entered by executing the SLEEP instruction with the STBY bit in the standby control register (STBCR) of the clock pulse generator (CPG) is set to 1.

Software standby mode is exited by means of an interrupt (NMI or IRQ) or a reset (power-on reset or manual reset).

In the process of canceling the mode using an interrupt, the watchdog timer counter (WTCNT) of the watchdog timer starts counting up on detection of the interrupt signal. When WTCNT overflows, the CPG begins to supply clocks and the CPU resumes operation.

For details on software standby mode, see section 22, Power-Down Modes; for details on the clock pulse generator, see section 3, Clock Pulse Generator (CPG); for details on interrupts, see section 5, Interrupt Controller (INTC); and for details on the watchdog timer, see section 14, Watchdog Timer (WDT), in the SH7206 Group Hardware Manual.

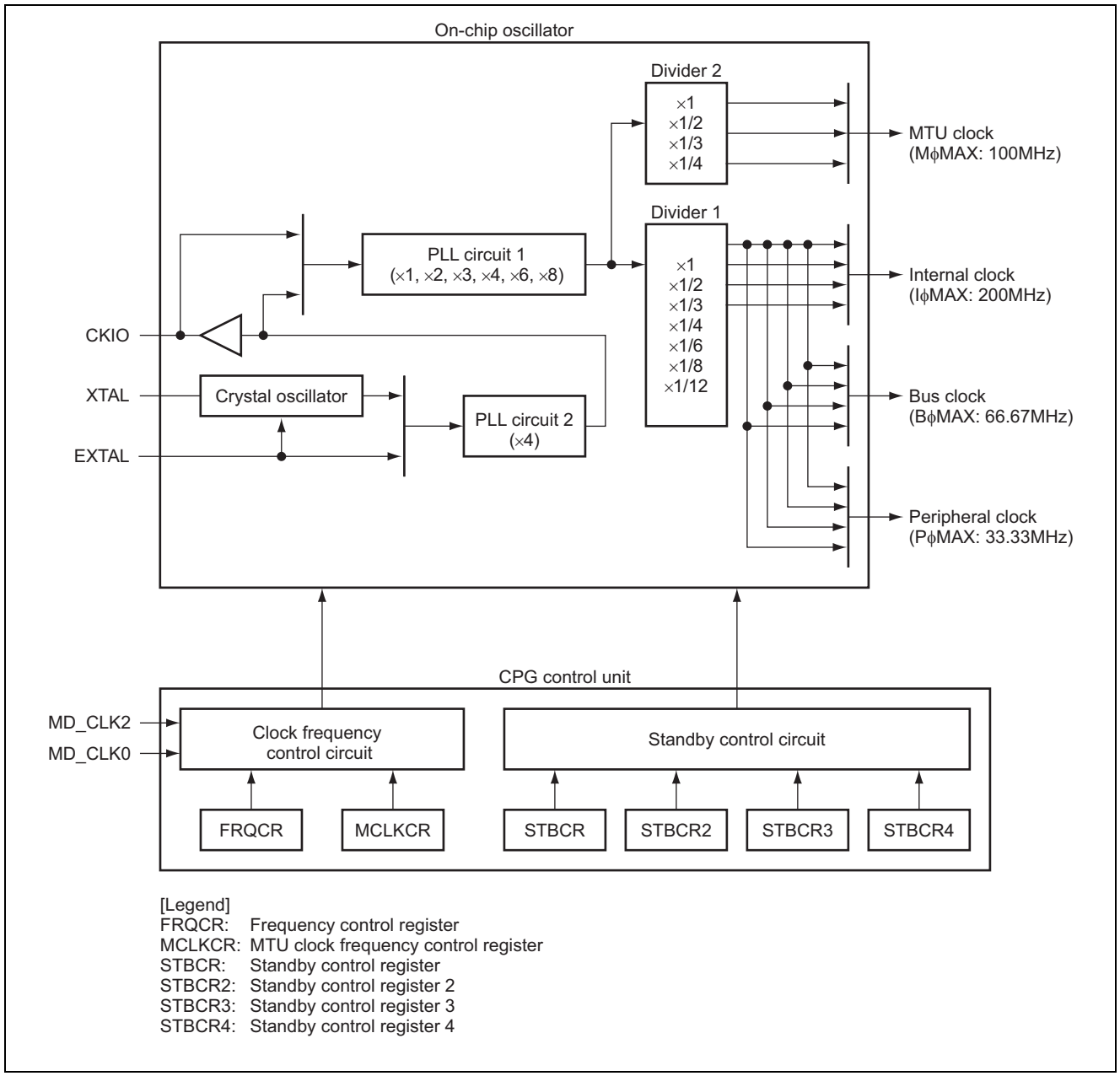
Tables 1 and 2 summarize the features of the CPG and WDT. Figures 1and 2 are schematic views of the CPG and WDT.

Table 1 Summary of CPG

Item	Function
Clock operating mode	2 (modes 2 and 7)
Generated clock signals	Internal clock (Iϕ): For the CPU and cache Peripheral clock (Pϕ): For the on-chip peripheral modules Bus clock (Bϕ): For the external bus interface MTU clock (Mϕ): For the MTU2S module
Frequency changing function	Internal and peripheral clock frequencies can be changed independently by configuring the PLL circuits and divider circuits in the CPG.
Power-down mode control	The clock supply can be stopped in sleep mode and software standby mode, and specific modules can be stopped using the module standby function.

Table 2 Summary of WDT

Item	Function
Number of available channels	1
Counter	8-bit counter (up-counter only)
Timer mode	Watchdog timer mode or interval timer mode
Pin function	WDTOVF: Outputs the counter overflow signal in watchdog timer mode.
Clock source	Pϕ, Pϕ/64, Pϕ/128, Pϕ/256, Pϕ/512, Pϕ/1024, Pϕ/4096, or Pϕ/16384 (Pϕ: On-chip peripheral clock)
Starting methods	Watchdog timer/interval timer: By software When the frequency is changed: By software When software standby mode is canceled: Detection of an interrupt



[Legend]
FRQCR: Frequency control register
MCLKCR: MTU clock frequency control register
STBCR: Standby control register
STBCR2: Standby control register 2
STBCR3: Standby control register 3
STBCR4: Standby control register 4

Figure 1 Schematic View of the CPG

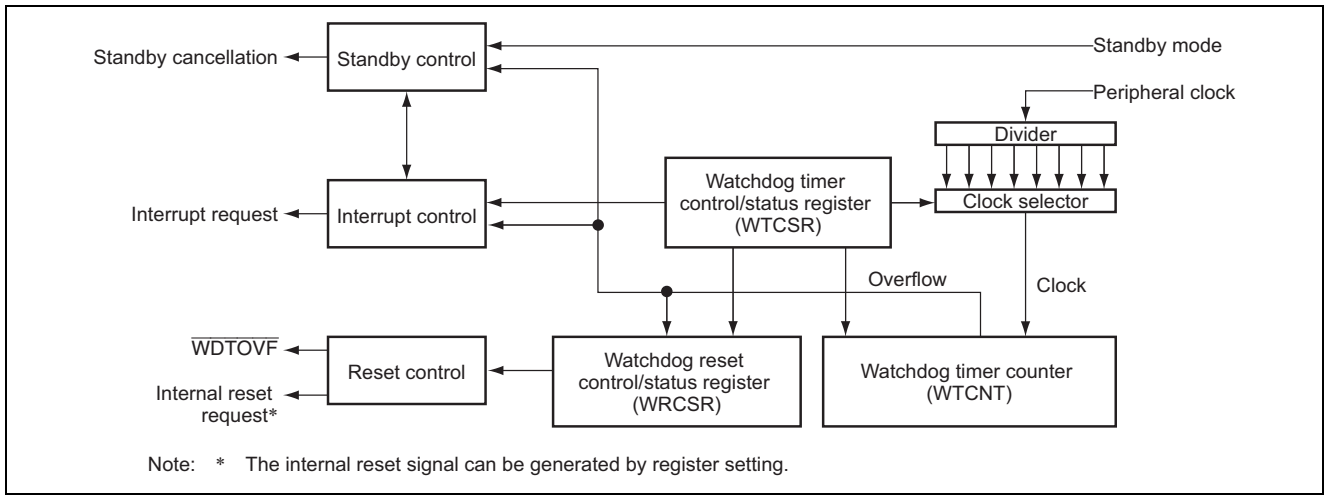


Figure 2 Schematic View of the WDT

2.2 Procedure for Setting the MCU Modules

Figure 3 shows the setting procedure for entering and exiting software standby mode. In this sample application, the NMI interrupt is used as the interrupt source for exiting standby mode.

For details on setting the individual registers, refer to the SH7206 Group Hardware Manual.

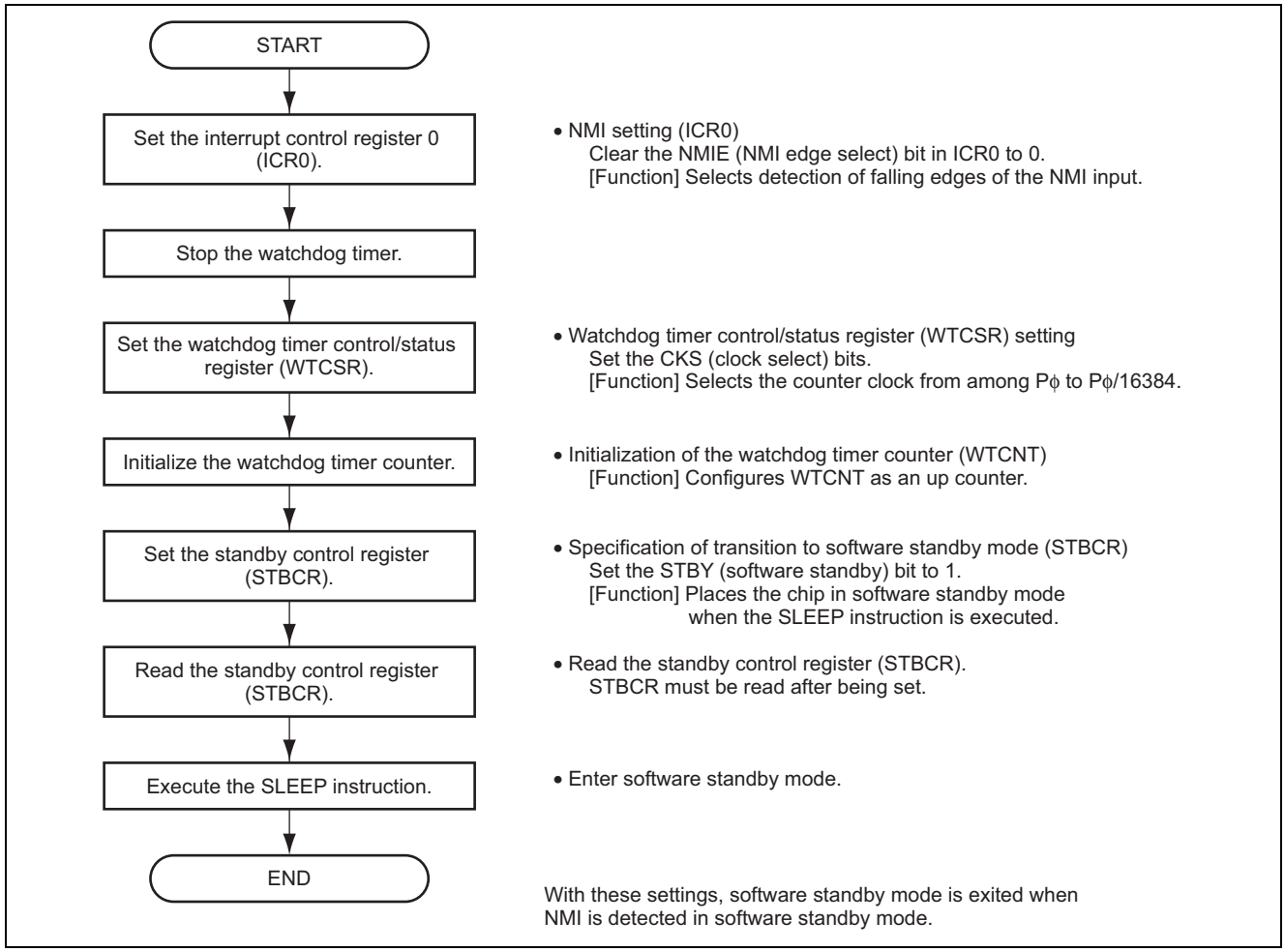


Figure 3 Setting Procedure for Entering and Exiting Software Standby Mode

2.3 Operation of Sample Program

In the sample program, the SH7206 is made to enter software standby mode by the main function. If an NMI interrupt is generated in software standby mode, the WDT is started. When the WDT overflows, the clock supply to the CPU starts and software standby mode is exited. Figure 4 shows the timing of the sample program operation.

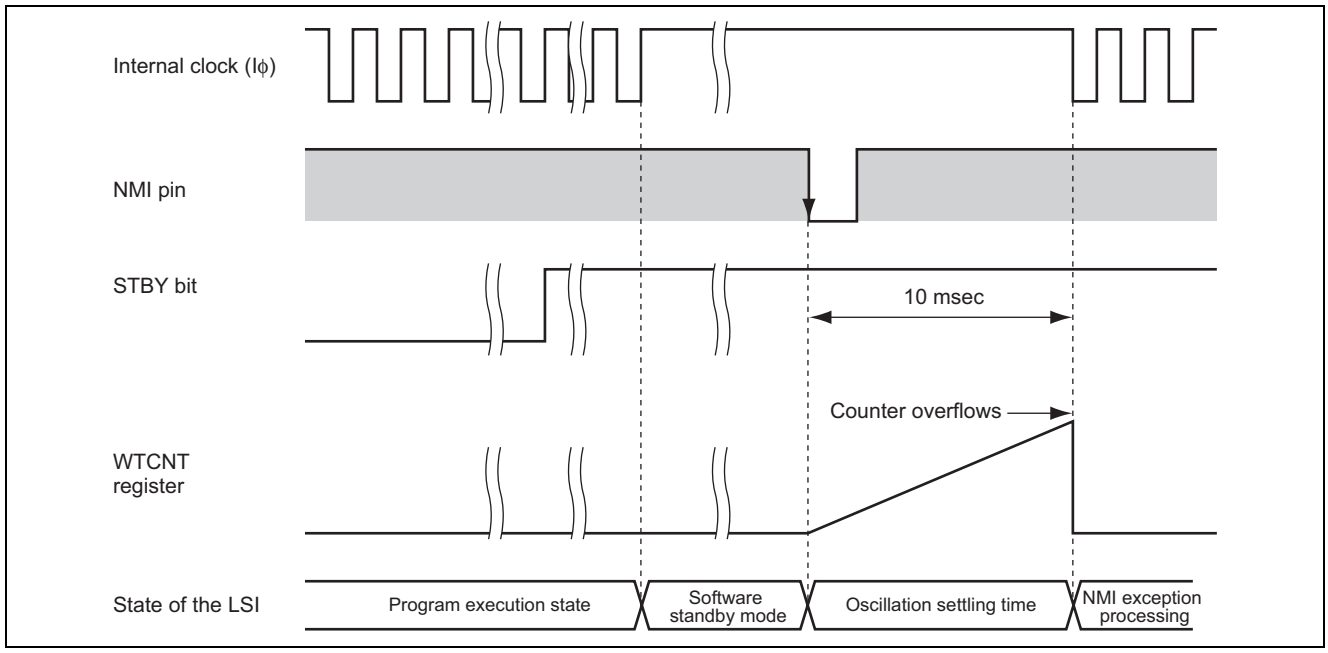


Figure 4 Timing of Sample Program Operation

2.4 Processing Sequence of Sample Program

Table 3 shows the register settings when the chip enters software standby mode. Figure 5 shows the processing flows of the sample program.

Table 3 Register Settings when Entering Software Standby Mode

Register Name	Address	Setting	Description
Watchdog timer control/ status register (WTCSR)	H'FFFE0000	H'A51E	TME = 0: The timer is disabled. CKS[2:0] = B'110: Counter clock is 1/4096 × Pϕ.
Watchdog timer counter (WTCNT)	H'FFFE0002	H'5AAD	The timer counter is initialized to H'AD.
Standby control register (STBCR)	H'FFFE0014	H'80	STBY = 1: Executing the SLEEP instruction puts the chip into software standby mode.
Interrupt control register 0 (ICR0)	H'FFFE0800	H'0000	NMIE = 0: An interrupt request is detected on the falling edge of the NMI input.

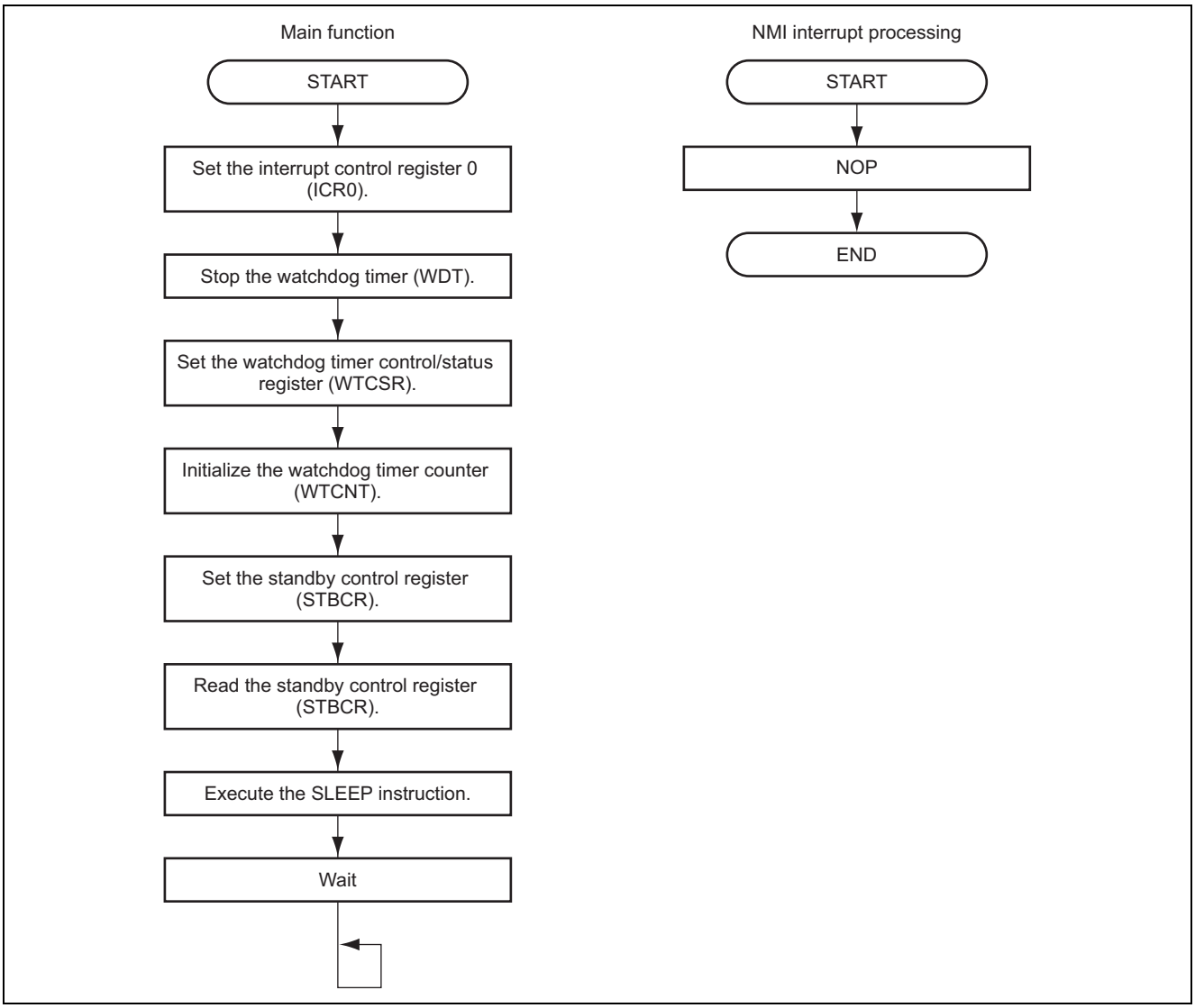


Figure 5 Flow of Processing by the Sample Program

3. Sample Program Listing

- Sample Program Listing: main.c (1)

```
 1 /*""FILE COMMENT""*************************************************************************
 2 *
 3 *   System Name: SH7206 Sample Program
 4 *   File Name  : main.c
 5 *   Contents   : Making settings for entering/exiting software standby mode (with use of WDT)
 6 *   Version    : 0.01
 7 *   Model      : M3A-HS60
 8 *   CPU        : SH7206
 9 *   Compiler   : SHC9.0.00
10 *
11 *    Note      : Sample program for entering software standby mode by executing the
12 *                SLEEP instruction, and exiting software standby mode by starting
13 *                the WDT on the falling edge of the NMI input.
14 *
15 *                <Caution>
16 *                This sample program is for reference
17 *                and its operation is not guaranteed.
18 *                Customers should use this sample program for technical reference
19 *                in software development.
20 *
21 * Copyright (C) 2004 Renesas Technology Corp. All Rights Reserved
22 * and Renesas Solutions Corp. All Rights Reserved
23 *
24 * History      :2004.09.30  ver.0.01
25 *""FILE COMMENT END""*************************************************************************/
26 #include <machine.h>                      /* machine.h is supplied with the C compiler.    */
27 #include "iodefine.h"                     /* iodefine.h is automatically created by HEW.   */
28
29 /* ==== Prototype declaration ==== */
30 void main(void);
31
```

- Sample Program Listing: main.c (2)

```
/*""FUNC COMMENT""*****************************************************************************
* ID            :
* Module summary: Main function of the sample program
*-------------------------------------------------------------------------------------------
* Include       : #include "iodefine.h"
*-------------------------------------------------------------------------------------------
* Declaration   : void main(void)
*-------------------------------------------------------------------------------------------
* Functional description:
*               : After selecting falling edge detection for the NMI signal,
*               : places the chip in software standby mode. The chip returns
*               : to normal mode by generation of an NMI interrupt.
*-------------------------------------------------------------------------------------------
* Argument      : None
*-------------------------------------------------------------------------------------------
* Return value  : None
*-------------------------------------------------------------------------------------------
* Notes         :
*""FUNC COMMENT END""*************************************************************************/
void main(void)
{
    volatile unsigned char stbcr;

    /* ---- Set interrupt control register 0 (ICR0) ---- */
    INTC.ICR0.BIT.NMIE = 0x0;           /* Select falling edge detection. */

    /* ==== Stop the watchdog timer (WDT) ==== */
    WDT.WTCSR.WORD = 0xa500;

    /* ---- Set watchdog timer control/status register (WTCSR) ---- */
     WDT.WTCSR.WORD = 0xa51e; /*
                              Set TME to 0.
                              Select the counter clock (Pphi = 33.3 MHz)
                              To write to WTCSR, H'A5 must be written to the upper byte.
                              */

    /* ---- Initialize watchdog timer counter (WTCNT) ---- */
    WDT.WTCNT.WORD = 0x5aad;  /* Counter overflows when approx 10 ms have elapsed. */

    /* ---- Set standby control register (STBCR) ---- */
    CPG.STBCR.BIT.STBY = 0x1;

    /* ---- Read standby control register (STBCR) ---- */
    stbcr = CPG.STBCR.BYTE; /* Dummy read */

    /* ---- Execute SLEEP instruction ---- */
     sleep();

    while(1){
        /* End of program */
    }
}

/* End of File */
```

- Sample Program Listing: intprg.c

```
 1 /*""FILE COMMENT""*****************************************************************************
 2 *
 3 *   System Name: SH7206 Sample Program
 4 *   File Name  : intprg.c
 5 *   Version    : 1.00.00
 6 *   Contents   : Interrupt processing function definition
 7 *   Model      : M3A-HS60
 8 *   CPU        : SH7206
 9 *   Compiler   : SHC9.0.00
10 *   OS         : none
11 *
12 *   Note       : This file was originally generated by Renesas Project Generator
13 *              : (Ver.3.1) and was modified for application note.
14 *
15 *                <Caution>
16 *                This sample program is for reference
17 *                and its operation is not guaranteed.
18 *                Customers should use this sample program for technical reference
19 *                in software development.
20 *
21 *
22 *   This file is generated by Renesas Project Generator (Ver.3.1).
23 *
24 *   Copyright (C) 2004 Renesas Technology Corp. All Rights Reserved
25 *   AND Renesas Solutions Corp. All Rights Reserved
26 *
27 *   History    : 2004.10.14 ver.1.00.00
28 *""FILE COMMENT END""*****************************************************************************/
29 #include <machine.h>
30 #include "vect.h"
31 #pragma section IntPRG
32

           Lines 33 through 42 are omitted


43 // 9 CPU Address error
44 void INT_CPU_Address(void){/* sleep(); */}
45 // 10 DMAC Address error
46 void INT_DMAC_Address(void){/* sleep(); */}
47 // 11 NMI
48 /*""FUNC COMMENT""*************************************************************************
49 * ID             :
50 * Module summary : NMI interrupt processing
51 *-------------------------------------------------------------------------------------------
52 * Include        :
53 *-------------------------------------------------------------------------------------------
54 * Declaration    : void INT_NMI(void)
55 *-------------------------------------------------------------------------------------------
56 * Functional description:
57 *                : NMI interrupt processing, which is also used when exiting
58 *                : software standby mode.
59 *-------------------------------------------------------------------------------------------
60 * Argument       : None
61 *-------------------------------------------------------------------------------------------
62 * Return value   : None
63 *-------------------------------------------------------------------------------------------
64 * Notes          :
65 *""FUNC COMMENT END""*********************************************************************/
66 void INT_NMI(void)
67 {
68     /* NOP */
69 }
           Line 70 and the subsequent lines are omitted.
```

4. Reference Documents

- SH-2A SH2A-FPU Software Manual (Rev.3.00)
  (Download the latest edition from the website of Renesas Technology Corp.)
- SH7206 Group Hardware Manual (Rev. 1.00)
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Rev.	Date	Page	Summary
1.00	Sep.14.05	—	First edition issued

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