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SH7206 Group

Example of Program Transfer to On-Chip RAM Using the DMAC

Introduction

This application note describes an example of transferring a program stored in an external ROM to the on-chip RAM of the SH7206.

Target Device

SH7206

Contents

1. Overview

1.1 Specifications

- The direct memory access controller (DMAC) is activated to transfer a program in an external ROM to the on-chip RAM, and the program in the on-chip RAM is executed.

1.2 MCU Functions Used

- Direct memory access controller (DMAC channel 0)

1.3 Conditions for Application

- MCU: SH7206 (R5S72060)
- Operating frequency: Internal clock: 200 MHz
  Bus clock: 66.67 MHz
  Peripheral clock: 33.33 MHz
- C compiler: SuperH RISC Engine Family C/C++ Compiler Package: version 9.00
  (from Renesas Technology Corp.)
- Compiler options: Default setting of HEW (-cpu = sh2a -debug –gbr = auto -global_volatile = 0
  -opt_range = all -infinite_loop = 0 -del_vacant_loop = 0
  -struct_alloc = 1)

1.4 Related Application Notes

- The operation of the sample program in this application note was confirmed with the configuration specified in the application note "Example of SH7206 Initial Configuration". Please refer to that note in combination with this one.
- Details on the DMAC are described in the SH7206 application note "Example-of Memory Transfer by the DMAC".

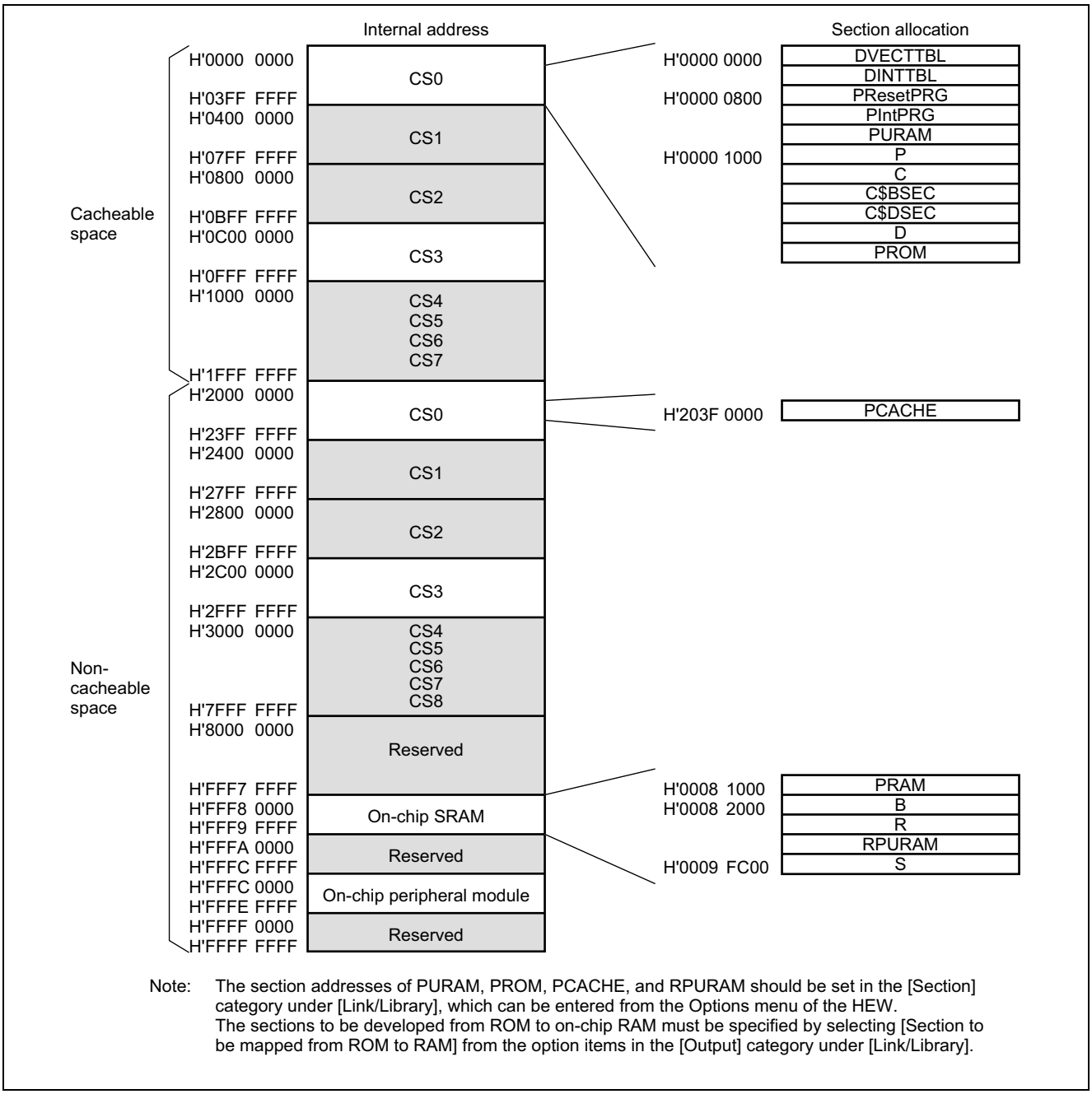
2. Description of Sample Application

This sample application applies the direct memory access controller (DMAC) to transfer of programs in an external ROM to the on-chip RAM, and executes the program in the on-chip RAM.

2.1 Section Allocation of Sample Program

The section name of the program to be transferred can be changed using "#pragma section", compiler's expanded function. In the sample program, the program section of the program to be transferred is changed to section PROM, and the program section in the on-chip RAM area to which the program is transferred will be section PRAM.

Figure 1 shows a memory map for the sample program.
Since the cache setting program must be executed in a non-cacheable space, section PCACHE is allocated in a non-cacheable space. Likewise, the program for setting AC characteristics switching must be executed in on-chip RAM, so section PURAM is allocated in the transfer source ROM area and section RPURAM is allocated in the transfer destination RAM area.



Note: The section addresses of PURAM, PROM, PCACHE, and RPURAM should be set in the [Section] category under [Link/Library], which can be entered from the Options menu of the HEW.
The sections to be developed from ROM to on-chip RAM must be specified by selecting [Section to be mapped from ROM to RAM] from the option items in the [Output] category under [Link/Library].

Figure 1 Memory Map

2.2 Setting the Linkage Editor

The section addresses are specified by options of the linkage editor. Table 1 lists the section names to be specified in the sample program. Table 2 shows linkage editor options to be used.

Table 1 Section Names to be Specified in Sample Program

Section Name	Description
PROM	Transfer source in which the program to be transferred is stored
PRAM	Transfer destination to which the program is transferred
PCACHE	A cache setting program is stored
PURAM	Transfer source of the program for setting AC characteristics switching
RPURAM	Transfer destination of the program for setting AC characteristics switching

Note: Section addresses are specified by selecting “SuperH RISC engine Standard Toolchain” from the pull-down menu in the HEW window. For details, refer to the HEW Manual.

Table 2 Linkage Editor Options

Option	Description
-rom=D=R,**PROM=PRAM**,PURAM=RPURAM	Specifies the ROM sections to be mapped to RAM.
start=DVECTTBL,DINTTBL/00,PResetPRG, PIntPRG,PURAM/0800,P,C,C$BSEC,C$DSEC,D, **PROM/1000**,**PCACHE/203F0000**, **PRAM/FFF81000**, B,R,RPURAM/FFF80000,S/FFF9FC00	Specifies the section start addresses.

2.3 Methods for Acquiring Section Addresses

Section address operators of the compiler are used to acquire section addresses by the program. Table 3 lists the section address operators.

Table 3 Address Operators

Syntax	Function
_sectop(“<section name>”)	Refers to the start address of the specified <section name>.
_secend(“<section name>”)	Refers to the end address of the specified <section name> + 1.
_secsize(“<section name>”)	Generates the size of the specified <section name>.

2.4 Operation of Sample Program

In the sample program, the direct memory access controller (DMAC) is placed in auto request mode, and data equal to the size of section PROM are transferred from the start address of section PROM in the CS0 space to section PRAM allocated in the on-chip RAM. For confirmation of the operation, function cmt0, which uses the compare-match timer, is placed in section PROM and is transferred to the on-chip RAM. After the transfer has been completed, function cmt0 is executed.

2.5 Notes when Changing to Transfer by the CPU

If a program is transferred to cacheable space by the CPU (the transfer is by software) while the operand cache (write-back mode) is enabled, the transferred program is taken into the operand cache and instruction fetches may not succeed. When a program is transferred by the CPU, the program should be transferred to a non-cacheable space, or write-back of the operand cache should be performed.

Since the sample program uses the DMAC to transfer a program, transfer is not affected by the state of the operand cache.

2.6 Register Settings and Processing Sequence of Sample Program

The register settings of the sample program are shown in table 4, and processing flow of the sample program is shown in figure 2.

Table 4 Register Settings in the Sample Program

Register Name	Address	Setting	Description
Standby control register 2 (STBCR2)	H'FFFE0018	H'00	MSTP8 = 0: The DMAC runs.
DMA channel control register_0 (CHCR_0)	H'FFFE100C	H'00000000	Before initial setting for DMA is made, DE = 0: DMA transfer is disabled.
		H'00005428	DMA initial setting TC = 1: Transfer by the number of times set in DMATCR in response to a DMA request. DM = B'01: Destination address is incremented. SM = B'01: Source address is incremented. RS = B'0100: Auto request TB = 1: Burst mode TS = B'01: Word transfer DE = 0: DMA transfer is disabled.
		H'80005429	When enabling DMA transfer, DE = 1: DMA transfer is enabled.
DMA source address register_0 (SAR_0)	H'FFFE1000	—	Transfer source address: Start address of section PROM
DMA destination address register_0 (DAR_0)	H'FFFE1004	—	Transfer destination address: Start address of section PRAM
DMA transfer count register_0 (DMATCR_0)	H'FFFE1008	—	Number of DMA transfers: Half the size of section PROM
DMA operation register (DMAOR)	H'FFFE1200	H'00000001	DME = 1: DMA transfer is enabled on all channels.

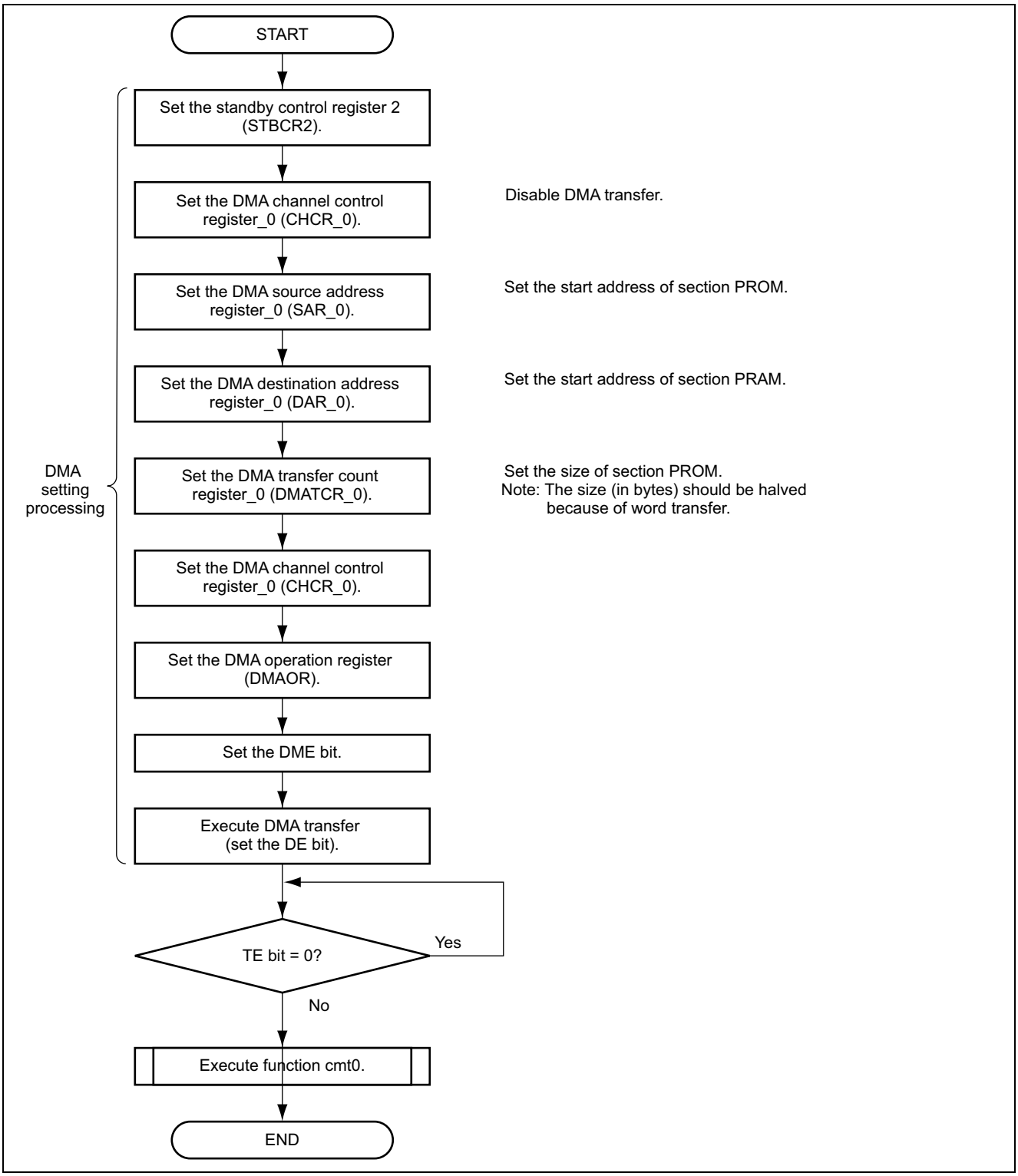


Figure 2 Processing Flow of the Sample Program

3. Sample Program Listing

1. Sample Program Listing: main.c (1)

```
/*""FILE COMMENT""*******************************************************************************
*
*   System Name : SH7206 Sample Program
*   File Name   : main.c
*   Contents    : Transferring a program section from ROM to on-chip RAM
*   Version     : 1.00.00
*   Model       : M3A-HS60
*   CPU         : SH7206
*   Compiler    : SHC9.0.00
*
*   Note        : Sample program for transferring the specified program section
*               : from external memory (ROM) to on-chip SRAM by the DMAC and
*               " executing the transferred program
*
*                <Caution>
*                This sample program is for reference
*                and its operation is not guaranteed.
*                Customers should use this sample program for technical reference
*                in software development.
*
*    Copyright (C) 2004 Renesas Technology Corp. All Rights Reserved
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*
*    history     : 2004.10.28 ver.1.00.00
*""FILE COMMENT END""*************************************************************************/
#include <machine.h>
#include "iodefine.h"                   /* iodefine.h is automatically created by HEW    */

/* ==== Prototype declarations ==== */
void main(void);
void cmt0(void);
void io_init_cmt0(void);

```

2. Sample Program Listing: main.c (2)

```
/*""FUNC COMMENT""*****************************************************************************
* ID            :
* Module summary: Main function of the sample program (program transfer from ROM to RAM)
*-----------------------------------------------------------------------------------------------
* Include       : #include "iodefine.h"
*-----------------------------------------------------------------------------------------------
* Declaration   : void main(void)
*-----------------------------------------------------------------------------------------------
* Functional description: Section PROM is transferred to section PRAM
*               : allocated in on-chip SRAM by the DMAC, and the transferred
*               : program (function cmt0) is executed.
*-----------------------------------------------------------------------------------------------
* Argument      : None
*-----------------------------------------------------------------------------------------------
* Return value  : None
*-----------------------------------------------------------------------------------------------
* Notes         : Section PROM and section PRAM as the transfer destination must be
*               : added to the section definitions of the optimizing linkage editor,
*               : and [Section to be mapped from ROM to RAM] must be specified.
*""FUNC COMMENT END""*************************************************************************/
void main(void)
{
    /* ==== Setting standby control register 2 (STBCR2) ==== */
    CPG.STBCR2.BIT.MSTP8 = 0x0;             /* Cancel DMAC module stop mode               */

    /* ---- Setting DMA channel control register (CHCR_0) ---- */
    DMAC.CHCR0.BIT.DE = 0x0ul;              /* Disable DMA transfer                       */

    /* ==== Setting DMA source address register_0 (SAR_0) ==== */
    DMAC.SAR0.LONG = (unsigned long)__sectop("PROM");
                                            /* Refer to the start address of section PROM */
    /* ==== Setting DMA destination address register_0 (DAR_0) ==== */
    DMAC.DAR0.LONG = (unsigned long)__sectop("PRAM");
                                            /* Refer to the start address of section PRAM */
    /* ==== Setting DMA transfer count register_0 (DMATCR_0) ==== */
    DMAC.DMATCR0.LONG = __secsize("PROM")/2;

    /* ==== Setting DMA channel control register_0 (CHCR_0) ==== */
    DMAC.CHCR0.LONG |= 0x80005428ul;
        /*
            bit31   : TC: 1-------------- Transfer by the number of times specified in DMATCR
            bit30-29: reserved 0
            bit28   : RLD OFF : 0-------------------- Disable reload function
            bit27-24: reserved 0
            bit23   : DO over run0 : 0--------------- Unused
            bit22   : TL TEND low active : 0--------- Unused
            bit21-20: reserved 0
            bit19   : HE :0-------------------------- Unused
            bit18   : HIE :0------------------------- Unused
            bit17   : AM :0-------------------------- Unused
            bit16   : AL :0-------------------------- Unused
            bit15-14: DM1:0 DM0:1-------------------- Increment destination address
            bit13-12: SM1:0 SM0:1-------------------- Increment source address
            bit11-8 : RS : auto request : B'0100----- Auto request
            bit7    : DL : DREQ level : 0 ----------- Unused
            bit6    : DS : DREQ select :0 Low level-- Unused
            bit5    : TB : cycle :1------------------ Burst mode
            bit4-3  : TS : transfer size: B'01------- Word transfer
            bit2    : IE : interrupt enable: 0------- Disable interrupt
            bit1    : TE : transfer end : 0---------- Clear the TE flag
            bit0    : DE : DMA enable bit: 0--------- Disable DMA transfer
        */

```

3. Sample Program Listing: main.c (3)

```
 97      /* ==== Setting DMA operation register (DMAOR) ==== */
 98      DMAC.DMAOR.WORD &= 0x0000u;
 99          /*
100             bit15-14 : reserved 0
101             bit13-12 : CMS1:0 CMS0:0------------------ Normal mode
102             bit11-10 : reserved 0
103             bit9-8   : PR1:0 PR0:0 ------------------- Fixed mode 1
104             bit7-3   : reserved 0
105             bit2     : AE: 0 ------------------------- Clear the address error flag
106             bit1     : NMIF: 0 ----------------------- Clear the NMI flag
107             bit0     : DME:0 ------------------------- Disable DMA transfer on all channels
108          */
109
110     /* ==== Setting DME bit ==== */
111     DMAC.DMAOR.BIT.DME = 1ul;
112
113     /* ==== Executing DMA transfer (setting DE bit) ==== */
114     DMAC.CHCR0.BIT.DE = 1ul;
115
116     /* ==== TE bit = "0"?==== */
117     while(DMAC.CHCR0.BIT.TE == 0ul){
118         /* ==== Wait for completion of DMA transfer ==== */
119     }
120
121     /* ==== Executing function CMT0 ==== */
122     cmt0();                                  /* Port E1 inversion processing          */
123 }
124
125
```

4. Sample Program Listing: main.c (4)

```
126  #pragma section ROM             /* P section from here is defined as section PROM */
127
128  /*""FUNC COMMENT""*****************************************************************************
129  * ID            :
130  * Module summary: Counting at a constant cycle
131  *-----------------------------------------------------------------------------------------------
132  * Include       : #include "iodefine.h"
133  *-----------------------------------------------------------------------------------------------
134  * Declaration   : void cmt0(void)
135  *-----------------------------------------------------------------------------------------------
136  * Functional description: Initializes (1 ms) IO port PE1 (connected to an LED) and
137  *               : compare-match timer CMT0, and turns on or off the LED connected
138  *               : to PE1 every thousandth setting of 1-ms flag (interrupt request bit).
139  *-----------------------------------------------------------------------------------------------
140  * Argument      : None
141  *-----------------------------------------------------------------------------------------------
142  * Return value  : None
143  *-----------------------------------------------------------------------------------------------
144  * Notes         : This module is placed in section PROM so that it is transferred.
145  *               : Section PROM and section PRAM as the transfer destination must
146  *               : be added to the section definitions of the optimizing linkage editor,
147  *               : and [Section to be mapped from ROM to RAM] must be specified.
148  *""FUNC COMMENT END""*************************************************************************/
149  void cmt0(void)
150  {
151      volatile unsigned int CountCMT0;   /* For one-second software counter */
152
153      /* ==== Port E initialization ==== */
154      PORT.PECRL1.WORD = 0x0000;         /* Set the pin as PE1 */
155      PORT.PEIORL.WORD = 0x0002;         /* Set PE1 as an output pin */
156      PORT.PEDRL.WORD  = 0x0002;         /* Write output value of 1 to port E data register */
157
158      /* ==== One-second software counter (CountCMT0) initialization ==== */
159      CountCMT0 = 1000u;                 /* Count 1000 times */
160
161      /* ==== CMT0 (1-ms constant cycle timer) initialization processing ==== */
162      io_init_cmt0();
163
164      while(1){
165          /* ---- Checking compare match (1ms) flag ---- */
166          while (CMT.CMCSR0.BIT.CMF == 0){
167              /* Wait until 1 ms elapses */
168          }
169
170          CMT.CMCSR0.BIT.CMF = 0;        /* Clear the compare match flag (CMF) to 0         */
171          CountCMT0--;                   /* Update one-second software counter (CountCMT0)  */
172
173          /* ---- Checking one-second software counter ---- */
174          if(CountCMT0 == 0u){
175              CountCMT0 = 1000u;         /* Re-initialize the one-second software counter   */
176              PORT.PEDRL.BIT.PE1DR ^= 1u ; /* Port E1 output inversion processing           */
177          }
178      }
179  }
180
181
```

5. Sample Program Listing: main.c (5)

```
/*""FUNC COMMENT""*****************************************************************************
* ID            :
* Module summary: Configuring CMT0 as a periodic timer
*-----------------------------------------------------------------------------------------------
* Include       : #include "iodefine.h"
*-----------------------------------------------------------------------------------------------
* Declaration   : void io_init_cmt0(void)
*-----------------------------------------------------------------------------------------------
* Functional description: Sets CMT0 so that the CMF flag is set every 1 ms.
*-----------------------------------------------------------------------------------------------
* Argument      : None
*-----------------------------------------------------------------------------------------------
* Return value  : None
*-----------------------------------------------------------------------------------------------
* Notes         : This module is placed in section PROM so that it is transferred.
*               : In the section definitions of the optimizing linkage editor, section
*               : PROM and transfer destination section PRAM must be added along with
*               : specification as "Section to be mapped from ROM to RAM".
*""FUNC COMMENT END""*************************************************************************/
void io_init_cmt0(void)
{
    /* ==== Initial settings for periodic (1 ms) timer ==== */
    /* ---- Setting standby control register 4 (STBCR4) ---- */
    CPG.STBCR4.BIT.MSTP42 = 0x0;            /* Cancel CMT module stop mode              */

    /* ---- Setting compare match timer start register (CMSTR) ---- */
    CMT.CMSTR.WORD = 0x0000;                /* Stop channel 0 counter                   */

    /* ---- Setting compare match timer control/status register (CMCSR0) ---- */
    CMT.CMCSR0.WORD = 0x0002;               /* Disable compare match interrupt,         */
                                            /*          and set 1/128 peripheral clock  */
    /* ---- Setting compare match timer counter register (CMCNT0) ---- */
    CMT.CMCNT0.WORD = 0x0000;               /* Clear timer counter                      */

    /* ---- Setting compare match timer constant register (CMCOR0) ---- */
    CMT.CMCOR0.WORD = 0x0104;               /* Set the period until compare match (1 ms) */

    /* ---- Setting compare match timer start register (CMSTR) ---- */
    CMT.CMSTR.BIT.STR = 0x1;                /* Start counting                           */
}
/* End of File */
```

4. Reference Documents

- SH-2A SH2A-FPU Software Manual (Rev.3.00)
  (Download the latest edition from the website of Renesas Technology Corp.)
- SH7206 Group Hardware Manual (Rev. 1.00)
  (Download the latest edition from the website of Renesas Technology Corp.)

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Rev.	Date	Page	Summary
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