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SH7137 Group

Example of Initialization

Summary

This application note gives an example of configuration items to activate the SH7137 Microcomputers (MCUs).

Target Device

SH7137 MCU

Contents

1. Introduction

1.1 Specifications

Configure the clock pulse generator (CPG) after the reset is canceled.

1.2 Modules Used

- Clock pulse generator (CPG)

1.3 Applicable Conditions

MCU	SH7137
Operating Frequency	Internal clock: 80 MHz Bus clock: 40 MHz Peripheral clock: 40 MHz
Integrated Development Environment	Renesas Technology Corp. High-performance Embedded Workshop Ver.4.03.00
C compiler	Renesas Technology SuperH RISC engine Family C/C++ compiler package Ver.9.01 Release 01
Compiler options	Default setting in the High-performance Embedded Workshop (-cpu=sh2 -debug -gbr=auto -global_volatile=0 -opt_range=all -infinite_loop=0 -del_vacant_loop=0 -struct_alloc=1)

2. Applications

Configuration program for the minimum hardware setup is required to execute the main function created in C code. This application note describes the configuration example for the configuration program.

All of the SH7137 application notes assume to use the sample program described in this application note as the configuration program.

2.1 Sample Program

The configuration program consists of several source files such as the resetprg.c, describing the PowerON_Reset_PC function, and the hwsetup.c, describing the hardware setup function. Main source files are as follows.

- resetprg.c
- hwsetup.c
- cpg.c

"resetprg.c" is a source file created on the file automatically generated by the High-performance Embedded Workshop, and describes the PowerON_ResetPC function. The PowerON_ResetPC function initially executed after the reset is canceled. Its beginning address is set in the reset vector defined by the vecttbl.c.

"hwsetup.c" describes the HardwareSetup function called by the PowerON_Reset_PC function. The HardwareSetup function calls the io_set_cpg function to set the CPG.

"cpg.c" describes the io_set_cpg function which is called from the HardwareSetup function. The io_set_cpg function sets the frequency control registers (FRQCR, MCLKCR, and ACLKCR) to clear the module standby function for internal peripheral modules.

Figure 1 shows flow charts of the PowerON_Reset_PC function, the HardwareSetup function, and the io_set_cpg function.

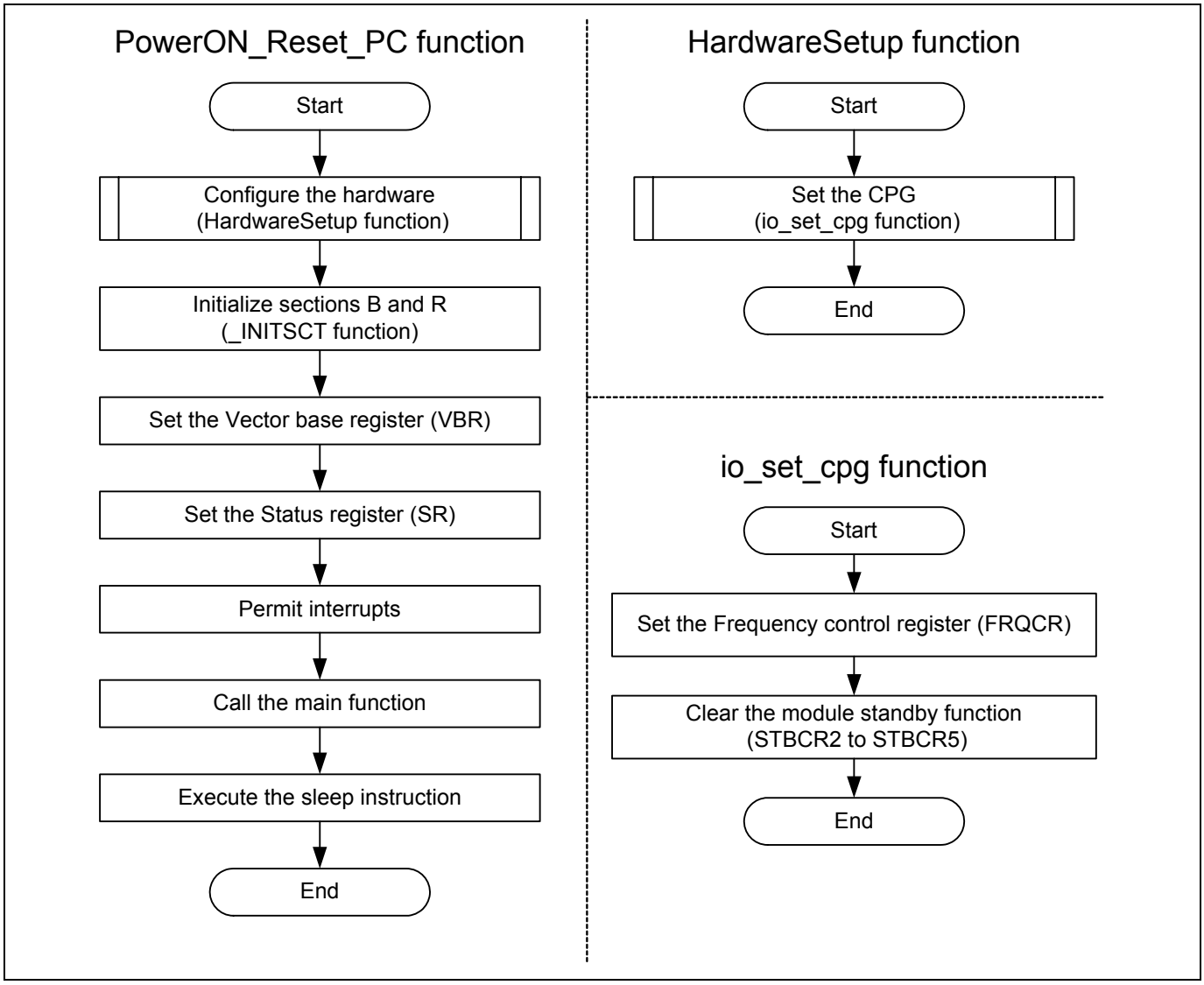


Figure 1 Flow Charts of Functions (PowerON_Reset_PC, HardwareSetup, io_set_cpg)

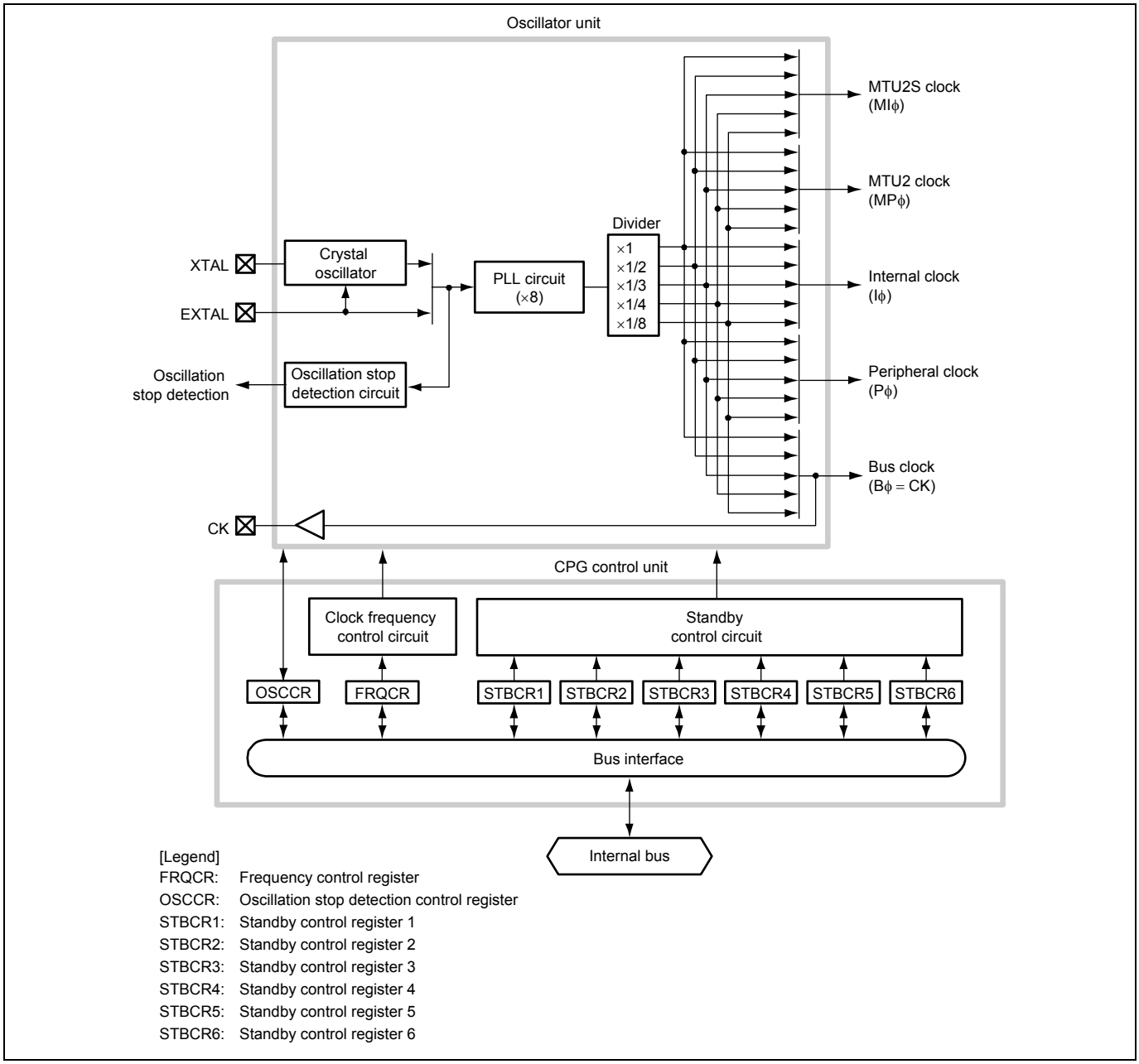
2.2 CPG Operation

CPG generates the internal clock (Iφ), bus clock (Bφ), peripheral clock (Pφ), clocks for MTU2S and MTU2 modules (MIφ, MPφ). It also controls the clock in low power mode.

The following table gives an overview of the CPG. Figure 2 shows the CPG block diagram.

Table 1 CPG Overview

Item	Description
Generate clock	• Internal clock (Iφ): Used by the CPU • Bus clock (Bφ): Used by the external bus interface • Peripheral clock (Pφ): Used by the internal peripheral module • MTU2S clock (MIφ): Used by the MTU2S module • MTU2 clock (MPφ): Used by the MTU2 module
Change frequency	• Sets frequencies for internal clock, bus clock, peripheral clock, MTU2S clock, and MTU2 clock independently using the divider circuits in the CPG. • Changes frequency by software using the Frequency control registers (FRQCR).
Control the low power mode	Stops clock in sleep mode or software standby mode. Stops the module specified by module standby function.



[Legend]
FRQCR: Frequency control register
OSCCR: Oscillation stop detection control register
STBCR1: Standby control register 1
STBCR2: Standby control register 2
STBCR3: Standby control register 3
STBCR4: Standby control register 4
STBCR5: Standby control register 5
STBCR6: Standby control register 6

Figure 2 CPG Block Diagram

2.3 CPG Setting

The figure below shows the flow chart of setting CPG. Internal peripheral modules are in module standby mode after the reset is canceled. The sample program clears the module standby function for internal peripheral module after setting the Frequency control register (FRQCR). For details on these registers, refer to the SH7137 Group Hardware Manual.

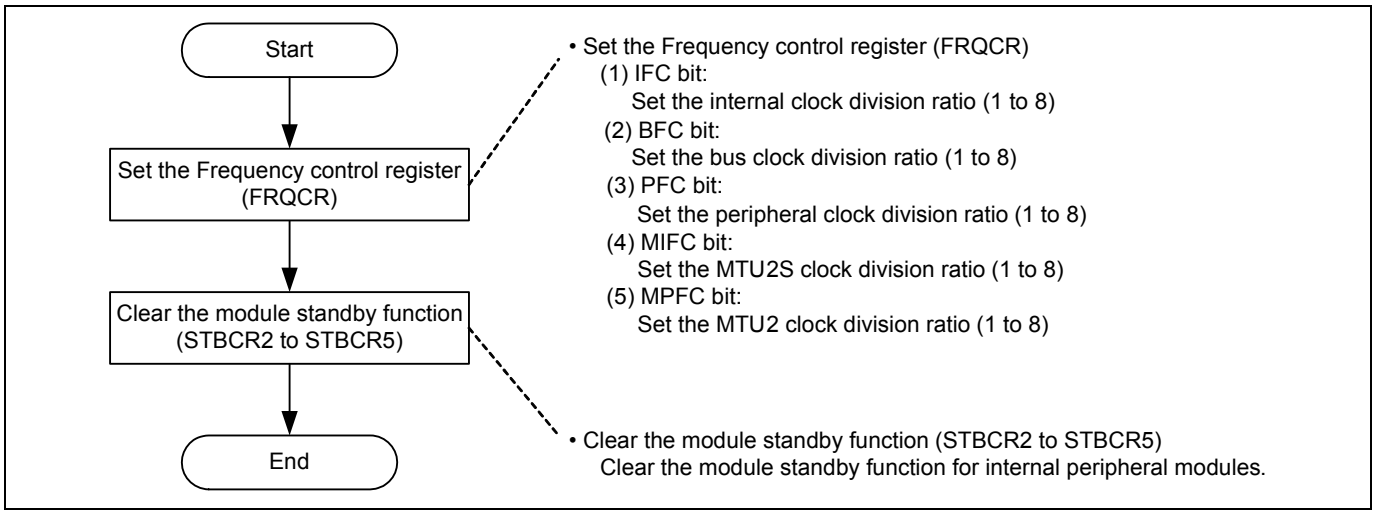


Figure 3 Flow Chart of CPG Setting

2.4 Setting in the Sample Program

Table 2 lists the setting in the sample program. Table 3 and

Table 4 list register settings for each module.

Table 2 Module Setting in the Sample Program

Module	Setting
Clock pulse generator (CPG)	• Clock frequency (input clock is 10 MHz) Internal clock: 80 MHz Bus clock: 40 MHz Peripheral clock: 40 MHz MTU2S clock: 80 MHz MTU2 clock: 40 MHz • Modules cleared the module standby function DTC, I^2C2, SCI_0, SCI_1, SCI_2, SSU, RCAN-ET_0, MTU2S, MTU2, CMT, A/D_0, A/D_1, AUD, UBC

Table 3 CPG Register Settings (1/2)

Register Name	Address	Setting	Description
Frequency control register (FRQCR)	H'FFFF E800	H'0241	• IFC[2:0] = "B'000": Internal clock (Iφ) division ratio = 1 • BFC[2:0] = "B'001": Bus clock (Bφ) division ratio = 2 • PFC[2:0] = "B'001": Peripheral (Pφ) clock division ratio = 2 • MIFC[2:0] = "B'000": MTU2S clock (MIφ) division ratio = 1 • MPFC[2:0] = "B'001": MTU2 clock (MPφ) division ratio = 2

Table 4 CPG Register Settings (2/2)

Register Name	Address	Setting	Description
Standby control register 2 (STBCR2)	H'FFFF E804	H'28	• MSTP7 = "0": RAM is operating • MSTP6 = "0": ROM is operating • MSTP4 = "0": DTC is operating
Standby control register 3 (STBCR3)	H'FFFF E806	H'42	• MSTP15 = "0": I^2C2 is operating • MSTP13 = "0": SCI_2 is operating • MSTP12 = "0": SCI_1 is operating • MSTP11 = "0": SCI_0 is operating • MSTP10 = "0": SSU is operating • MSTP8 = "0": RCAN-ET_0 is operating
Standby control register 4 (STBCR4)	H'FFFF E808	H'07	• MSTP23 = "0": MTU2S is operating • MSTP22 = "0": MTU2 is operating • MSTP21 = "0": CMT is operating • MSTP20 = "0": A/D_1 is operating • MSTP19 = "0": A/D_0 is operating
Standby control register 5 (STBCR5)	H'FFFF E80A	H'00	• MSTP25 = "0": AUD is operating • MSTP24 = "0": UBC is operating

3. Sample Program Listing

3.1 Sample Program Listing "resetprg.c" (1/3)

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29      *""FILE COMMENT""*********** Technical reference data *************************
30      *   System Name : SH7137 Sample Program
31      *   File Name    : resetprg.c
32      *   Abstract     : SH7137 Initial Setting
33      *   Version      : 1.00.00
34      *   Device       : SH7137
35      *   Tool-Chain  : High-performance Embedded Workshop (Ver.4.03.00).
36      *                 : C/C++ compiler package for the SuperH RISC engine family
37      *                 :                                    (Ver.9.01 Release01).
38      *   OS           : None
39      *   H/W Platform: M3A-HS37 (CPU board)
40      *   Description :
41      ***********************************************************************
42      *   History      : Jun.18,2009 Ver.1.00.00
43      *""FILE COMMENT END""*****************************************************/
44      #include <machine.h>
45      #include <_h_c_lib.h>
46      #include "stacksct.h"
47      #include "iodefine.h"
48
```

3.2 Sample Program Listing "resetprg.c" (2/3)

```
49    /* ==== Macro definition ==== */
50    #define SR_Init     0x000000F0
51    #define INT_OFFSET 0x10
52
53    /* ==== Prototype declaration ==== */
54    void PowerON_Reset_PC(void);
55    void Manual_Reset_PC(void);
56
57    /* ==== External reference declaration ==== */
58    /* ---- Function prototype ---- */
59    extern void HardwareSetup(void);
60    extern void main(void);
61    /* ---- Global variable ---- */
62    extern unsigned int INT_Vectors;
63
64    /* ==== Section name changed to ResetPRG ==== */
65    #pragma section ResetPRG
66
67    /* ==== Entry function specified ==== */
68    #pragma entry PowerON_Reset_PC
69
70    /*""FUNC COMMENT""*****************************************************************
71     * ID             :
72     * Outline        : CPU initialization
73     *-------------------------------------------------------------------------------
74     * Include        : <machine.h> and <_h_c_lib.h>
75     *-------------------------------------------------------------------------------
76     * Declaration    : void PowerON_Reset_PC(void);
77     *-------------------------------------------------------------------------------
78     * Description    : Executes the CPU initialization processing to register
79     *                  : the power-on reset vector to the exception vector table.
80     *-------------------------------------------------------------------------------
81     * Argument       : void
82     *-------------------------------------------------------------------------------
83     * Return Value : void
84     *-------------------------------------------------------------------------------
85     * Note           : This function is executed first after power-on reset.
86     *""FUNC COMMENT END""*************************************************************/
87    void PowerON_Reset_PC(void)
88    {
89        /* ==== Hardware initialization ==== */
90        HardwareSetup();                /* HardwareSetup function */
91
92        /* ==== B and R sections initialization ==== */
93        _INITSCT();
94
```

3.3 Sample Program Listing "resetprg.c" (3/3)

```
95        /* ==== Vector Base Register setting ==== */
96        set_vbr((void *)((char *)&INT_Vectors - INT_OFFSET));
97
98        /* ==== Status Register initialization ==== */
99        set_cr(SR_Init);
100       nop();
101
102       /* ==== Interrupt enabling ==== */
103       set_imask(0);                    /* Interrupt mask bits clear */
104
105       /* ==== Main function call ==== */
106       main();
107
108       /* ==== Sleep instruction execution ==== */
109       sleep();
110   }
111
112   //#pragma entry Manual_Reset_PC     /* Remove the comment when you use Manual Reset */
113   /*""FUNC COMMENT""*****************************************************************
114    * ID             :
115    * Outline        : Manual reset processing
116    *-------------------------------------------------------------------------------
117    * Include        :
118    *-------------------------------------------------------------------------------
119    * Declaration  : void Manual_Reset_PC(void);
120    *-------------------------------------------------------------------------------
121    * Description  : Registers the manual reset vector to the exception vector table.
122    *-------------------------------------------------------------------------------
123    * Argument       : void
124    *-------------------------------------------------------------------------------
125    * Return Value : void
126    *-------------------------------------------------------------------------------
127    * Note           : This sample does not describe the processing content at all.
128    *                 : Add the program in this function as needed.
129    *""FUNC COMMENT END""*************************************************************/
130   void Manual_Reset_PC(void)
131   {
132       /* NOP */
133   }
134
135   /* END of File */
```

3.4 Sample Program Listing "hwsetup.c" (1/2)

```
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29  *""FILE COMMENT""*********** Technical reference data *************************
30  *   System Name : SH7137 Sample Program
31  *   File Name    : hwsetup.c
32  *   Abstract     : Hardware Function Initial Setting
33  *   Version      : 1.00.00
34  *   Device       : SH7137
35  *   Tool-Chain  : High-performance Embedded Workshop (Ver.4.03.00).
36  *                 : C/C++ compiler package for the SuperH RISC engine family
37  *                 :                                    (Ver.9.01 Release01).
38  *   OS           : None
39  *   H/W Platform: M3A-HS37 (CPU board)
40  *   Description :
41  ***********************************************************************
42  *   History      : Jun.18,2009 Ver.1.00.00
43  *""FILE COMMENT END""*****************************************************/
44  #include "iodefine.h"
45
46  /* ==== Prototype declaration ==== */
47  void HardwareSetup(void);
48
```

3.5 Sample Program Listing "hwsetup.c" (2/2)

```
49    /* ==== External reference ==== */
50    /* ---- Function prototype ---- */
51    extern void io_set_cpg(void);
52
53    /*""FUNC COMMENT""*****************************************************************
54     * ID             :
55     * Outline        : Hardware initialization
56     *-------------------------------------------------------------------------------
57     * Include        :
58     *-------------------------------------------------------------------------------
59     * Declaration  : void HardwareSetup(void);
60     *-------------------------------------------------------------------------------
61     * Description  : Initializes the hardware function.
62     *-------------------------------------------------------------------------------
63     * Argument       : void
64     *-------------------------------------------------------------------------------
65     * Return Value : void
66     *-------------------------------------------------------------------------------
67     * Note           : None
68     *""FUNC COMMENT END""*************************************************************/
69    void HardwareSetup(void)
70    {
71        /* ==== CPG setting ==== */
72        io_set_cpg();
73    }
74
75    /* End of File */
```

3.6 Sample Program Listing "cpg.c" (1/2)

```
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29    *""FILE COMMENT""************ Technical reference data *************************
30    *   System Name : SH7137 Sample Program
31    *   File Name    : cpg.c
32    *   Abstract     : CPG Setting Processing
33    *   Version      : 1.00.00
34    *   Device       : SH7137
35    *   Tool-Chain  : High-performance Embedded Workshop (Ver.4.03.00).
36    *                 : C/C++ compiler package for the SuperH RISC engine family
37    *                 :                                    (Ver.9.01 Release01).
38    *   OS           : None
39    *   H/W Platform: M3A-HS37 (CPU board)
40    *   Description :
41    ***********************************************************************
42    *   History      : Jun.18,2009 Ver.1.00.00
43    *""FILE COMMENT END""*****************************************************/
44    #include "iodefine.h"
45
46    /* ==== Prototype declaration ==== */
47    void io_set_cpg(void);
48
```

3.7 Sample Program Listing "cpg.c" (2/2)

```
/*""FUNC COMMENT""*****************************************************************
 * ID             :
 * Outline        : CPG setting
 *-----------------------------------------------------------------------------
 * Include        : "iodefine.h"
 *-----------------------------------------------------------------------------
 * Declaration    : void io_set_cpg(void);
 *-----------------------------------------------------------------------------
 * Description    : Initializes the clock pulse generator (CPG) as follows:
 *                :   I-clock = 80MHz, B-clock = 40MHz, P-clock = 40MHz,
 *                :   MI-clock = 80MHz, and MP-clock = 40MHz.
 *                : And then supplies clock to all the peripheral modules.
 *-----------------------------------------------------------------------------
 * Argument       : void
 *-----------------------------------------------------------------------------
 * Return Value : void
 *-----------------------------------------------------------------------------
 * Note           : This function is an example of CPG setting at the input clock
 *                : of 10MHz.
 *""FUNC COMMENT END""*************************************************************/
void io_set_cpg(void)
{
    /* ==== CPG setting ==== */
    CPG.FRQCR.WORD = 0x0241;        /* Clock-in = 10MHz */
                                        /* I-clock = 80MHz */
                                        /* B-clock = 40MHz */
                                        /* P-clock = 40MHz */
                                        /* MI-clock = 80MHz */
                                        /* MP-clock = 40MHz */


    /* ==== Module Stanby Clear ==== */
    STB.CR2.BYTE = 0x28;            /* RAM, ROM, Reserve(1), DTC, Reserve(1), */
                                        /* Reserve(0), Reserve(0), Reserve(0) */

    STB.CR3.BYTE = 0x42;            /* IIC2, Reserve(1), SCI_2, SCI_1, SCI_0, */
                                        /* SSU, Reserve(1), RCAN */

    STB.CR4.BYTE = 0x07;            /* MTU2S, MTU2, CMT, A/D_1, A/D_0, */
                                        /* Reserve(1), Reserve(1), Reserve(1) */

    STB.CR5.BYTE = 0x00;            /* Reserve(0), Reserve(0), Reserve(0), */
                                        /* Reserve(0), Reserve(0), Reserve(0), */
                                        /* AUD, UBC */
}

/* End of File */
```

3.8 Sample Program Listing "vecttbl.c" (1/2)

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29  *""FILE COMMENT""*********** Technical reference data *************************
30  *   System Name : SH7137 Sample Program
31  *   File Name    : vecttbl.c
32  *   Abstract     : Initialization for Vector Table
33  *   Version      : 1.00.00
34  *   Device       : SH7137
35  *   Tool-Chain  : High-performance Embedded Workshop (Ver.4.03.00).
36  *                 : C/C++ compiler package for the SuperH RISC engine family
37  *                 :                                    (Ver.9.01 Release01).
38  *   OS           : None
39  *   H/W Platform: M3A-HS37 (CPU board)
40  *   Description :
41  ***********************************************************************
42  *   History      : Jun.18,2009 Ver.1.00.00
43  *""FILE COMMENT END""*****************************************************/
44  #include "vect.h"
45
46  #pragma section VECTTBL
47  void *RESET_Vectors[] = {
48  // <<VECTOR DATA START (POWER ON RESET)>>
49  // 0 Power On Reset PC
50      (void *)PowerON_Reset_PC,
```

3.9 Sample Program Listing "vecttbl.c" (2/2)

```
51      // <<VECTOR DATA END (POWER ON RESET)>>
52      // 1 Power On Reset SP
53          __secend("S"),
54      // <<VECTOR DATA START (MANUAL RESET)>>
55      // 2 Manual Reset PC
56          (void *)Manual_Reset_PC,
57      // <<VECTOR DATA END (MANUAL RESET)>>
58      // 3 Manual Reset SP
59          __secend("S")
60      };
61
62      #pragma section INTTBL
63      void *INT_Vectors[] = {
64      // 4 Illegal code
65          (void *)INT_Illegal_code,

...     ...

566     // 255 Reserved
567         (void *)Dummy
568     };
569
570     /* End of File */
```

4. References

- Software Manual
  SH-1/SH2/SH-DSP Software Manual Rev. 7.00
  (Download the latest version from the Renesas website.)

- Hardware Manual
  SH7137 Group Hardware Manual Rev. 2.00
  (Download the latest version from the Renesas website.)

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Revision History

Rev.	Date	Description	
		Page	Summary
1.00	Jun. 30, 2009	—	First edition issued

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