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SH7263/SH7203 Groups

Example of Initialization

Introduction

This application note describes an example of initialization of the SH7263 and SH7203 CPUs.

Target Devices

SH7263/SH7203

Contents

1. Preface

1.1 Specifications

The clock pulse generator (CPG), bus state controller (BSC), pin function controller (PFC), and cache are initialized after release from the reset state.

1.2 Modules Used

- Clock pulse generator (CPG)
- Bus state controller (BSC)
- Pin function controller (PFC)
- Cache

1.3 Applicable Conditions

• MCU	SH7263/SH7203
• Operating frequency	Internal clock: 200 MHz Bus clock: 66.67 MHz Peripheral clock: 33.3 MHz
• C compiler	SuperH RISC Engine Family C/C++ Compiler Package Ver.9.01 from Renesas Technology
• Compiler options	-cpu = sh2afpu -fpu = single -include = "$(WORKSPDIR)\inc" -object = "$(CONFIGDIR)\$(FILELEAF).obj" -debug -gbr = auto –chgincpath -errorpath -global_volatile = 0 -opt_range = all -infinite_loop = 0 -del_vacant_loop = 0 -struct_alloc = 1 –nologo

1.4 Related Application Notes

Please refer to the following application notes in combination with this one.

- SH7263/SH7203 Example of Setting the CPU to Change the Operating Frequency
- SH7263/SH7203 Example of Connection with BSC SDRAM Interface (16-Bit Data Bus)
- SH7263/SH7203 Example of Setting the BSC for Connection with NOR Flash Memory (16-Bit Data Bus)
- SH7263/SH7203 Example of Setting the Cache

2. Description of the Sample Application

Use of the program for initial settings described in this application note is a precondition for all of the other SH7263/SH7203 application notes.

2.1 Description of the Sample Program

The initialization program consists of the following two source files:

- resetprg.c
- hwsetup.c

Code for the PowerON_Reset_PC function, which is executed first after release from the reset state, is written in resetprg.c.

Code for the HardwareSetup function, which is called from the PoweON_Reset_PC function, is written in hwsetup.c. Code in the HardwareSetup function includes the individual function calls for the CPG, BSC, and cache settings.

Figure 1 shows flows of processing by the PowerON_Reset_PC and HardwareSetup functions.

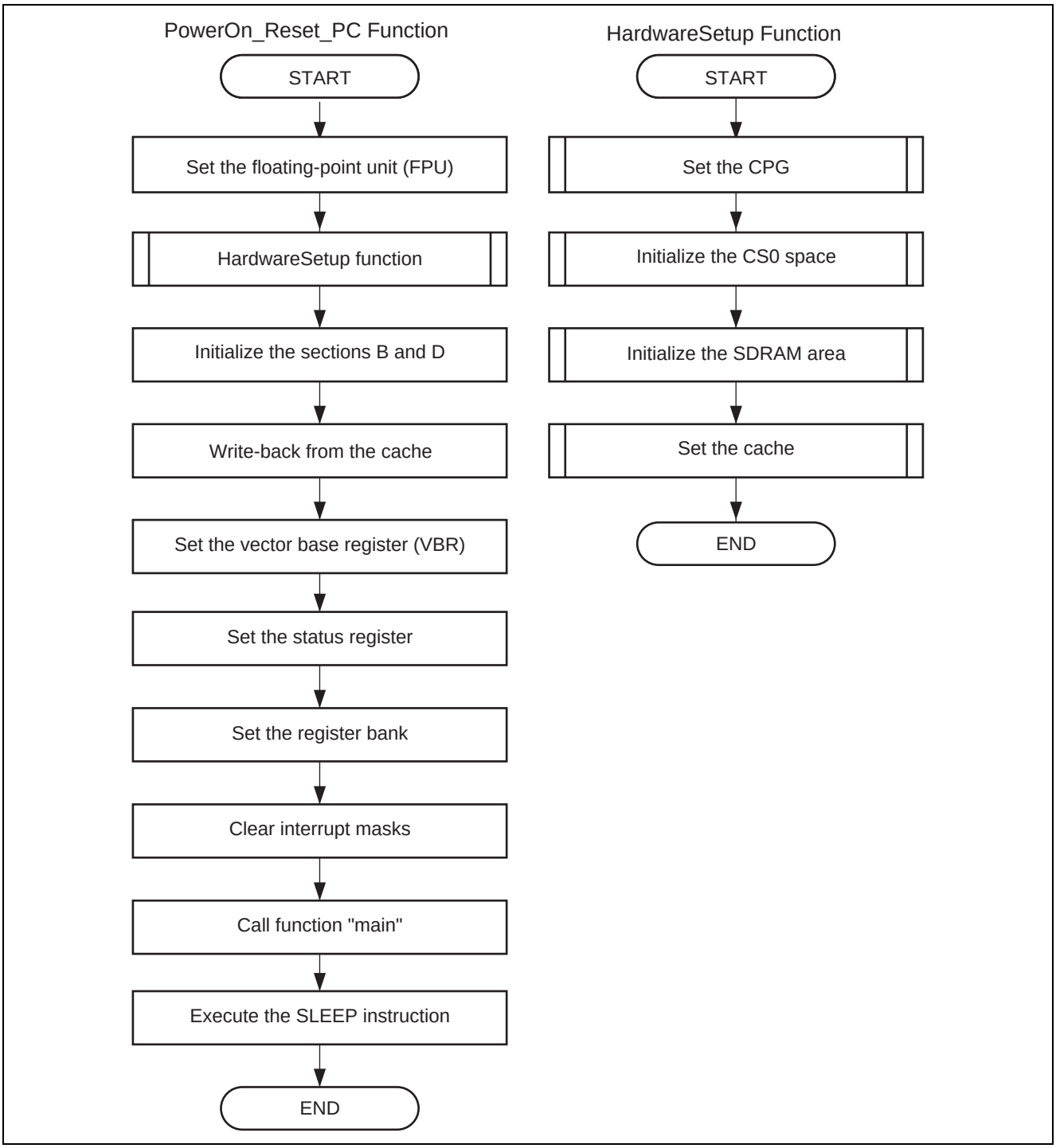

Figure 1 Flows of Processing by the PowerON_Reset_PC and HardwareSetup Functions

2.2 Description of Settings in the Sample Program

Table 1 is a list of the settings in the sample program.

Table 1 Settings in the Sample Program

Module	Description
FPU	Transfer size of FMOV instruction: 32 bits Precision mode: Single-precision operations Rounding mode: Round to zero Denormalized number is treated as zero.
CPG	Input clock: 16.67 MHz Internal clock: 200 MHz Bus clock: 66.67 MHz Peripheral clock: 33.33 MHz
INTC	Use of register banks is enabled for all interrupts except NMI and user break. (Settings of the bank control register (IBCR) are ignored.)
BSC	CS0 space: Flash memory Number of cycles to wait for access: 6 cycles CS3 space: SDRAM Data bus width: 32 bits Row address bits: 12 Column address bits: 9 CAS latency: 2 cycles
PFC	The address bus, data bus, and bus control pin functions for use in the CS0 and CS3 spaces are selected for multiplexed pins.
Cache	Instruction/operand cache is enabled.

2.3 Notes on Using the Sample Program

In this sample program, the bus state controller is initialized in HardwareSetup function. Only access sections B and D in external memory after initialization of the bus state controller.

3. Listing of Sample Program

1. Sample Program Listing: "resetprg.c" (1)

```
/*""FILE COMMENT""*****************************************************************
*
*          System Name    : SH7203 Sample Program
*          File Name      : resetprg.c
*          Version        : 1.00.00
*          Contents       : sample main
*          Model          : M3A-HS30
*          CPU            : SH7203
*          Compiler       : SHC9.1.1.0
*          OS             : none
*
*          note           :
*
*                 Note
*                 This sample program is for reference
*                 and its operation is not guaranteed.
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*       history        : 2007.11.13 ver.1.00.00
* ""FILE COMMENT END""*************************************************************/
#include <machine.h>
#include <_h_c_lib.h>
#include "stacksct.h"
#include "iodefine.h"

#define FPSCR_Init     0x00040001

#define SR_Init        0x000000F0
#define INT_OFFSET     0x10

extern unsigned int INT_Vectors;
void PowerON_Reset_PC(void);
void Manual_Reset_PC(void);

extern void main(void);
extern void HardwareSetup(void);
extern void io_cache_writeback(void);



//extern void srand(unsigned int);    // Remove the comment when you use rand()
//extern char *_s1ptr;                // Remove the comment when you use strtok()

/*==== Switch section name to ResetPRG ====*/
#pragma section ResetPRG

/*==== Specifying the entry function ====*/
#pragma entry PowerON_Reset_PC
```

2. Sample Program Listing: "resetprg.c" (2)

```
/*""FUNC COMMENT""*****************************************************************
* ID           :
* Outline      : CPU initialization function
*-----------------------------------------------------------------------------
* Include      : #include "iodefine.h"
*-----------------------------------------------------------------------------
* Declaration  : void PowerON_Reset_PC(void) ;
*-----------------------------------------------------------------------------
* Function     : It is the CPU initialization process to register the power on
*              : reset exception vector table.
*              : This function is firstly executed after power on reset.
*-----------------------------------------------------------------------------
* Argument     : None
*-----------------------------------------------------------------------------
* Returnvalue  : None
*-----------------------------------------------------------------------------
* Notice       : Enable the processes that are commented depending on its needs.
*              :
*""FUNC COMMENT END""*************************************************************/
void PowerON_Reset_PC(void)
{
        set_fpscr(FPSCR_Init);

        /*==== HardwareSetup function====*/
        HardwareSetup();          // Use Hardware Setup

        /*==== B and D sections initialization ====*/
        _INITSCT();
        io_cache_writeback();

        /*==== Vector base register (VBR) setting ====*/
        set_vbr((void *)((char *)&INT_Vectors - INT_OFFSET));

//      _INIT_IOLIB();            // Use stdio I/O

//      errno=0;                  // Remove the comment when you use errno
//      srand(1);                 // Remove the comment when you use rand()
//      _s1ptr=NULL;              // Remove the comment when you use strtok()

        /*==== Status register setting ====*/
        set_cr(SR_Init);
        nop();

        /* ==== Bank number register setting ==== */
        INTC.IBNR.BIT.BE = 0x01;  /* Use the register bank in all interrupts */

        /* ==== Interrupt mask level change ==== */
        set_imask(0);

        /*==== Function call of main function ====*/
        main();

        /*==== sleep instruction execution ====*/
        sleep();
}
```

3. Sample Program Listing: "resetprg.c" (3)

```
115 //#pragma entry Manual_Reset_PC      // Remove the comment when you use Manual Reset
116 /*""FUNC COMMENT""*************************************************************
117 * ID           :
118 * Outline      : Manual reset process
119 *-----------------------------------------------------------------------------
120 * Include      :
121 *-----------------------------------------------------------------------------
122 * Declaration  : void Manual_Reset_PC(void);
123 *-----------------------------------------------------------------------------
124 * Function     : It is the function to register the manual reset exception vector table.
125 *              : The process is not defined in the reference program.
126 *              : Add the processes depending on its needs
127 *-----------------------------------------------------------------------------
128 * Argument     : None
129 *-----------------------------------------------------------------------------
130 * ReturnValue  : None
131 *-----------------------------------------------------------------------------
132 * Notice       : None
133 * ""FUNC COMMENT END""*************************************************************/
134 void Manual_Reset_PC(void)
135 {
136         /* NOP */
137 }
138 /* END of File */
```

4. Sample Program Listing: "hwsetup.c" (1)

```
139 /*""FILE COMMENT""*****************************************************************
140 *
141 *       System Name    : SH7203 Sample Software
142 *       File Name      : hwsetup.c
143 *       Version        : 1.00.00
144 *       Contents       : Hardware initialization function
145 *       Model          : M3A-HS30
146 *       CPU            : SH7203
147 *       Compiler       : SHC9.1.1.0
148 *       OS             : none
149 *
150 *       note           :
151 *                        Note
152 *                        This sample program is for reference
153 *                        and its operation is not guaranteed.
154 *                        Customers should use this sample program for technical reference
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164 *
165 *       history        : 2007.11.13 ver.1.00.00
166 *""FILE COMMENT END""*************************************************************/
167 #include "iodefine.h"
168
169 #define SDRAM_BUS_WIDTH    32      /* '32' is SDRAM bus width 32bit  SW6-4 = "OFF" */
170                                    /* '16' is SDRAM bus width 16bit  SW6-4 = "On" */
171
172 /* ==== Prototype declaration ==== */
173 void  HardwareSetup(void);
174
175 /* ==== referenced external Prototype declaration ==== */
176 extern void io_set_cpg(void);
177 extern void io_init_bsc_cs0(void);
178 extern void io_init_sdram(void);
179 extern void io_init_sdram32(void);
180 extern void io_init_cache(void);
181
```

5. Sample Program Listing: "hwsetup.c" (2)

```
/*""FUNC COMMENT""*************************************************************
* ID           :
* Outline      : Hardware initialization function
*-----------------------------------------------------------------------------
* Include      : #include "iodefine.h"
*-----------------------------------------------------------------------------
* Declaration  : void  HardwareSetup(void);
*-----------------------------------------------------------------------------
* Function     : The initial settings of CPG, PFC, and BSC Flash memory
*              : access control and SDRAM initialization) are processed.
*-----------------------------------------------------------------------------
* Argument     : None
*-----------------------------------------------------------------------------
* ReturnValue  : None
*-----------------------------------------------------------------------------
* Notice       :
*""FUNC COMMENT END""*********************************************************/
void    HardwareSetup(void)
{
            /*====CPG setting====*/
            io_set_cpg();

            /*====CS0 initialization====*/
            io_init_bsc_cs0();

            /*====SDRAM area initialization====*/
#if SDRAM_BUS_WIDTH == 16
            io_init_sdram();
#elif SDRAM_BUS_WIDTH == 32
            io_init_sdram32();
#else
            #error SDRAM_BUS_WIDTH
#endif

            /*====Cache setting====*/
            io_init_cache();

}
/* End of File */
```

4. Documents for Reference

- Software Manual
  SH-2A/SH2A-FPU Software Manual
  The most up-to-date version of this document is available on the Renesas Technology Website.
- Hardware Manuals
  SH7203 Group Hardware Manual
  SH7263 Group Hardware Manual
  The most up-to-date versions of the documents are available on the Renesas Technology Website.

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