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SH7206 Group

Example of BSC Flash Memory Connection

Introduction

This document describes a common case of setting up the bus state controller (BSC) in the form of a practical example of connection between flash memory and a normal space of the SH7206.

Target Device

SH7206

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2. Description of Application Examples 3
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5. Website and Support Window 11

1. Overview

1.1 Specifications

- 32-bit NOR-type flash memory (2 Mwords x 16 bits) is connected to the SH7206 with a 16-bit data bus width.
- The bus state controller (BSC) of the SH7206 is used to set up conditions for the execution of read and write operations.

1.2 Function Used

Bus state controller (BSC)

1.3 Applied Conditions

- MCU: SH7206 (R5S72060)
- Flash memory: M5M29KT331AVP
- Operating frequency: Internal clock of 200 MHz
  Bus clock of 66.67 MHz
  Peripheral clock of 33.33 MHz
- C compiler: Manufactured by Renesas Technology Corp.
  C/C++ compiler package Version 9.00 of the SuperH RISC engine Family
- Compile option: Default settings of the High-performance Embedded Workshop (-cpu=sh2a -debug -gbr=auto -global_volatile=0 -opt_range=all -infinite_loop=0 -del_vacant_loop=0 -struct_alloc=1)

1.4 Related Application Note

Operation of the sample program in this application note has been confirmed with the setting conditions given in the application note on *Example of SH7206 Initial Configuration*. Please refer to that document when setting up this sample task.

2. Description of Application Examples

2.1 Operation Overview of Function Used

The BSC of SH7206 is used to control externally connected flash memory. Table 1 shows the specifications of the flash memory used in this sample task.

Table 1 Flash Memory Specifications Used in this Sample Task

Item	Flash Memory Specification
Product Type No.	M5M29KT331AVP (manufactured by Renesas)
Configuration	4 Mbytes (2 Mwords x 16 bits x 1)
Access Time	At random access: 70 ns (maximum) At page read: 25 ns (maximum)
Boot Block	Top boot

Figure 1 is the memory map. Specifications to suit the type of memory to be connected and set up the corresponding data bus width are made per CS space. In this sample task, flash memory is connected to the CS0 space.

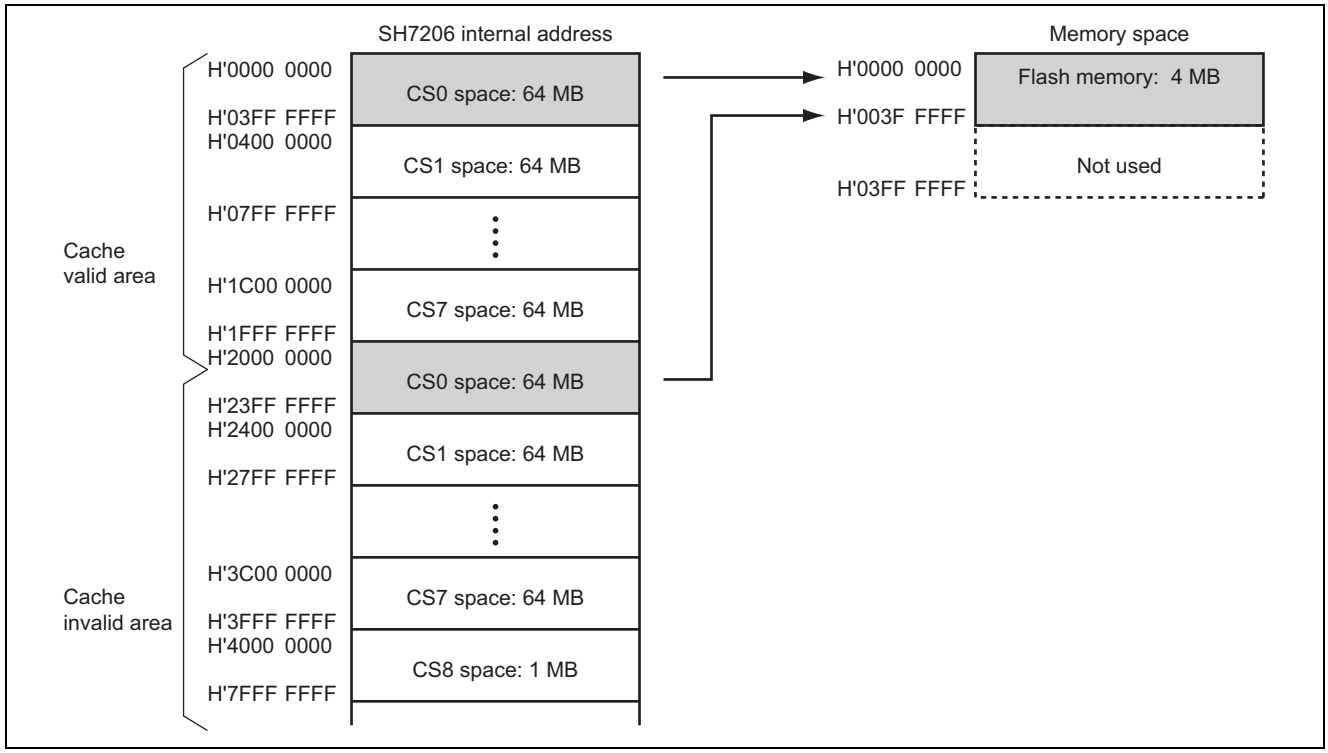

Figure 1 Memory Map

Figure 2 shows an example of a circuit used to connect flash memory.

SH7206 is connected to M5M29KT331AVP with a 16-bit data bus width. To set up the M5M29KT331AVP to operate with a data-bus width of 16 bits, the $\overline{\text{BYTE}}$ singal is fixed to the high level. To set up the CS0 space of the SH7206 for the same bus width, the MD2 pin is fixed to the high level and the MD0 pin is fixed to the low level.

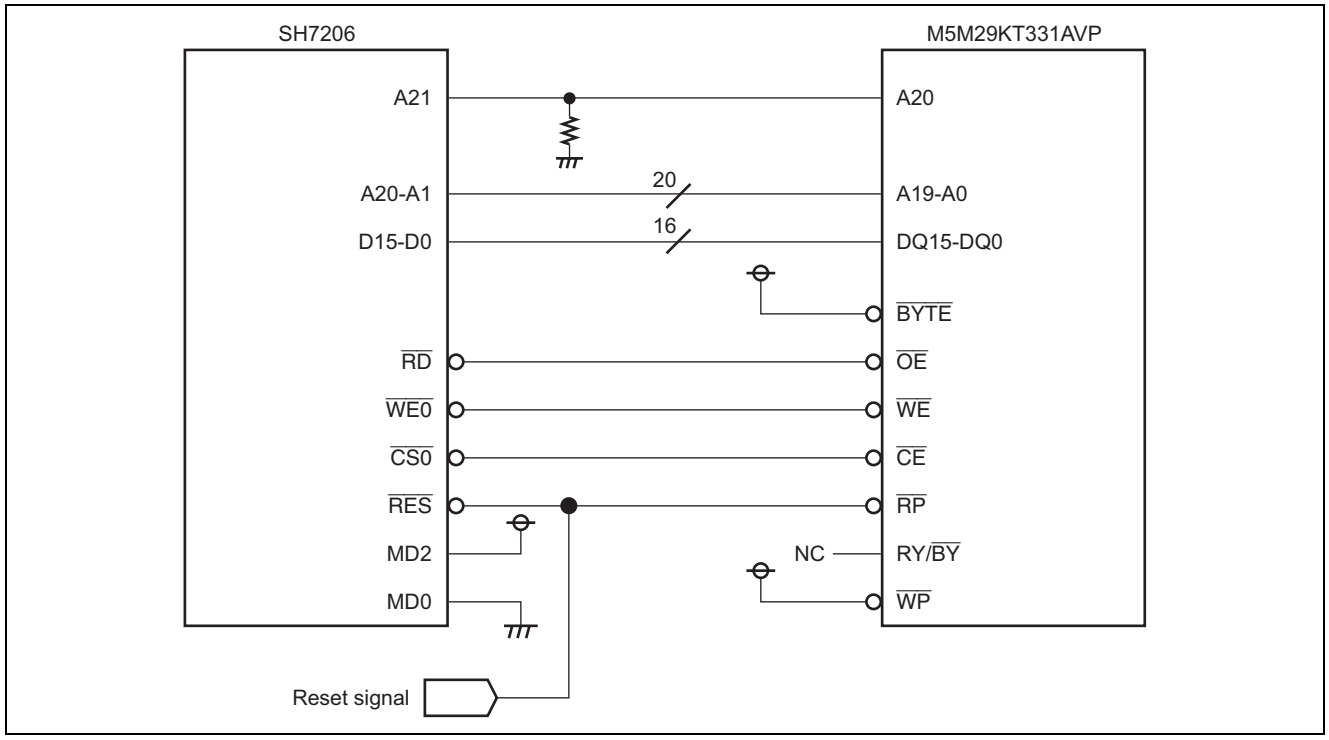

Figure 2 Sample Circuit for the Connection of Flash Memory (4-Mbyte and 16-bit bus)

Table 2 shows pin functions of the SH7206. Pins A21 and $\overline{WE0}$ are initially set for operation as I/O pins. To do this, the pin-function controller (PFC) must be used to switch the pin functions.

Table 2 SH7206 Pin Functions

SH7206 Pin	Input/Output	Initial Pin Function	Function
A21	Output	I/O port (PB9)	Address bus
A20 to A2	Output	A20 to A2	Address bus
A1	Output	*1	Address bus
D15 to D8	Input/output	*1	Data bus
D7 to D0	Input/output	D7 to D0	Data bus
$\overline{RD}$	Output	$\overline{RD}$	Read pulse signal (read data output enable signal)
$\overline{WE0}$	Output	I/O port (PA12)	Indicates byte write on D7 to D0
$\overline{CS0}$	Output	$\overline{CS0}$	Chip selection
MD2, MD0	Output	MD2, MD0	Select initial values for the CS0 space data bus width and CS1 to CS7 space data bus widths. The CS0 space data bus width cannot be changed after a power-on reset.

MD2	MD0	Data bus width
1	1	32 bits
	0	16 bits*
0	1	8 bits
	0	Reserved (please do not set)

*This is the set value for this sample task.

Note: *1. Initial pin functions after a power-on rest differ according to the settings of pins MD2 and MD0.

2.2 Procedure for Setting of Functions Used

Table 3 gives an example of the bus state controller settings. For details on the individual registers, please refer to the *SH7206 Group Hardware Manual*.

Table 3 Example of Bus State Controller Setting

Name of Register	Address	Setting Value	Function
CS0 space bus control register (CS0BCR)	H'FFFC 0004	H'2000 0400	-IWW[2:0] = B'010 Idle cycles for insertion between write and read and between write and write: 2 Note: Values written to the BSZ[1:0] bits (bits to specify data bus width) in this register will be ignored. Please set the MD2 and MD0 pins to specify the width of the data bus in the CS0 space.
CS0 space wait control register (CS0WCR)	H'FFFC 0028	H'0000 0AC1	-SW[1:0] = B'01 Number of delay cycles from address and $\overline{CS0}$ assertion to $\overline{RD}$ or $\overline{WE}$ assertion: 1.5 -WR[3:0] = B'0101 Number of access-wait cycles: 5 -WM = B'1 Ignore external wait input -HW[1:0] = B'01 Number of cycles for delay from negation of $\overline{RD}$ or $\overline{WEn}$ to negation of the address and $\overline{CS0}$: 1.5

Figure 3 shows an example of the procedure for setting up the bus state controller.

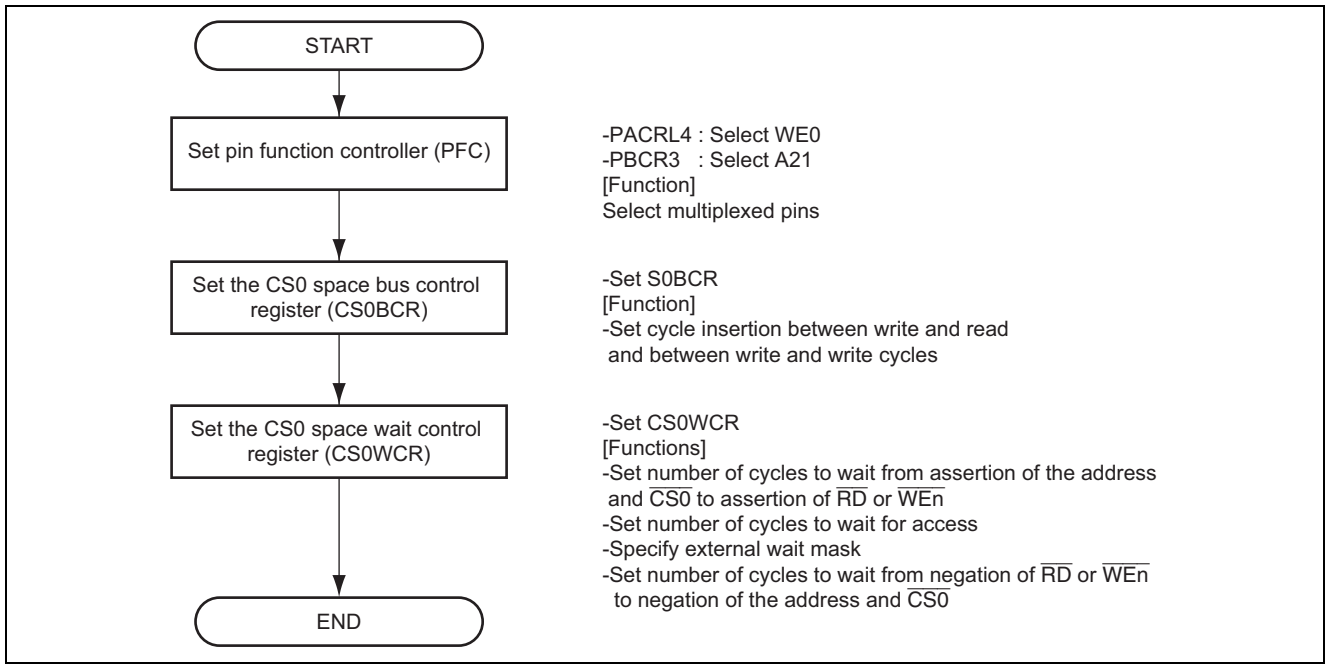

Figure 3 Example of the Procedure for Setting up the Bus State Controller

2.3 Operation of the Sample Program

In this sample program, we set the numbers of wait cycles required to support the access speed of the memory unit (M5M29KT331AVP) to be connected. The SH7206 establishes a frequency of 66.67 MHz (tcyc = 15 ns) as an operating condition for the bus clock. For the AC characteristics of the SH7206 and M5M29KT331AVP, please refer to the datasheets for the individual devices. The settings for wait cycles in this sample program are as follows.

- Expansion of CS assert period
  - — Delay cycle (Th) from address and $\overline{CS0}$ assert to $\overline{RD}$ and $\overline{WE0}$ assert
    In this sample program, 1.5 cycles (Th = 1.5) is set as delay cycle. The equation below confirms that this setting satisfies the tCS (chip enable setup time) requirement of the M5M29KT331AVP.
    tCS (min.) ≤ tcyc x (Th - 0.5) + tWED1 (min) - tCSD1 (max.)

  - — Delay cycle (Tf) from $\overline{RD}$ and $\overline{WE0}$ negate to address and $\overline{CS0}$ negate
    In this sample program, 1.5 cycles (Tf = 1.5) is set as delay cycle. The equation below confirms that this setting satisfies the tAH (address hold time) requirement of the M5M29KT331AVP.
    tAH (min.) ≤ tcyc x (Tf + 0.5) + tAD1 (min.) - tWED1 (max.)

- Access wait cycle
  - — Number of wait cycles (Tw) between T1 and T2 cycles. In this sample program, the setting is 5 cycles (Tw = 5). The equations below confirm that this setting satisfies the bus-timing requirement of the M5M29KT331AVP and SH7206.
    - tRDS1 (read data setup time 1) of SH7206
      tRDS1 (min.) ≤ tcyc x (Tw + 1 + (Th - 0.5)) + tRSD (min.) - tAD1 (max.) - ta (AD)
      tRDS1 (min.) ≤ tcyc x (Tw + 1 + (Th - 0.5)) + tRSD (min.) - tCSD1(max.) - ta (CE)
      tRDS1 (min.) ≤ tcyc x (Tw+1) - ta (OE)
    - tRDH1 (read data hold time 1)
      tRDH1 (min.) ≤ tOH (min.)
    - tRC (read cycle time) of M5M29KT331AVP
      tRC (min.) ≤ tcyc x (Tw + 2 + (Th - 0.5) + (Tf - 0.5))
    - tWC (write cycle time) of M5M29KT331AVP
      tWC (min) ≤ tcyc x (Tw + 2 + (Th - 0.5) + (Tf - 0.5))
    - tAS (address setupt time) of M29KT331AVP
      tAS (min.) ≤ tcyc x (Tw + 2 + (Th - 0.5) + (Tf - 0.5))
    - tWP (write pulse width) of M5M29KT331AVP
      tWP (min.) ≤ tcyc x (Tw + 1)
    - tDS (data setup time) of M5M29KT331AVP
      tDS (min.) ≤ tcyc x (Tw + 1 + (Th - 0.5)) - tWDD1 (max.)
    - tDH (data hold time) of M5M29KT331AVP
      tDH (min.) ≤ tWDH4 (min.)

  - — Wait between access cycles
    Wait between access cycles is the wait setting for insertion between consecutive rounds of access. In this sample program, 2 cycles (Taw = 2) is set as the number of wait cycles between write and read/write and write cycles. The equation below confirms that this satisfies the tWPH (H write pulse width) requirement of the M5M29KT331AVP.
    tWPH (min.) ≤ tcyc x (1 + (Tf - 0.5) + (Th - 0.5) + Taw) - tWED1 (max.)

Figure 4 shows the timing of flash memory reading with the bus clock running at 66.67 MHz.

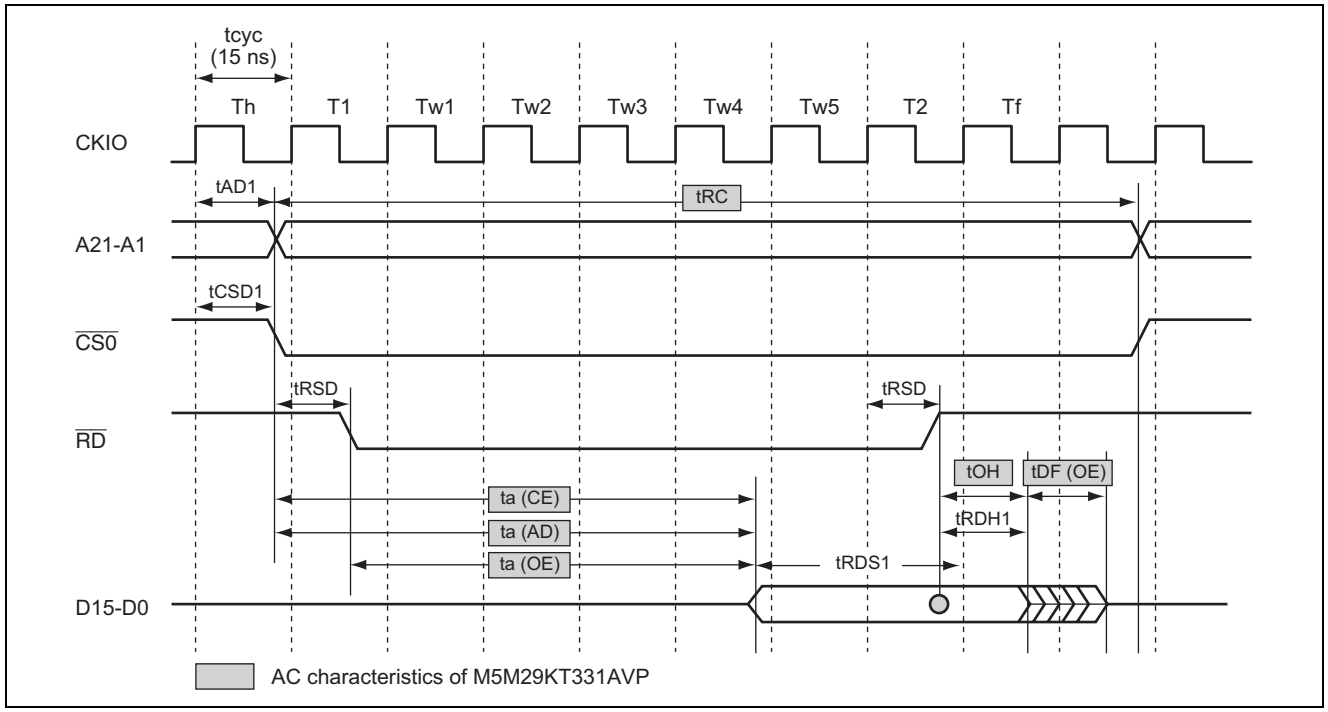

Figure 4 Timing of Flash Memory Reading (with the bus clock at 66.67 MHz)

Figure 5 show write timing of flash memory at 66.67 MHz of bus clock.

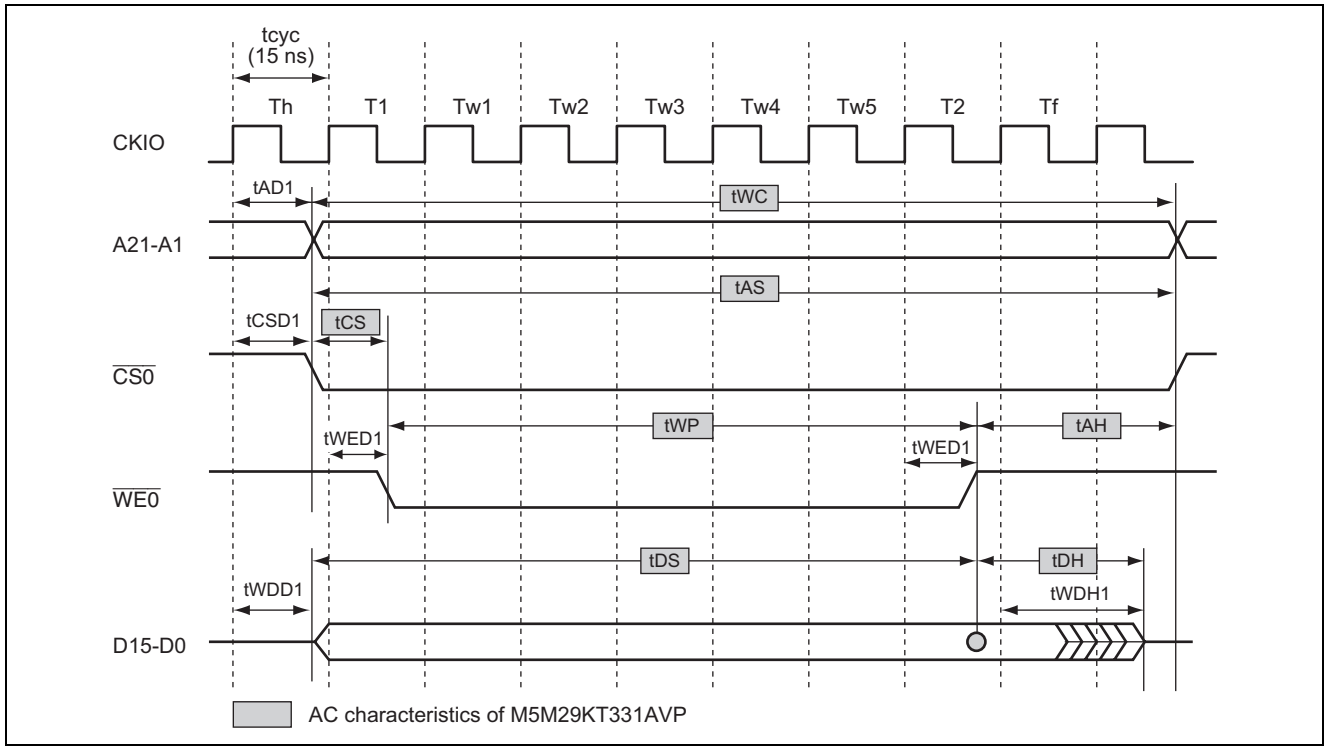

Figure 5 Flash Memory Write timing (at 66.7 MHz of bus clock)

3. Sample Program

- Sample Program: L isting of “bsc_cs0.c” (1)

```
1   /*""FILE COMMENT""*****************************************************************
2   *
3   *       System Name : SH7206 Sample Program
4   *       File Name   : bsc_cs0.c
5   *       Version     : 1.00.00
6   *       Contents    : Initial settings of the SH7206
7   *       Model       : M3A-HS60
8   *       CPU         : SH7206
9   *       Compiler    : SHC9.0.00
10  *       OS          : None
11  *
12  *       Note        :
13  *                     <Caution>
14  *                     This entire sample program is for reference only and
15  *                     its operation is not guaranteed.
16  *                     Please use this sample as a technical reference
17  *                     in software development.
18  *
19  *       Copyright (C) 2004,2005 Renesas Technology Corp. All Rights Reserved
20  *       AND Renesas Solutions Corp. All Rights Reserved
21  *
22  *       History     : 2004.10.01 ver.1.00.00
23  *                   : 2005.03.17 ver.1.00.01 Invalid number of wait cycles
24  *                   : 2005.03.22 ver.1.00.02 Wait cycle setting changed
25  *""FILE COMMENT END""*************************************************************/
26  #include "iodefine.h"
27
28  /* ==== Prototype declaration ==== */
29  void io_init_bsc_cs0(void);
30
```

- Sample Program: Listing of “bsc_cs0.c” (2)

```
/*""FUNC COMMENT""*****************************************************************
* ID         :
* Overview of module : CS0 setting
*-------------------------------------------------------------------------------
* Include            : #include "iodefine.h"
*-------------------------------------------------------------------------------
* Declaration        : void io_init_bsc_cs0(void)
*-------------------------------------------------------------------------------
* Function           : Sets pin function controller (PFC) and bus state
*                    : controller (BSC) to get proper timing for access to
*                    : Flash memory in the CS0 space
*-------------------------------------------------------------------------------
* Argument           : None
*-------------------------------------------------------------------------------
* Return value       : None
*-------------------------------------------------------------------------------
* Caution            : PFC settings are applied to the individual bits to avoid
*                    : changes to PFC settings made in other processing.
*""FUNC COMMENT END""*************************************************************/
void io_init_bsc_cs0(void)
{
      /* ==== PFC setting ==== */
      PORT.PACRL4.BIT.PA12MD = 0x1;     /* Set to WE0 output                  */
      PORT.PBCR3.BIT.PB9MD = 0x2;       /* Output A21                         */

      /* ==== CS0 space bus control register (CS0BCR) setting ==== */
      BSC.CS0BCR.LONG = 0x20000400ul;
                  /* Between write & read/between write & write cycles      */
                  /* Idle specification : inserts 2 idle cycles             */
                  /* Data bus width specification: 16-bit width             */

      /* ==== CS0 space wait control register (CS0WCR) setting ====  */
      BSC.UN0_BSC.NORMAL.REG_CS0WCR.LONG = 0x00000ac1ul;
            /* Cycles to wait for RD, WE assertion after addr., CS assertion*/
            /* :1.5                                                         */
            /* Number of cycles to wait for access :5                       */
            /* Ignore external wait input.                                  */
            /* RD, WE negation → cycles to wait for addr. and CS negation   */
            /* :1.5                                                         */
}

/* End of file */
```

4. Documents for Reference

- Software manual
  SH-2A SH2A-FPU Software Manual Rev.3.00
- Hardware manual
  SH7206 Group Hardware Manual Rev.1.00
- Datasheet
  M5M29KB/T331AVP Rev.1.0

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