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H8S Family

DRAM Control

Introduction

This sample task connects the DRAM to the H8S microcomputer by using the DRAM control function of the bus controller.

Target Device

H8S/2377R

Contents

1. Specifications

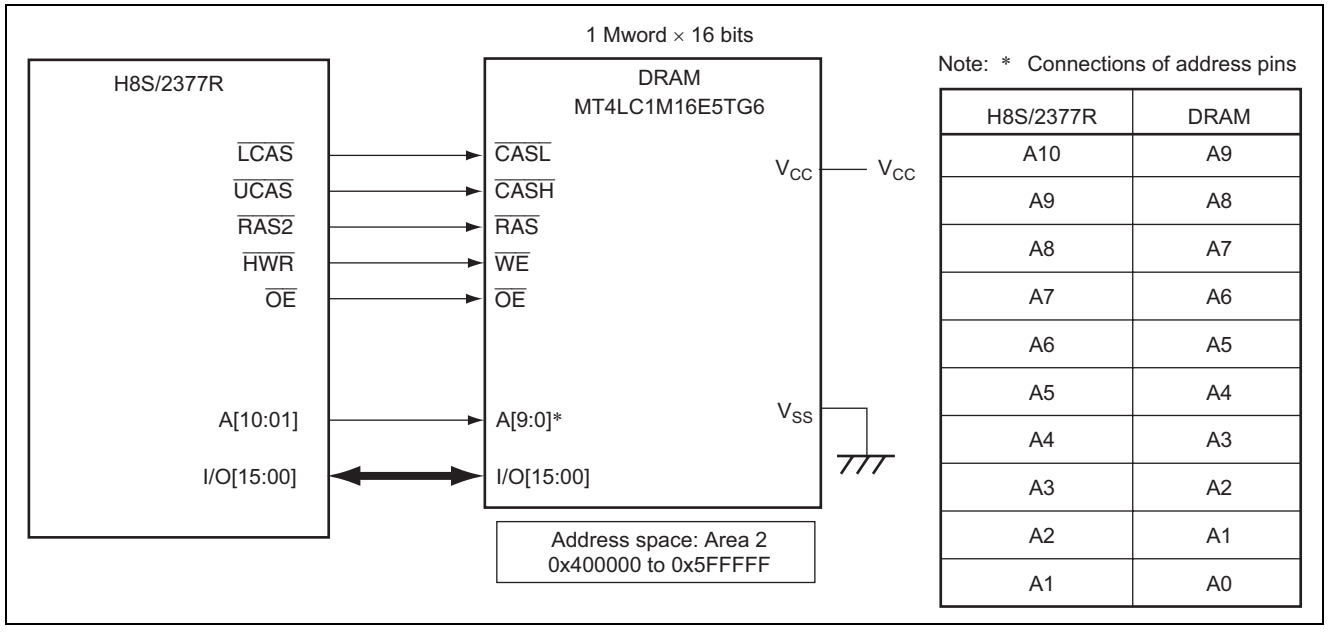
This sample task connects the DRAM to the H8S microcomputer by using the DRAM control function of the bus controller.

2. Configuration

Table 1 shows the configuration of this sample task.

Table 1 Configuration of This Sample Task

Component	Specification
H8S/2377 CPU board Part no.: HSB8S2377F (Manufactured by Hokuto Denshi Co., Ltd.)	Board power supply input: 3.3 V DC Operating frequency: 19.6608 MHz MCU operating mode: 4
EDO DRAM Part no.: MT4LC1M16E5TG6 (manufactured by Micron Technology, Inc.)	Power supply for operation: 3.3 V DC Capacity: 1 Mwords × 16 bits Refresh cycle: 16 ms/1024 cycles
Debugger High-performance Embedded Workshop	Version 4.02.00.022
Compiler H8S, H8/300, C/C++ compiler	Version 6.01.02
On-chip debugging emulator E10A-USB Part no.: HS0005KCU02H	



H8S/2377R	DRAM
A10	A9
A9	A8
A8	A7
A7	A6
A6	A5
A5	A4
A4	A3
A3	A2
A2	A1
A1	A0

Figure 1 Connections between H8S/2377R and DRAM

3. Description of Functions

By using the DRAM control function of the bus controller, this sample task directly links the DRAM to the H8S microcomputer, writes the fixed value 0x12345678 to address 0x400000, reads the address, and store it in the on-chip RAM area read_data.

On-Chip RAM Area Name	Data Size	Function
read_data	unsigned long	Area to store data read from the DRAM

4. Description of Operation

4.1 Initialization Processing

Before the DRAM can be accessed, appropriate settings must be performed in order to connect the DRAM.

(1) **Initial Values**

Register Name	Bit	Name	Value	Description	Reference Section
DRAMCR	10 to 8	RMTS2 to RMTS0	001	DRAM Space Setting Areas 3 to 5: Regular space Area 2: DRAM space	4.1 (2)
DRAMCR	2 to 0	MXC2 to MXC0	010	Address Multiplexing Setting (Sets the amount of row-address shift.) Sets to 10 bits.	4.1 (3)
PBDDR	7 to 0	—	0x07	Address Bus Setting Sets address output for A10 to A0	4.1 (4)
PCDDR	7 to 0	—	0xFF		
ABWCR	2	ABW2	0	Data Bus Width Setting Sets to 16 bits.	4.1 (5)
PFCR0	2	CS2E	1	RAS2 Pin Setting Sets the PG2 pin as the RAS2 pin.	—
PFCR2	1	OES	1	OE Pin Setting Sets the PH3 pin as the OE pin.	—
DRAMCR	15	OEE	1		
DRAMCR	12	CAST	0	Column Address Output Setting Sets to 2 states	4.1 (6)
DRAMCR	14	RAST	0	Row Address Output State Setting (Sets the RAS assertion timing) Asserts the signal at the falling edge of ϕ in a Tr cycle.	
DRACCR	9, 8	RCD1, RCD0	00	Row Address Output State Setting (Controls wait between RAS and CAS) Sets to no wait.	
DRACCR	13, 12	TPC1, TPC0	00	Precharge State Count Setting Sets to 1 state	
ASTCR	2	AST2	0	Wait Control Setting Sets area 2 to 2-state access space with no wait.	
DRAMCR	7	BE	1	Burst Access Mode Setting Enables burst mode. Sets to RAS-up mode	4.1 (7)
DRAMCR	6	RCDM	0		
				Refresh Control Setting	4.1 (8)
RTCNT	7 to 0	—	0x00	Resets the counter.	
RTCOR	7 to 0	—	152	Sets the refresh interval to within 16 ms/1024 cycles.	
REFCR	7	RFSHE	1	Enables refresh.	
REFCR	10 to 8	RTCK2 to RTCK0	1	Counts on ϕ/2	

(2) **DRAM Space Setting**

The address space for the H8S microcomputer is divided into eight areas in units of 2 Mbytes. A bus can be set for each area. The DRAM can be connected to Areas 2 to 5. The following areas can be assigned to the DRAM space: Area 2 if the space is 2 Mbytes or less; Areas 2 to 3 if the space if 4 Mbytes or less; or Areas 2 to 5 if the space is more than 4 Mbytes and up to 8 Mbytes. The sample task in this application note uses 2-Mbyte DRAM and assigns Area 2 to the DRAM space with an available address range of 0x400000 to 0x5FFFFF.

(3) **Address Multiplexing Setting**

The DRAM space is multiplexed in terms of row and column addresses. Therefore, the amount of a row-address shift needs to be set according to the address width (memory capacity) of the DRAM to be used. Because the DRAM used in this application note has an address width of 10 bits, the row-address shift amount is also set to 10 bits.

(4) **Address Bus Setting**

To use as an address bus, the output mode must be set using the DDR register of the I/O port.

(5) **Data Bus Setting**

The data width (16 bits) for the DRAM used in the application note must be set. Note that because access is made in units of 16 bits, the least significant bit of an address is not connected, and that connections are shifted by 1 bit. (See the connection diagram in section 2, Configuration.)

(6) **Signal Timing Adjustment**

Appropriate settings must be provided according to the AC characteristic of the DRAM to be connected and the operating frequency of the microcomputer.

The figure below shows fundamental access timing.

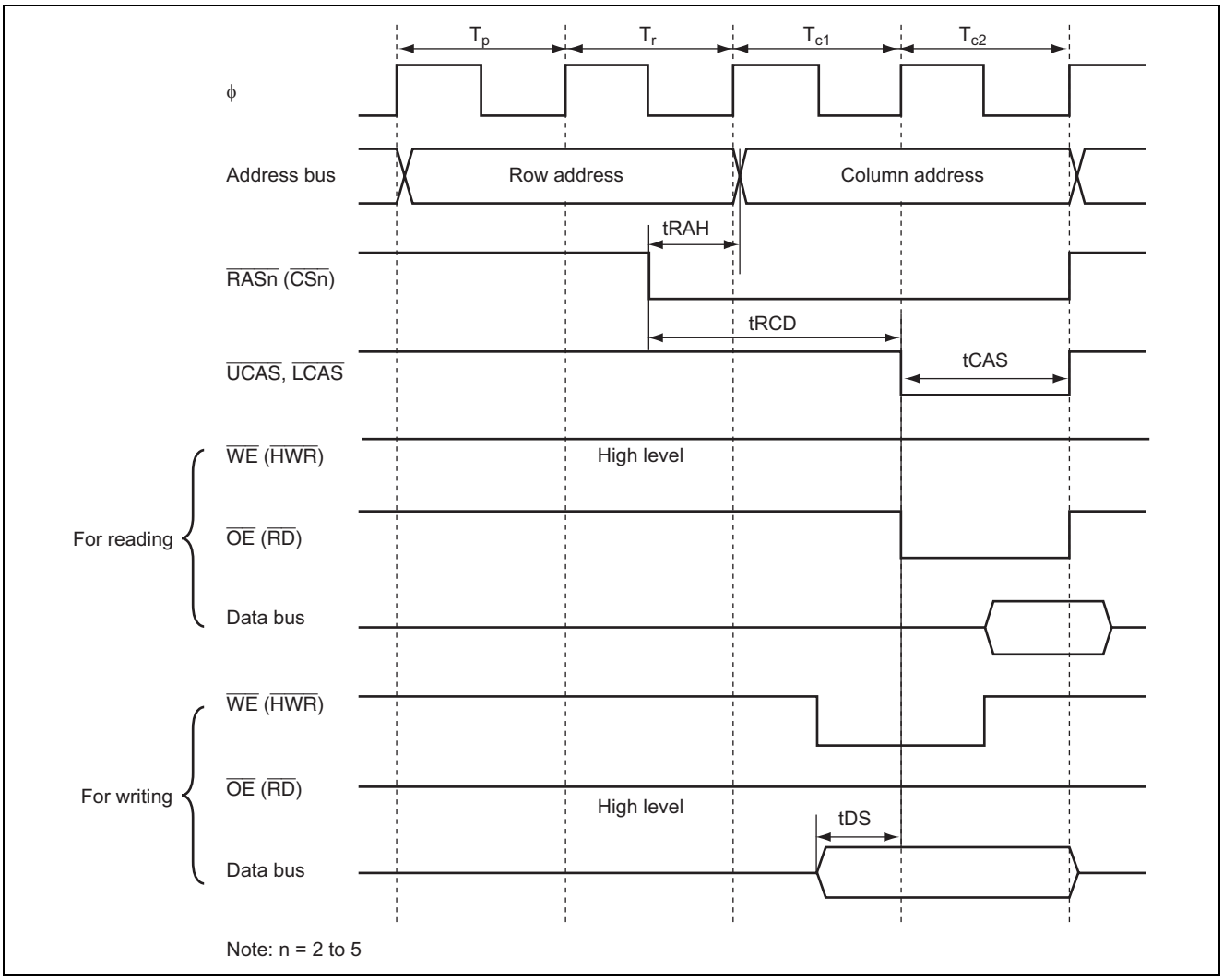


Figure 2 Fundamental Access Timing of DRAM

Symbol	Description	DRAM Specification	Microcomputer Access Timing	Register to Adjust Timing
ϕ	Access cycle	—	19.6608 MHz, 50.86 ns	—
tRAH	Row address hold time	Min. 10 ns	ϕ/2 = 25.43 ns	DRAMCR (RAST)
tRCD	Delay time between $\overline{RAS}$ and $\overline{CAS}$	Min. 14 ns	1.5ϕ = 76.29 ns	DRACCR (RCD)
tCAS	$\overline{CAS}$ pulse width	Min. 10 ns	ϕ = 50.86 ns	DRAMCR (CAST), AST (AST2)
tDS	Data-in setup time	Min. 0 ns	ϕ = 50.86 ns	AST (AST2)
Tp	Precharge time	Min. 40 ns	ϕ = 50.86 ns	DRACCR (TPC)

As indicated in the above table, the DRAM used in the application note can be accessed at fundamental access timing. If a given access timing cannot meet the DRAM specifications, it can be modified using the timing adjustment register. For details, refer to the hardware manual.

(7) **Burst Access Mode Setting**

A burst access mode can be set when connecting DRAM that supports the burst mode. The burst mode refers to a mode that permits high-speed access when identical row addresses are encountered in succession, by simply changing column addresses after the row address is output.

In the RAS-up mode, bust operations are performed only when the DRAM space is contiguous, such that if access to another external space occurs in the midst of access to the DRAM space, the burst operations cease. In the RAS-down mode, burst operations continue even if access to another external space occurs in the midst of access to the DRAM space. The figure below illustrates examples of burst mode operation timing.

Because DRAM with a fast page mode feature is used in this application note, a RAS-up mode with a burst mode will be set.

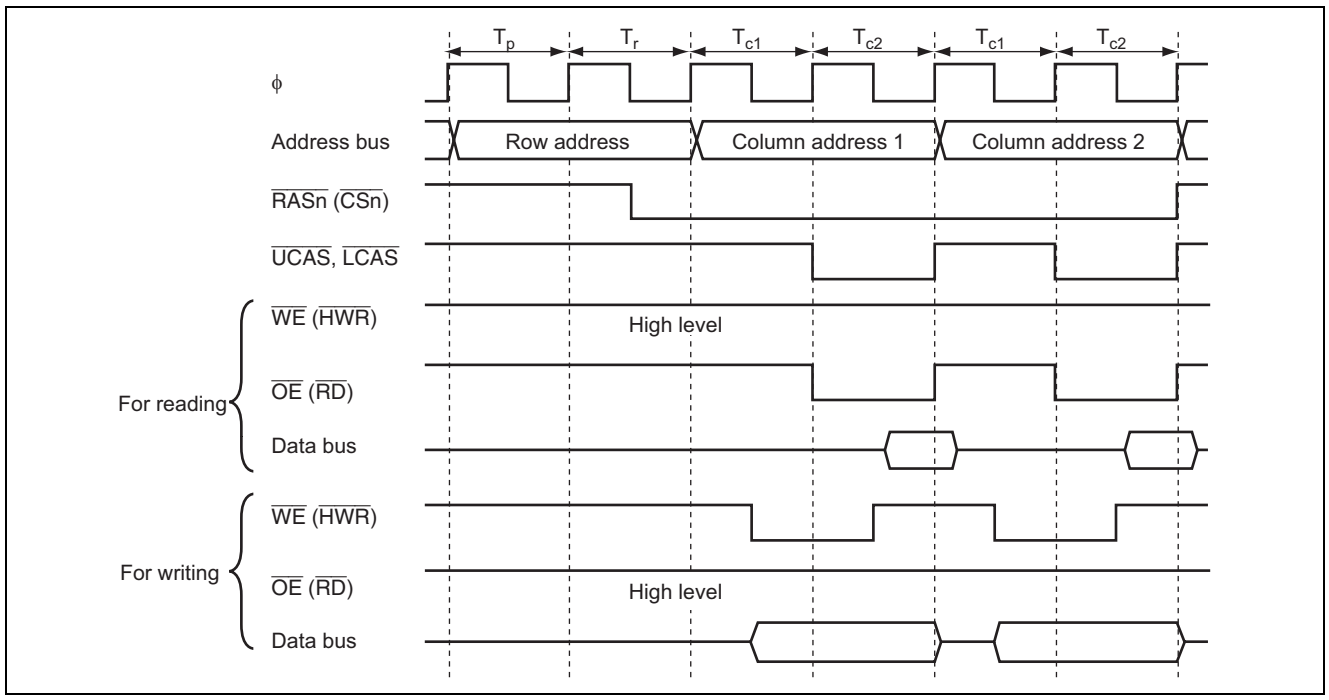


Figure 3 Burst Mode Operation Timing

(8) **Refresh Control Setting**

In accordance with DRAM specifications, a CBR refresh can be issued at fixed intervals.

The refresh interval is set to 15.563 µs in this application note.

Refreshing of DRAM:

16 ms/1024 cycles = 15.625 µs

Refresh timing in this application note:

Operating frequency 19.6608 MHz = 50.86 ns
Counting at ϕ/2, 15.625 µs/(50.86 ns × 2) ≅ 153 cycles
50.86 ns × 2 × 153 ≅ 15.563 µs
Since 15.563 µs < 15.625 µs, set the RTCOR register to 152 (153-1).

4.2 DRAM Access

The above settings enable access to the DRAM.

For this application, the DRAM space is 0x400000 to 0x5FFFFF, with an access unit of 4 bytes.

5. Description of Sample Program

5.1 File Configuration

Table 2 shows file configuration of this sample task.

Table 2 Description of Functions

File Name	Specification
resetprg.c	Executed from reset vector address 0 if the MCU is reset.
intprg.c	Executed if an interrupt other than a reset occurs.
dbsct.c	Sets start and end addresses of the section used by _INITSCT function in resetprg.c to section initialization table. For details, refer to sections 9 and 10 in the H8S, H8/300H Series C/C++ Compiler, Assembler, and Optimization Linkage Editor User's Manual.
H8S_2377_1.c	Main routine of this sample task.
Iodefine.h	Configuration definition file of internal registers.
stacksct.h	Defines stack size.

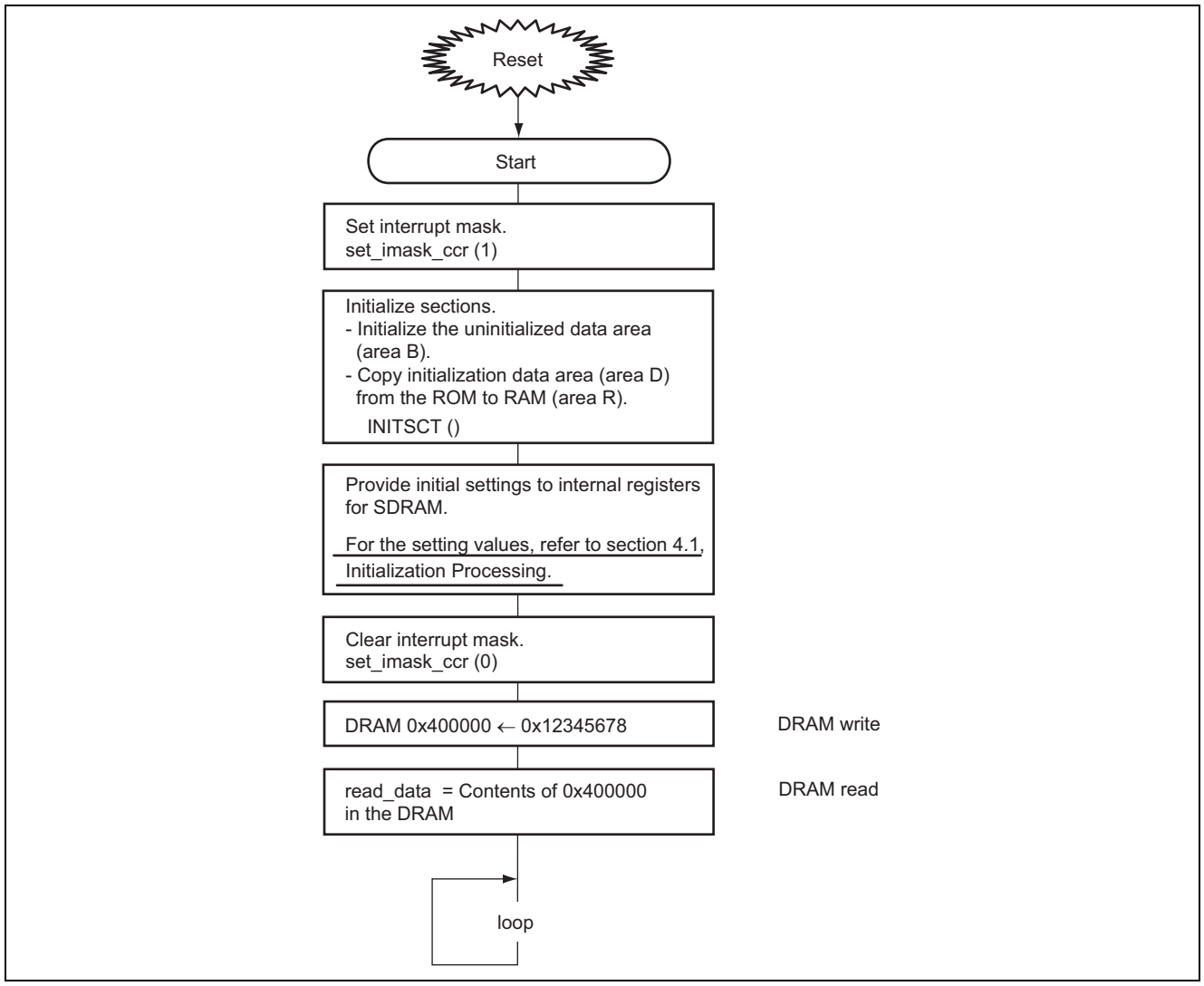
5.2 Linkage

The linkage addresses of each section are as follows.

In the HEW project files, the linkage addresses can be referenced and set by Category: section of Link/librarq tab in option – Standard Toolchain.

Section	Start Address
PResetPRG	0x000400
PIntPRG	
P	0x000800
C$DSEC	
C$BSEC	
D	
B	0xFF6000
R	
S	0xFFBDF0

6. Flowchart


Reset
Start
Set interrupt mask.
set_imask_ccr (1)
Initialize sections.
- Initialize the uninitialized data area (area B).
- Copy initialization data area (area D) from the ROM to RAM (area R).
INITSCT ()
Provide initial settings to internal registers for SDRAM.
For the setting values, refer to section 4.1, Initialization Processing.
Clear interrupt mask.
set_imask_ccr (0)
DRAM 0x400000 ← 0x12345678
DRAM write
read_data = Contents of 0x400000 in the DRAM
DRAM read
loop

References

Document Name	How to Get the Document
H8S/2378, H8S/2378R Group Hardware Manual	Download from the website of Renesas Technology Corp.

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Revision Record

		Description	
Rev.	**Date**	**Page**	**Summary**
1.00	Mar.09.05	—	First edition issued
2.00	Jun.15.07	Page 2	Correction to the DRAM refresh cycle in table 1
		Page 2	Addition of three components to table 1
		Page 2	Correction to the vocabulary used as “product code” to “Part no.”, in table 1.
		Page 2	Correction to the pin name in figure 1 from “$\overline{\text{CS2}}$” to “$\overline{\text{RAS2}}$”
		Page 3	Correction on the data size “unsigned int” to “unsigned long”, in the table
		Pages 3, 7, 9	Correction on the fixed value of address “0x400000” to “0x12345678 and an access unit to “4 bytes”
		Page 4	Correction on the content in “(1) Initial Values”
		Page 7	Correction on the content in “(8) Refresh Control Setting”
		Page 8	Deletion of URL under table 2
		Page 8	Correction on the text of “5.1 File Configuration”
		Page 9	Correction on the content in “6 Flowchart”

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