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H8/300L SLP Series

Displaying the Results of A/D Conversion on an LCD

Introduction

The results of A/D conversion from the 10-bit A/D converter of the H8/38024 are displayed on an LCD as a hexadecimal number.

Target Device

H8/38024

Contents

1. Specifications

1. The results of A/D conversion from the 10-bit A/D converter of the H8/38024 are displayed on an LCD.
2. In this sample task, a variable resistor is connected to the AN1 pin.
3. The A/D-converted value is displayed on the LCD as a hexadecimal number.
4. Figure 1.1 shows the connection of the sample task.

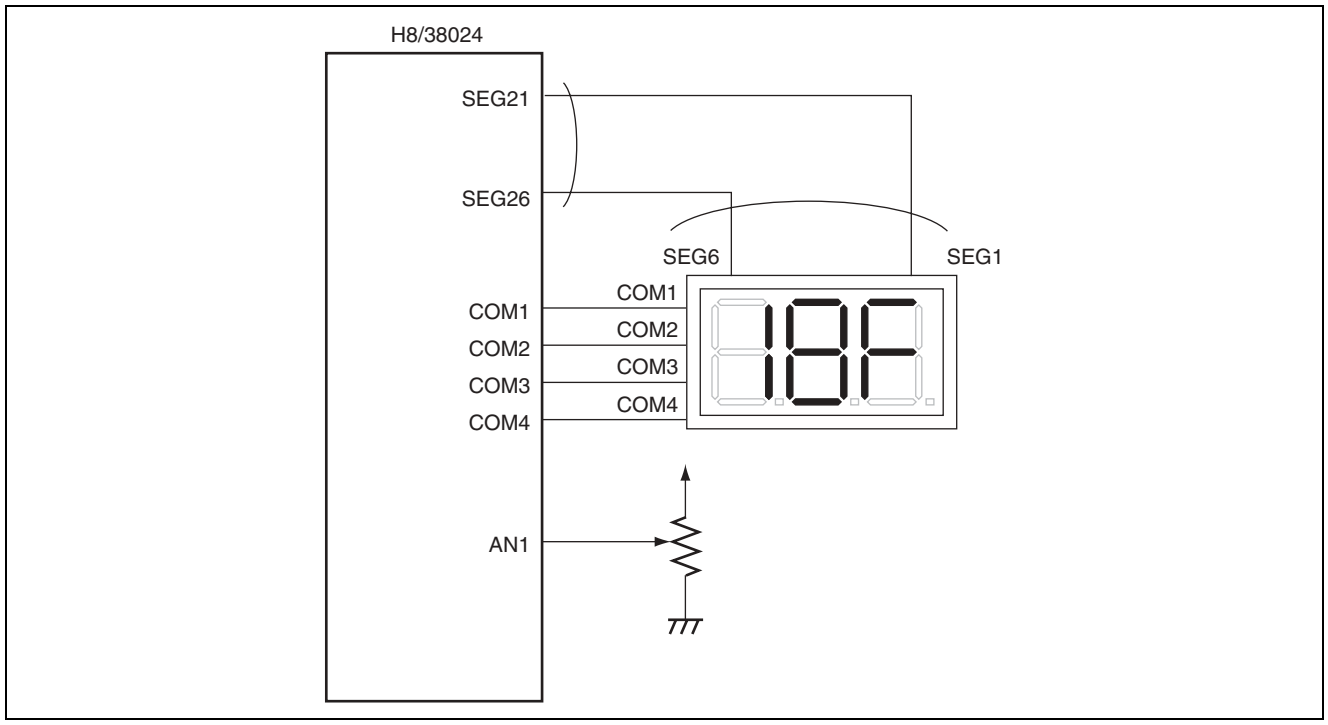


Figure 1.1 Configuration for the Sample Task

2. Description of Functions

1. This section explains the H8/38024 functions used for A/D conversion and LCD display. Figure 2.1 shows the block diagram of the functions used in this sample task.

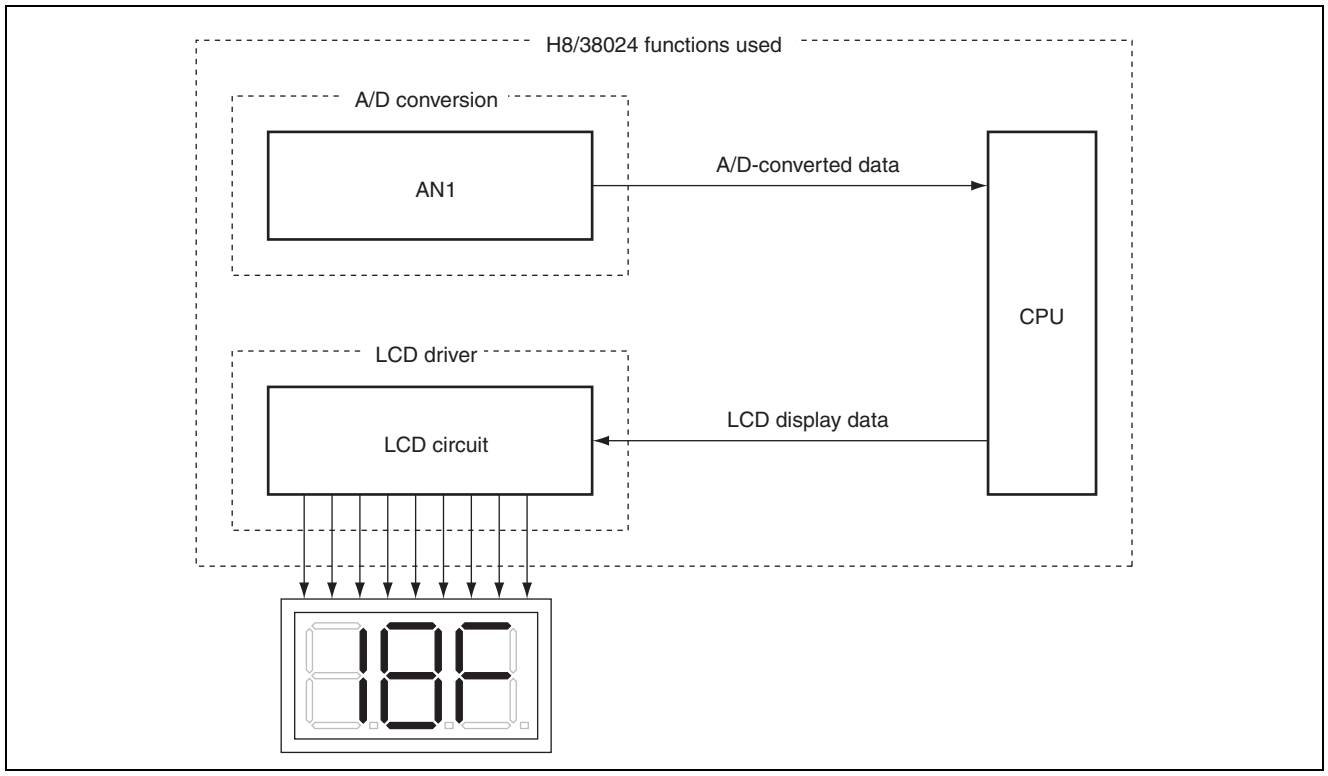


Figure 2.1 H8/38024 Functions Used

2. Figure 2.2 shows the block diagram of the LCD controller/driver used for the sample task.

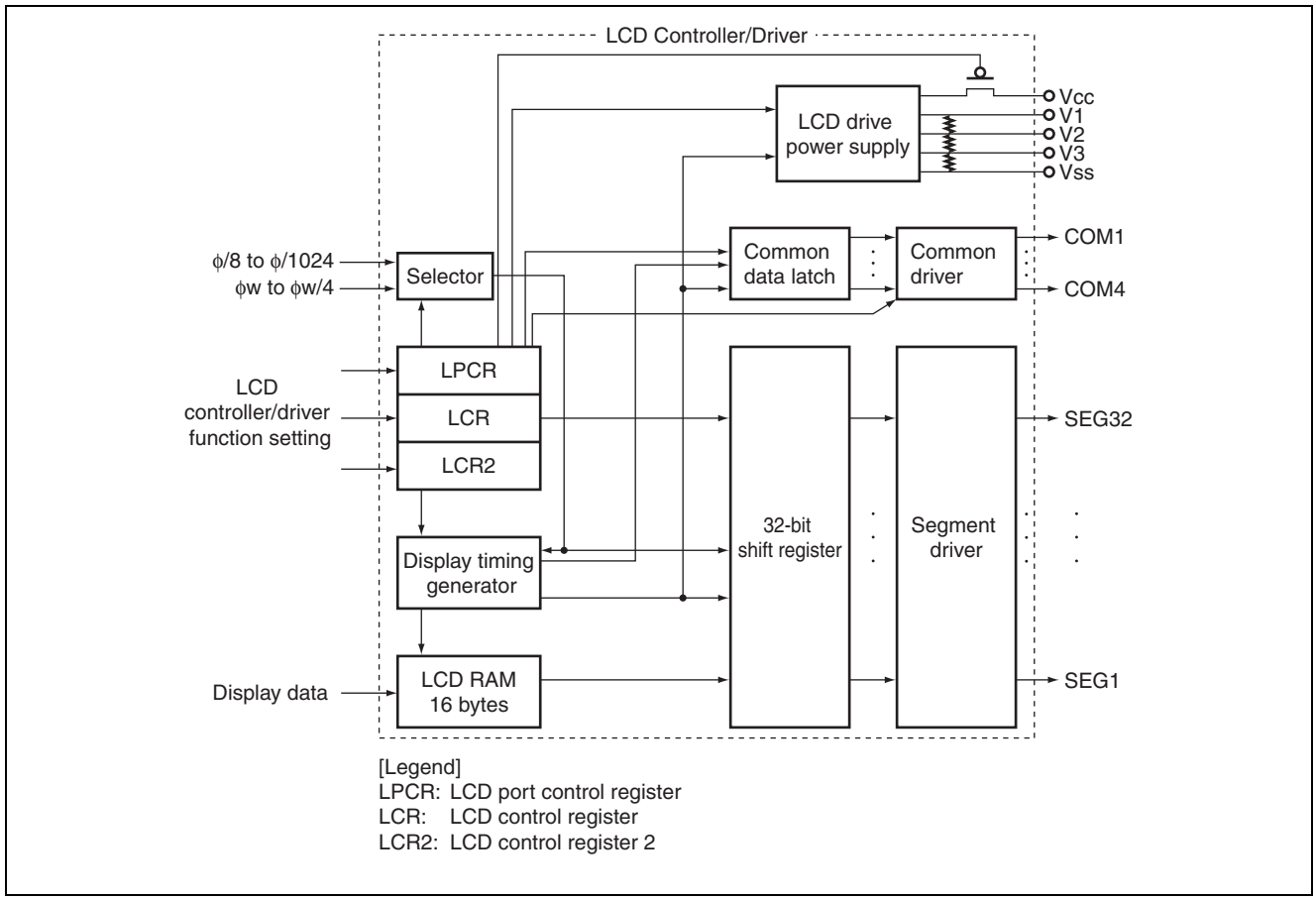


Figure 2.2 Block Diagram of LCD Controller/Driver

3. The following explains the functions supported by the LCD controller/driver.
   - LCD port control register (LPCR)
     LPCR is an 8-bit readable/writable register which selects the duty cycle, the LCD driver, and pin functions.
   - LCD control register (LCR)
     LCR is an 8-bit readable/writable register which turns on and off the LCD drive power supply, controls starting of the display function and display data, and selects the frame frequency.
   - LCD control register 2 (LCR2)
     LCR2 is an 8-bit readable/writable register which controls switching between A and B waveforms, and selects a clock for the triple step-up circuit, the drive power supply, and an appropriate duty cycle for a period during which the split-resistor is connected with the power supply circuit.
   - Segment output pins (SEG1 to SEG32)
     These are pins used for driving LCD segments; all these pins are multiplexed as port pins (setting is programmable).
   - Common output pins (COM1 to COM4)
     These are LCD common driving output pins; under static or 1/2-duty cycle driving, they can be used in parallel.
   - LCD power supply pins (V1, V2, and V3)
     These pins are used when connecting an external bypass capacitor or when using an external power supply circuit.
   - LCD RAM
     Display data is placed here. The relation between the LCD RAM and the display segments differs according to the duty cycle setting. Display is started in this way: after the registers necessary for display have been set, write data in the locations corresponding to the given duty cycle using the same instructions as those for writing to ordinary RAM, and then turn the display on. Word/byte access instructions can be used to set data in the LCD RAM.

4. Table 2.1 lists display of SEG21 and SEG22 of the 3-digit 8-segment LCD, along with sample display data.

Table 2.1 Sample Display Data

Symbol	Display	Address	Display data								
			Binary								Hexadecimal
0		0xF746	1	1	0	1	0	1	1	1	0xD7
1		0xF746	0	0	0	0	0	1	1	0	0x06
2		0xF746	1	1	1	0	0	0	1	1	0xE3
3		0xF746	1	0	1	0	0	1	1	1	0xA7
4		0xF746	0	0	1	1	0	1	1	0	0x36
5		0xF746	1	0	1	1	0	1	0	1	0xB5
6		0xF746	1	1	1	1	0	1	0	1	0xF5
7		0xF746	0	0	0	0	0	1	1	1	0x07
8		0xF746	1	1	1	1	0	1	1	1	0xF7
9		0xF746	1	0	1	1	0	1	1	1	0xB7
A		0xF746	0	1	1	1	0	1	1	1	0x77
B		0xF746	1	1	1	1	0	1	0	0	0xF4
C		0xF746	1	1	0	1	0	0	0	1	0xD1
D		0xF746	1	1	1	0	0	1	1	0	0xE6
E		0xF746	1	1	1	1	0	0	0	1	0xF1
F		0xF746	0	1	1	1	0	0	0	1	0x71

5. Figure 2.3 shows the block diagram of the A/D converter used in the sample task.

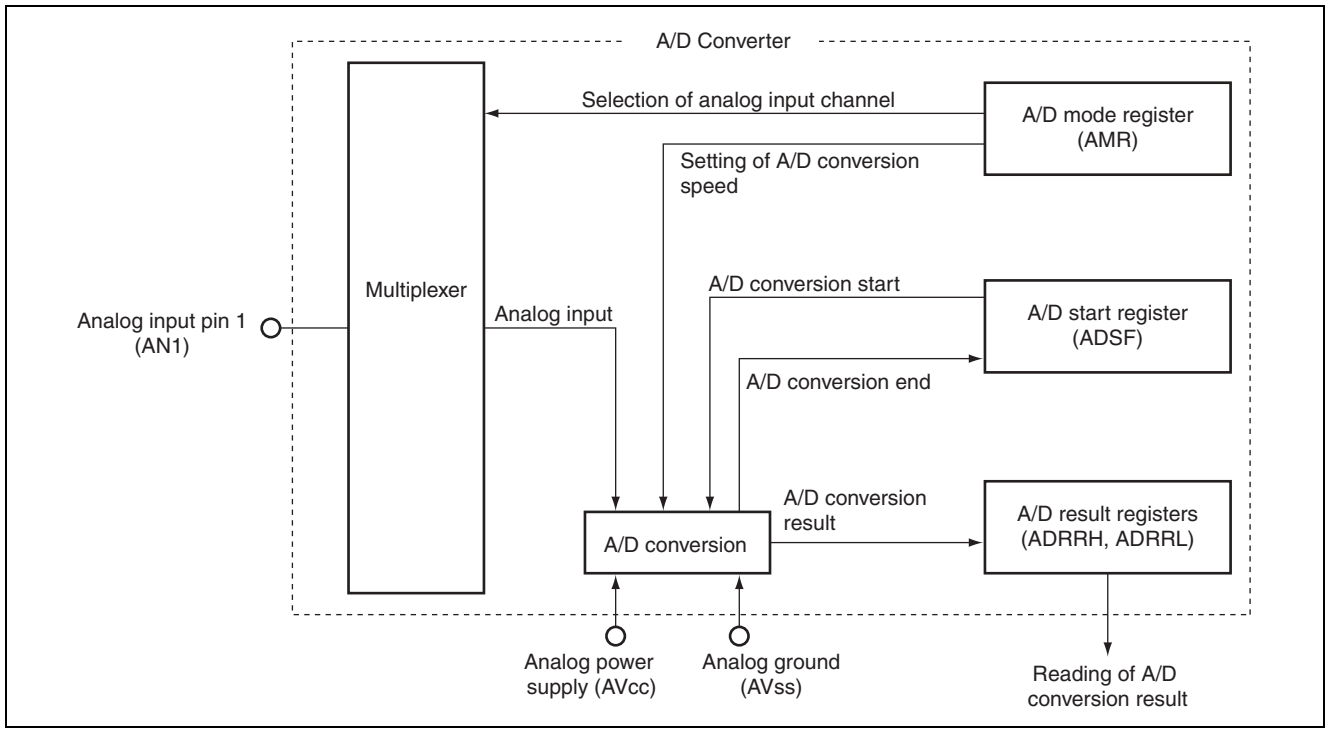


Figure 2.3 Block Diagram of A/D Converter

A. The following explains the block diagram of the A/D converter.

- A/D result registers (ADRRH and ADRRL)
  They makes up a 16-bit read-only register that stores the results of A/D conversion. The upper eight bits of 10-bit result data are stored into the ADRRH, while the lower two bits of the data are stored into bits 6 and 7 in ADRRL.
- A/D mode register (AMR)
  This is an 8-bit readable/writable register that sets an A/D conversion speed and specifies an analog input pin. In the sample task, the A/D conversion speed is set at 12.4 µs.
- A/D start register (ADSR)
  This is an 8-bit readable/writable register that specifies the start or termination of A/D conversion.
- Analog input pin 1 (AN1)
  This is the input pin for input voltage channel 1. In the sample task, an external variable resistor is connected to measure a voltage for A/D conversion.
- Analog power supply (AVCC)
  This is the pin for the analog power supply and reference voltage.
- Analog ground (AVSS)
  This is the pin for the analog ground and reference voltage.

6. Table 2.2 lists the functions assigned for the sample task. With these function assignments, the value undergone A/D conversion is displayed on the LCD.

Table 2.2 Function Assignments

Function	Function Allocation
LPCR	Selects a duty cycle, the LCD driver, and pin functions.
LCR	Turns on or off LCD drive power supply, controls the start of the display function and display data, and selects a frame frequency.
LCR2	Controls waveform A or B selection.
SEG26 to SEG21	Used as segment driver pins.
COM4 to COM1	Used as common driver pins.
LCDRAM	RAM where LCD display data is placed.
AMR	Sets the A/D conversion speed, and specifies an analog input pin.
ADSF	Specifies the start or termination of A/D conversion.
ADRRH, ADRRL	Stores the results of A/D conversion.
AN3	Input pin for input voltage channel 1
AVcc	Power supply and reference voltage pin for the analog section
AVss	Ground pin for the analog section

3. Description of Software

3.1 Modules

Table 3.1 lists the modules used for the sample task.

Table 3.1 Description of Modules

Module	Label	Function
Main routine	main	Sets global variables and PWM1, and enables the interrupt.
LCD initialization	lcd_init	Makes settings for the LCD, and clears the LCD RAM.

3.2 Arguments

The sample task uses no arguments.

3.3 Internal Registers

Table 3.2 lists the internal registers used for the sample task.

Table 3.2 Description of Internal Registers

Register		Function	Address	Setting
LPCR	DTS1 DTS0	LCD port control register (duty cycle selection 1 and 0) Selects a duty cycle from among “static”, 1/2, 1/3, and 1/4 by the settings of DTS1 and DTS0 in combination. When DTS1 = 1 and DTS0 = 1, 1/4 duty cycle is selected.	0xFFC0 Bit 7 Bit 6	DTS1 = 1 DTS0 = 1
	CMX	LCD port control register (common function selection) Selects whether the same waveform is output from several pins in order to increase the common driving capacity when common pins are not used with the given duty cycle. If CMX = 0, the same waveform is not output from multiple common pins not used with that duty cycle. If CMX = 1, the same waveform is output from multiple common pins not used with that duty cycle.	0xFFC0 Bit 5	0
LPCR	SGS3 SGS2 SGS1 SGS0	LCD port control register (segment driver selection 0 to 3) Selects a segment driver to be used. When SGS3 = 1, SGS2 = 0, SGS1 = 1, and SGS0 = 1, pins SEG13 to SEG32 function as the segment driver pins, while pins SEG1 to SEG12 function as ports.	0xFFC0 Bit 3 Bit 2 Bit 1 Bit 0	SGS3 = 1 SGS2 = 0 SGS1 = 1 SGS0 = 1
LCR	PSW	LCD control register (LCD power supply split-resistor connection control) The split-resistor for the LCD power supply can be disconnected from Vcc when LCD display is not used in power-down mode or when an external power supply is used. When ACT = 0 or in standby mode, the split-resistor for the LCD power supply is disconnected from Vcc regardless of this bit. When PSW = 0, the split-resistor for the LCD power supply is disconnected from Vcc. When PSW = 1, the split-resistor for the LCD power supply is connected to Vcc.	0xFFC1 Bit 6	1

Register		Function	Address	Setting
LCR	ACT	LCD control register (display function start) Selects whether the LCD controller/driver is to be used or not. By clearing this bit to 0, LCD controller/driver operation is halted. In addition, regardless of the value of PSW, the LCD drive power supply is turned off. However, the register contents are retained. When ACT = 0, LCD controller/driver operation is halted. When ACT = 1, LCD controller/driver operates.	0xFFC1 Bit 5	1
	DISP	LCD control register (display data control) Selects whether to display data in LCD RAM or display blank regardless of LCD RAM contents. When DISP = 0, blank is displayed. When DISP = 1, LCD RAM data is displayed.	0xFFC1 Bit 4	1
	CKS3 CKS2 CKS1 CKS0	LCD control register (frame frequency selection 0 to 3) Selects a clock to obtain a desired frame frequency. When CKS3 = 1, CKS2 = 1, CKS1 = 1, and CKS0 = 0, selects ϕ/128 as the LCD operating clock.	0xFFC1 Bit 3 Bit 2 Bit 1 Bit 0	CKS3 = 1 CKS2 = 1 CKS1 = 1 CKS0 = 0
LCR2	LCDAB	LCD control register 2 (waveform A or B select control) Selects whether to use waveform A or B as the LCD drive waveform. When LCDAB = 0, uses waveform A to drive the LCD. When LCDAB = 1, uses waveform B to drive the LCD.	0xFFC2 Bit 7	0
LCDRAM		LCDRAM Sets LCD display data.	0xF740 to 0xF74F	—
ADRRH, ADRRL		A/D result register This is a 16-bit read-only register that stores the results of A/D conversion. ADRRH stores the upper eight bits, while ADRRL stores the lower two bits.	0xFFC4 0xFFC5	—
AMR	CKS	A/D mode register (clock selection) Sets an A/D conversion speed. When CKS = 0, the conversion cycle time is 62/ϕ. When CKS = 1, the conversion cycle time is 31/ϕ.	0xFFC6 Bit 7	0
AMR	TRGE	A/D mode register (external trigger selection) Enables or disables starting of A/D conversion by an external trigger. When TRGE = 0, disables starting of A/D conversion by an external trigger. When TRGE = 1, enables starting of A/D conversion by an external trigger.	0xFFC6 Bit 6	0
	CH3 CH2 CH1 CH0	A/D mode register (channel selection 0 to 3) Selects an analog input channel. When CH3 = 0, CH2 = 1, CH1 = 0, and CH0 = 1, selects AN1 as the analog input channel.	0xFFC6 Bit 3 Bit 2 Bit 1 Bit 0	CH3 = 0 CH2 = 1 CH1 = 0 CH0 = 1
ADSR	ADSF	A/D start register (A/D start flag) When ADSF = 1, sets the start of A/D conversion. Upon the end of A/D conversion, the ADSF bit is cleared to 0.	0xFFC7 Bit 7	—

3.4 Description of RAM

The sample task does not use the RAM.

3.5 Structure and Union

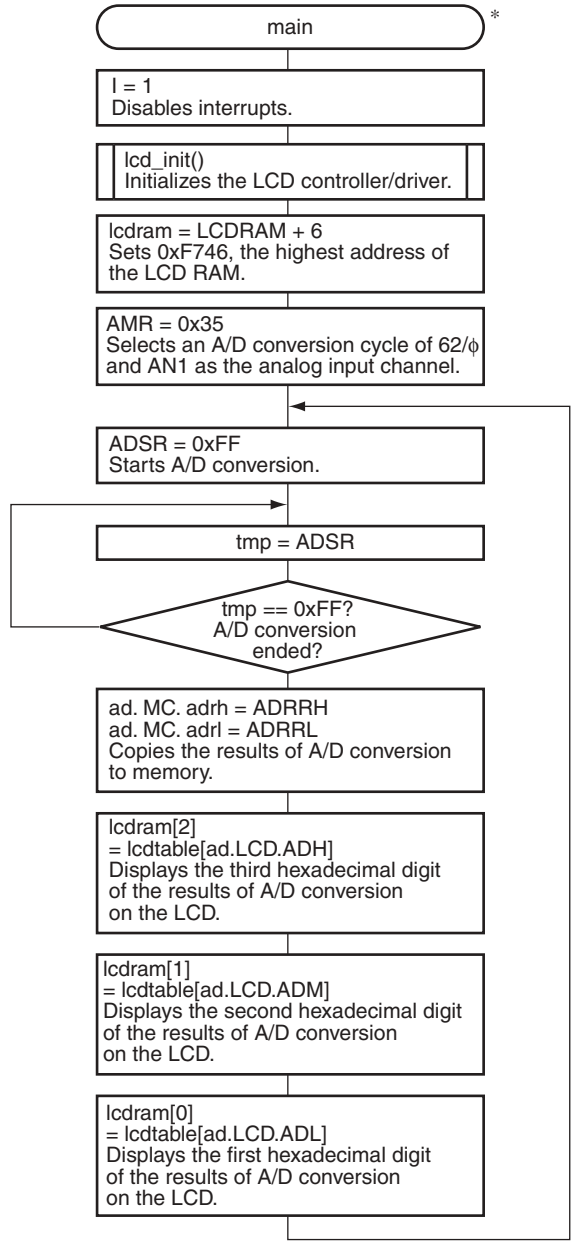
- The A/D-converted results, which are stored as the upper eight bits and lower two bits, is converted into the format of two, four, and four bits in descending order to generate the number for display on the LCD.
  Figure 3.1 illustrates the addt structure. Copying ADRRH to adrh and ADRRL to adrl reflects the data in ADH, ADM, and ADL as well.

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
addt.MC	adrh								adrl							
addt.LCD	ADH			ADM			ADL				Not used					

Figure 3.1 Description of Structure and Union

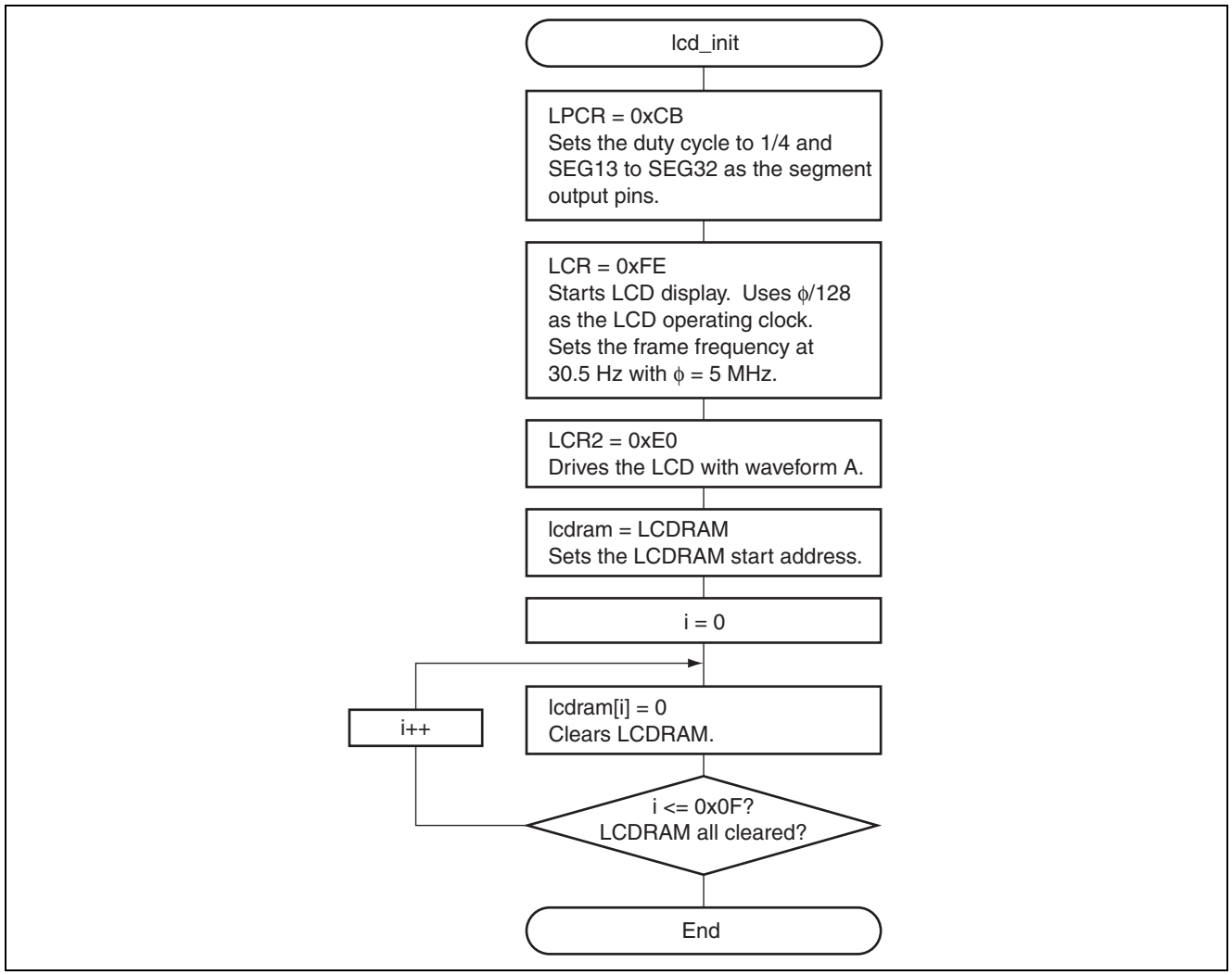
4. Flowchart

1. Main routine



Note: * In the sample task, the stack pointer is set in INIT.SRC (assembly language).

2. LCD initialization



5. Program Listing

INIT.SRC (Program listing)

```
    .EXPORT   _INIT
    .IMPORT   _main
;
    .SECTION  P,CODE
_INIT:
    MOV.W     #H'FF80,R7
    LDC.B     #B'10000000,CCR
    JMP       @_main
;
    .END
```

```
/************************************************************************************************************************/
/*                                                                                                                      */
/*  H8/300L Super Low Power Series                                                                                      */
/*      -H8/38024 Series-                                                                                               */
/*  Application Note                                                                                                    */
/*                                                                                                                      */
/*  'A/D Converter Value on LCD'                                                                                        */
/*                                                                                                                      */
/*  Function                                                                                                            */
/*  : LCD Controller / Driver                                                                                           */
/*  : A/D Converter                                                                                                     */
/*                                                                                                                      */
/*  External Clock : 10MHz                                                                                              */
/*  Internal Clock : 5MHz                                                                                               */
/*  Sub Clock      : 32.768kHz                                                                                          */
/*                                                                                                                      */
/************************************************************************************************************************/

#include    <machine.h>

/************************************************************************************************************************/
/*  Symbol Definition                                                                                                   */
/************************************************************************************************************************/
struct BIT {
    unsigned char   b7:1;       /* bit7 */
    unsigned char   b6:1;       /* bit6 */
    unsigned char   b5:1;       /* bit5 */
    unsigned char   b4:1;       /* bit4 */
    unsigned char   b3:1;       /* bit3 */
    unsigned char   b2:1;       /* bit2 */
    unsigned char   b1:1;       /* bit1 */
    unsigned char   b0:1;       /* bit0 */
};

#define     LPCR        *(volatile unsigned char *)0xFFC0       /* LCD Port Control Register               */
#define     LCR         *(volatile unsigned char *)0xFFC1       /* LCD Control Register                    */
#define     LCR2        *(volatile unsigned char *)0xFFC2       /* LCD Control Register 2                  */
#define     LCDRAM      (volatile unsigned char *)0xF740        /* LCD RAM                                 */
#define     ADRRH       *(volatile unsigned char *)0xFFC4       /* A/D Result Registers H                  */
#define     ADRRL       *(volatile unsigned char *)0xFFC5       /* A/D Result Registers L                  */
#define     AMR         *(volatile unsigned char *)0xFFC6       /* A/D Mode Register                       */
#define     ADSR        *(volatile unsigned char *)0xFFC7       /* A/D Start Register                      */
```

```
/************************************************************************************************************************/
/*  Function define                                                                                                     */
/************************************************************************************************************************/
extern void INIT ( void );                                      /* SP Set                                               */
void main( void );
void lcd_init( void );

unsigned char lcdtable[16] = {                                  /* LCD Key Select Table                                 */
    0xD7,   /* 0 */
    0x06,   /* 1 */
    0xE3,   /* 2 */
    0xA7,   /* 3 */
    0x36,   /* 4 */
    0xB5,   /* 5 */
    0xF5,   /* 6 */
    0x07,   /* 7 */
    0xF7,   /* 8 */
    0xB7,   /* 9 */
    0x77,   /* A */
    0xF4,   /* B */
    0xD1,   /* C */
    0xE6,   /* D */
    0xF1,   /* E */
    0x71,   /* F */
};

/************************************************************************************************************************/
/*  Vector Address                                                                                                      */
/************************************************************************************************************************/
#pragma section V1                                              /* Vector Section Set                                   */
void (*const VEC_TBL1[])(void) = {
    INIT                                                        /* 0x0000 Reset Vector                                  */
};

#pragma section                                                 /* P                                                    */
/************************************************************************************************************************/
/*  Main Program                                                                                                        */
/************************************************************************************************************************/
void main( void )
{
    int i;
    unsigned char *lcdram,tmp;
    union addt{
        struct {
            unsigned char adrh :8;
            unsigned char adrl :8;
        }MC;

        struct {
            unsigned char ADH :2;
            unsigned char ADM :4;
            unsigned char ADL :4;
            unsigned char     :6;
        }LCD;
    }ad;

    set_imask_ccr(1);                                           /* Interrupt Disable                                    */

    lcd_init();                                                 /* Initialize LCD                                       */
```

```
    lcdram = LCDRAM + 0x0006;                          /* Set LCDRAM Address                */

    AMR = 0x35;                                        /* AN1 Select                        */

    while (1) {
        ADSR = 0xFF;                                   /* A/D Start                         */
        do{
            tmp = ADSR;
        }while(tmp == 0xFF);                           /* Finish A/D conversion ?           */

        ad.MC.adrh = ADRRH;                            /* Copy A/D Data H                   */
        ad.MC.adrl = ADRRL;                            /* Copy A/D Data L                   */
        lcdram[2] = lcdtable[ad.LCD.ADH];              /* A/D Data 3 figures on LCD         */
        lcdram[1] = lcdtable[ad.LCD.ADM];              /* A/D Data 2 figures on LCD         */
        lcdram[0] = lcdtable[ad.LCD.ADL];              /* A/D Data 1 figures on LCD         */
    }
}

/*****************************************************************************************************************/
/*  LCD Initialize                                                                                               */
/*****************************************************************************************************************/
void lcd_init( void )
{
    unsigned char i;
    unsigned char *lcdram;

    LPCR = 0xCB;                                       /* 1/4 Duty, Select SEG32-SEG13      */
    LCR  = 0xFE;                                       /* LCD ON                            */
    LCR2 = 0xE0;                                       /* A waveform                        */

    lcdram = LCDRAM;                                   /* Set LCDRAM Address                */
    for ( i = 0; i <= 0x0F; i++ ){                     /* Initialize LCD RAM                */
        lcdram[i] = 0;
    }
}
```

Link address specifications

Section Name	Address
CV1	0x0000
P	0x0100

Revision Record

		Description	
Rev.	Date	Page	Summary
1.00	Dec.19.03	—	First edition issued

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