

To our customers,

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## Old Company Name in Catalogs and Other Documents

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April 1<sup>st</sup>, 2010  
Renesas Electronics Corporation

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# M32C/83, M32C/84 Group

## Differences between M32C/83 and M32C/84

### 1. Abstract

The following document describes differences between M32C/83 and M32C/84.

### 2. Introduction

The explanation of this issue is applied to the following condition:

Applicable MCU: M32C/83, M32C/84 Group

### 3. Contents

#### 3.1 Function Differences

Table 3.1.1 and Table 3.1.3 show the Function Differences.

**Table 3.1.1 Function Differences (1/3) (Note1)**

Item	M32C/83	M32C/84
I/O power supply	Single (VCC)	M32C/84 Double ( $VCC1 \geq VCC2$ ) M32C/84T Single ( $VCC1 = VCC2$ )
Supply Voltage	4.2V to 5.5V ( $f(BCLK)=32MHz$ ) 3.0V to 5.5V ( $f(BCLK)=20MHz$ , VDC on) 3.0V to 3.6V ( $f(BCLK)=20MHz$ , VDC off)	$VCC1=4.2V$ to $5.5V$ , $VCC2=3.0V$ to $VCC1$ ( $f(BCLK)=32MHz$ ) $VCC1=3.0V$ to $5.5V$ , $VCC2=3.0V$ to $VCC1$ ( $f(BCLK)=24MHz$ )
System Clock Protect Function	None	Have
Voltage Detection Circuit	None	M32C/84 Have M32C/84T None
Power Consumption	41mA ( $VCC=5V$ , $f(BCLK)=32MHz$ ) 26mA ( $VCC=3.3V$ , $f(BCLK)=20MHz$ ) 470 $\mu A$ ( $VCC=5V$ , $f(BCLK)=32kHz$ , in wait mode) 5.0 $\mu A$ ( $VCC=3.3V$ , $f(BCLK)=32kHz$ , VDC off, in wait mode) 0.4 $\mu A$ (in stop mode)	28mA ( $VCC1=VCC2=5V$ , $f(BCLK)=32MHz$ ) 22mA ( $VCC1=VCC2=3.3V$ , $f(BCLK)=24MHz$ ) 10 $\mu A$ ( $VCC1=VCC2=5V$ , $f(BCLK)=32kHz$ , in wait mode) 10 $\mu A$ ( $VCC1=VCC2=3.3V$ , $f(BCLK)=32kHz$ , in wait mode) 0.8 $\mu A$ (in stop mode)
Bus Wait	No wait to 3 waits (Select WCR register)	1 wait to 8 waits (Select EWCR0 to EWCR3 register)
Recovery Cycle	Not available	Available
Protect	Can be set for CM0, CM1, CM2, MCD, PLC0, PLC1, PM0, PM1, INVC0, INVC1, PD9, PS3, PLV, VDC0 register	Can be set for CM0, CM1, CM2, MCD, PLC0, PLC1, PM0, PM1, INVC0, INVC1, PD9, PS3, <u>PM2</u> , <u>VCR2</u> , <u>D4INT</u> register
Address Match Interrupt	Set in four addresses	Set in eight addresses
DMA Request Factors	Falling edge or both edges of input signals to the INT0 to INT3 pin Timer A0 to timer A4 interrupt requests Timer B0 to timer B5 interrupt requests UART0 to UART4 transmit and receive interrupt requests A/D0 conversion interrupt request A/D1 conversion interrupt request Intelligent I/O interrupt request 0 to 11 CAN interrupt request Software trigger	The next interrupt is deleted from M32C/83. A/D1 conversion interrupt request Intelligent I/O interrupt request 5 to 7

Note 1: About the details and the characteristics, refer to hardware manual.

**Table 3.1.2 Function Differences (2/3) (Note1)**

Item	M32C/83	M32C/84
Intelligent I/O	4 group	1 group
Intelligent I/O Time Measurement	12 channel (144-pin version) 5 channel (100-pin version)	8 channel (144-pin version) 8 channel (100-pin version)
Intelligent I/O Waveform Generation	28 channel (144-pin version) 10 channel (100-pin version)	8 channel (144-pin version) 8 channel (100-pin version)
Intelligent I/O Waveform Generation Mode	Single-Phase Waveform Output Mode (Group 0 to 3) Phase-Delayed Waveform Output Mode (Group 0 to 3) Set/Reset Waveform Output (SR Waveform Output) Mode (Group 0 to 3) Bit Modulation PWM Output Mode (Group 2 and 3) Real-Time Port (RTP) Output Mode (Group 2 and 3) Parallel Real-Time Port Output Mode (Group 2 and 3)	Single-Phase Waveform Output Mode  Phase-Delayed Waveform Output Mode  Set/Reset Waveform Output (SR Waveform Output) Mode
Intelligent I/O Communication Function	Clock Synchronous Serial I/O Mode Clock Asynchronous Serial I/O Mode (UART) HDLC Data Processing Mode <u>Variable Clock Synchronous Serial I/O Mode</u> <u>IEBus Mode (Note 2)</u> <u>8-bit or 16-bit Clock Synchronous Serial I/O Mode</u>	Clock Synchronous Serial I/O Mode Clock Asynchronous Serial I/O Mode (UART) HDLC Data Processing Mode
A/D Converter	2 circuit	1 circuit
A/D Converter Operating Clock	Selectable: fAD, fAD/2, fAD/3, fAD/4	Selectable: fAD, fAD/2, fAD/3, fAD/4, <u>fAD/6</u> , <u>fAD/8</u>
A/D Converter Mode	One-shot mode, repeat mode, single sweep mode, repeat sweep mode 0, repeat sweep mode 1	The next mode is added to M32C/83. <u>Multi-port single sweep mode</u> , <u>multi-port repeat sweep mode 0</u>
A/D Converter DMAC Operating Mode	None	Have
A/D Converter Two-Circuit Simultaneous Start	Have	None
A/D Converter Pin Input Replacement Function	Have	None
DRAMC	Have	None
Flash Memory Program	Per page (per 256 byte)	Per word, per byte (Note 3)
Flash Memory Rewrite Mode	CPU rewrite mode (EW mode 0 corresponding)	EW mode 0, EW mode 1
Flash Memory Boot ROM	8K bytes	4K bytes
Flash Memory Block A	None	Have (4K bytes)
Flash Memory Block	Block 0: 16K bytes Block 1: 8K bytes Block 2: 8K bytes Block 3: 32K bytes Block 4 to block 10: 64K bytes	Block 0: 4K bytes Block 1: 4K bytes Block 2: 8K bytes Block 3: 8K bytes Block 4: 8K bytes Block 5: 32K bytes Block 6 to block 12: 64K bytes

Note 1: About the details and the characteristics, refer to hardware manual.

Note 2: IEBus is a trademark of NEC Electronics Corporation.

Note 3: Programming per byte is available in parallel I/O mode only.

Table 3.1.3 Function Differences (3/3) (Note1)

Item	M32C/83	M32C/84
Flash Memory Software Command Program	“41h” is written in the first bus cycle. Data to the write address in the second bus cycle to 129th bus cycle.	“xx40h” is written in the first bus cycle. Data to the write address in the second bus cycle.
Flash Memory Software Command Read Lock Bit Status	“71h” is written in the first bus cycle. Read lock highest-order address of a block in the second bus cycle.	“xx71h” is written in the first bus cycle. “xxD0h” is written in the second bus cycle. Read the FMR16 bit in the FMR1 register.
Flash Memory Status Register	b0: Reserved bit b1: Reserved bit b2: Reserved bit <u>b3: Block status after program</u> b4: Program status b5: Erase status b6: Reserved bit <u>b7: Write state machine (WSM) status</u>	b0: Reserved bit b1: Reserved bit b2: Reserved bit <u>b3: Reserved bit</u> b4: Program status b5: Erase status b6: Reserved bit <u>b7: Sequence status</u>

Note 1: About the details and the characteristics, refer to hardware manual.

### 3.2 Pin function Differences

Table 3.2.1 and Table 3.2.2 show the Pin Function Differences.

**Table 3.2.1 Pin Function Differences (1/2)**

Pin.no			M32C/83	M32C/84	Remarks
144 Pin	100 Pin				
GP	FP	GP			
5	5	3	P92/TB2IN/TxD3/SDA3/SRxD3/ OUTC20/ IEOUT/ISTxD2	P92/TB2IN/TxD3/SDA3/SRxD3	Delete OUTC20/IEOUT/ISTxD2
6	6	4	P91/TB1IN/RxD3/SCL3/STxD3/ IEIN/ISRxD2	P91/TB1IN/RxD3/SCL3/STxD3	Delete IEIN/ISRxD2
13	-	-	P141/OUTC15	P141/INPC15/OUTC15	Add INPC15
14	-	-	P140/OUTC14	P140/INPC14/OUTC14	Add INPC14
27	20	18	P82/INT0/CANOUT/OUTC32/ISRxD3	P82/INT0/CANOUT	Add CANOUT Delete CANOUT/OUTC32/ISRxD3
28	21	19	P81/TA4IN/U/OUTC30/ISTxD3	P81/TA4IN/U/INPC15/OUTC15	Add Add INPC15/OUTC15 Delete OUTC30/ISTxD3
29	22	20	P80/TA4OUT/U/INPC02/ISRxD0/BE0IN	P80/TA4OUT/U/ISRxD0	Delete INPC02/BE0IN
30	23	21	P77/TA3IN/CANIN/INPC01/OUTC01/ISCLK0	P77/TA3IN/CAN0IN/INPC14/ OUTC14/ISCLK0	Add CAN0IN/INPC14/OUTC14 Delete CANIN/INPC01/OUTC01
31	24	22	P76/TA3OUT/CANOUT/INPC00/OUTC00/ ISTxD0/BE0OUT	P76/TA3OUT/CAN0OUT/INPC13/ OUTC13/ISTxD0	Add CAN0OUT/INPC13/OUTC13 CANOUT/INPC00/OUTC00/ Delete BE0OUT
34	27	25	P73/TA1IN/V/CTS2/RTS2/SS2/ OUTC10/ISTxD1/BE1OUT	P73/TA1IN/V/CTS2/RTS2/SS2/INPC10/ OUTC10/ISTxD1/BE1OUT	Add INPC10
36	29	27	P71/TB5IN/TA0IN/RxD2/SCL2/STxD2/ OUTC22/ISRxD2/IEIN	P71/TB5IN/TA0IN/RxD2/SCL2/STxD2/ INPC17/OUTC17	Add INPC17/OUTC17 Delete OUTC22/ISRxD2/IEIN
37	30	28	P70/TA0OUT/TxD2/SDA2/SRxD2/OUTC20/ ISTxD2/IEOUT	P70/TA0OUT/TxD2/SDA2/SRxD2/ INPC16 /OUTC16	Add INPC16/OUTC16 Delete OUTC20/ISTxD2/IEOUT
43	34	32	P64/CTS1/RTS1/SS1/OUTC21/ISCLK2	P64/CTS1/RTS1/SS1	Delete OUTC21/ISCLK2
48	-	-	P137/OUTC27	P137	Delete OUTC27
49	-	-	P136/OUTC21/ISCLK2	P136	Delete OUTC21/ISCLK2
50	-	-	P135/OUTC22/ISRxD2/IEIN	P135	Delete OUTC22/ISRxD2/IEIN
51	-	-	P134/OUTC20/ISTxD2/IEOUT	P134	Delete OUTC20/ISTxD2/IEOUT
53	40	38	P56/ALE/RAS	P56/ALE	Delete RAS
56	-	-	P133/OUTC23	P133	Delete OUTC23
58	-	-	P132/OUTC26	P132	Delete OUTC26
60	-	-	P131/OUTC25	P131	Delete OUTC25
61	-	-	P130/OUTC24	P130	Delete OUTC24
63	44	42	P52/RD/DW	P52/RD	Delete DW
64	45	43	P51/WRH/BHE/CASH	P51/WRH/BHE	Delete CASH
65	46	44	P50/WRL/WR/CASL	P50/WRL/WR	Delete CASL
66	-	-	P127/OUTC37	P127	Delete OUTC37
67	-	-	P126/OUTC36	P126	Delete OUTC36
68	-	-	P125/OUTC35	P125	Delete OUTC35
72	50	48	P44/CS3/A20(MA12)	P44/CS3/A20	Delete MA12
73	51	49	P43/A19(MA11)	P43/A19	Delete MA11
75	52	50	P42/A18(MA10)	P42/A18	Delete MA10
77	53	51	P41/A17(MA9)	P41/A17	Delete MA9
78	54	52	P40/A16(MA8)	P40/A16	Delete MA8
79	55	53	P37/A15(MA7)(/D15)	P37/A15(/D15)	Delete MA7

Table 3.2.2 Pin Function Differences (2/2)

Pin.no			M32C/83	M32C/84	Remarks
144 Pin	100 Pin				
GP	FP	GP			
80	56	54	P36/A14(MA6)/(D14)	P36/A14/(D14)	Delete MA6
81	57	55	P35/A13(MA5)/(D13)	P35/A13/(D13)	Delete MA5
82	58	56	P34/A12(MA4)/(D12)	P34/A12/(D12)	Delete MA4
83	59	57	P33/A11(MA3)/(D11)	P33/A11/(D11)	Delete MA3
84	60	58	P32/A10(MA2)/(D10)	P32/A10/(D10)	Delete MA2
85	61	59	P31/A9(MA1)/(D9)	P31/A9/(D9)	Delete MA1
86	-	-	P124/OUTC34	P124	Delete OUTC34
87	-	-	P123/OUTC33	P123	Delete OUTC33
88	-	-	P122/OUTC32/ISRxD3	P122	Delete OUTC32/ISRxD3
89	-	-	P121/OUTC31/ISCLK3	P121	Delete OUTC31/ISCLK3
90	-	-	P120/OUTC30/ISTxD3	P120	Delete OUTC30/ISTxD3
92	63	61	P30/A8(MA0)/(D8)	P30/A8/(D8)	Delete MA0
115	-	-	P113/OUTC13	P113/INPC13/OUTC13	Add INPC13
118	-	-	P110/OUTC10/STxD1/BE1OUT	P110/INPC10/OUTC10/STxD1/BE1OUT	Add INPC10
123	-	-	P157/INPC07/AN157	P157/AN157	Delete INPC07
124	-	-	P156/INPC06/AN156	P156/AN156	Delete INPC06
125	-	-	P155/INPC05/OUTC05/AN155	P155/AN155	Delete INPC05
126	-	-	P154/INPC04/OUTC04/AN154	P154/AN154	Delete INPC04
127	-	-	P153/INPC03/AN153	P153/AN153	Delete INPC03
128	-	-	P152/INPC02/ISRxD0/BE0IN/AN152	P152/ISRxD0/AN152	Delete INPC02/BE0IN
129	-	-	P151/INPC01/OUTC01/ISCLK0/AN151	P151/ISCLK0/AN151	Delete INPC01/OUTC01
131	-	-	P150/INPC00/OUTC00/ISTxD0/BE0OUT/AN150	P150/ISTxD0/AN150	Delete INPC00/OUTC00/BE0OUT

### 3.3 SFR Differences

Table 3.3.1 and Table 3.3.3 show the SFR Differences.

**Table 3.3.1 SFR Differences (1/3)**

M32C/83	M32C/84	Remarks
PM1	PM1	Delete bit 3. Add reserved bit (bit 6)
CM0	CM0	Change function (bit3)
WCR	-	
AIER	AIER	Add bits 4 to 7
PRCR	PRCR	Change function (bits 1, 3)
WDC	WDC	Add bit 5
-	PM2	
-	VCR2	
PLV	-	
-	VCR1	
VDC0	-	
PLC0	PLC0	Add reserved bit (bit 3), Change set value (bit 6). Address change from 0376h to 0026h.
PLC1	PLC1	Change function (bit 1). Add reserved bit (bits 4 to 7). Address change from 0377h to 0027h.
-	RMAD4	
-	RMAD5	
-	D4INT	
-	RMAD6	
-	RMAD7	
DRAMCONT	-	
REFCNT	-	
-	EWCR0	
-	EWCR1	
-	EWCR2	
-	EWCR3	
-	PWCR0	
-	PWCR1	
-	FMR1	
FMR0	FMR0	Change function (bit 3). Add bits 6, 7.
IIO6IC	-	
IIO11IC/CAN2IC	CAN2IC	Delete IIO11IC.
AD1IC	-	
IIO5IC	-	
IIO7IC	-	
IIO0IR to IIO4IR	IIO0IR to IIO4IR	Change function.
IIO5IR to IIO7IR	-	
IIO8IR to IIO11IR	IIO8IR to IIO11IR	Change function.
IIO0IE to IIO4IE	IIO0IE to IIO4IE	Change function.
IIO5IE to IIO7IE	-	
IIO8IE to IIO11IE	IIO8IE to IIO11IE	Change function.



**Table 3.3.2 SFR Differences (2/3)**

M32C/83	M32C/84	Remarks
G0TM0 to G0TM7	-	
G0PO0 to G0PO7 G2PO0 to G2PO7 G3PO0 to G3PO7	-	
G0POCR0 to G0POCR7 G2POCR0 to G2POCR7 G3POCR0 to G3POCR7	-	
G1POCR0 to G1POCR7	G1POCR0 to G1POCR7	Add bit 6
G0TMCR0 to G0TMCR7	-	
G0BT, G2BT, G3BT	-	
G0BCR0, G0BCR1 G2BCR0, G2BCR1 G3BCR0, G3BCR1	-	
G1BCR1	G1BCR1	Delete bits 0, 7.
BTSR	-	
G0TPR6, G0TPR7	-	
G0FE, G2FE, G3FE	-	
G2RTP, G3RTP	-	
G0FS	-	
G0RB, G1RB	G0RB, G1RB	Add bit 14.
G0MR	G0MR	Change function (bits 0, 1). Delete bit 3.
G1MR	G1MR	Add bits 4, 5
G2MR, G3MR	-	
G2CR, G3CR	-	
G2TB, G3TB	-	
G2RB, G3RB	-	
IEAR	-	
IECR	-	
IETIF	-	
IERIF	-	
IPS	IPS	Change function (bits 0, 1). Delete bits 4 to 7.
-	IPSA	
-	CCS	
G0EMR	G0EMR	Delete bit 0.
G0IRF	G0IRF	Add reserved bit (bits 0, 1). Delete bit 3.
G1IRF	G1IRF	Add reserved bit (bits 0, 1).
G0ETC	G0ETC	Delete bits 3, 5.
G3MK4 to G3MK7	-	
G3FLG	-	
AD10 to AD17	-	
AD1CON2	-	
AD1CON0	-	
AD1CON1	-	
-	C0EFR	
-	C0MDR	
-	C0SSCTLR	
-	C0SSSTR	

**Table 3.3.3 SFR Differences (3/3)**

M32C/83	M32C/84	Remarks
AD00 to AD07	AD00 to AD07	Change function in 8 bit mode (bits 8, 9)
-	AD0CON4	
-	AD0CON3	
AD0CON2	AD0CON2	Add bits 1, 2. Change set value to reserved bit (bit 3). Delete bits 4, 6, 7.
PS9	PS9	Change function (bits 0, 1). Delete bits 4, 5.
-	PSD1	
-	PSC2	
-	PSC3	
PSC	PSC	Change function (bits 0, 1, 6).
PS1	PS1	Change function (bit 7).
PSL0	PSL0	Change function (bit 4).
PSL1	PSL1	Change function (bit 7).
PS3	PS3	Change function (bit 6).
PSL2	PSL2	Change function (bits 1, 2).
PSL3	PSL3	Change function (bit 2).
PS6	-	
PS7	-	
PCR	PCR	Add reserved bit (bits 1, 2).

### 3.4 Interrupt Vector Differences

Table 3.4.1 shows the Fixed Vector Table Differences. Table 3.4.2 shows the Relocatable Vector Table Differences.

**Table 3.4.1 Fixed Vector Table Differences**

M32C/83 Interrupt Factor	M32C/84 Interrupt Factor	Remarks
Watchdog Timer Oscillation Stop Detection	Watchdog Timer Oscillation Stop Detection Low Voltage Detection	Add Low Voltage Detection

**Table 3.4.2 Relocatable Vector Table Differences**

M32C/83 Interrupt Factor	M32C/84 Interrupt Factor	Software Interrupt Number
A/D1	-	7
Intelligent I/O Interrupt 5	-	49
Intelligent I/O Interrupt 6	-	50
Intelligent I/O Interrupt 7	-	51
Intelligent I/O Interrupt 11, CAN2	CAN2	57

### 3.5 I/O Port Power Supply Voltage Differences

Power supplies which relate to the external bus pins are separated as VCC2, thus they can be interfaced using the different voltage as VCC1. Table 3.5.1 shows I/O Port Power Supply Voltage Differences

**Table 3.5.1 I/O Port Power Supply Voltage Differences**

	M32C/83 I/O Port Power Supply Voltage	M32C/84 I/O Port Power Supply Voltage
P0 to P5, P11 to P13	VCC	VCC2
P6 to P10, P14 to P15	VCC	VCC1

### 3.6 Support Tool Differences

Table 3.6.1 shows the support tool differences.

**Table 3.6.1 Support Tool Differences**

Tool information	M32C/83 Tool Product	M32C/84 Tool Product
C Compiler	M3T-NC308WA	M3T-NC308WA
Real-time OS	M3T-MR308	M3T-MR308
Simulator Debugger	M3T-PD308SIM	M3T-PD308SIM
Emulator Debugger	M3T-PD308F	M3T-PD308F
Emulator	PC7501	PC7501
Emulation Probe	M30830T-EPB	M30850T-EPB
Compact Emulator	M30830T-CPE (Sunny Giken Inc.)	M30850T2-CPE

#### 4. Reference

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Hardware Manual

M32C/84 Group Hardware Manual

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User's Manual

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## REVISION HISTORY

Rev.	Date	Description	
		Page	Summary
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