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April 1st, 2010
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M16C/64 Group, M16C/64A Group

Difference between M16C/64 and M16C/64A

1. Abstract

The following document describes differences between M16C/64 and M16C/64A. Refer to each device's hardware manual for details.

2. Introduction

The explanation of this application note is applied to the following MCUs:

Applicable MCUs: M16C/64, M16C/64A

3. Differences

3.1 Differences in Functions

Table 3.1 lists Differences in Function.

Table 3.1 Differences in Functions (1)

Item		M16C/64	M16C/64A
Voltage Detection		2 voltage detection points	3 voltage detection points
Clock Generator	CLKOUT pin (2)	High is output in stop mode	State of the pin prior to entering stop mode is retained
Reset	Power-on reset	No	Yes
Programmable I/O Ports	$\overline{\text{NMI}}$/$\overline{\text{SD}}$ digital filter	No	The digital filter can be enabled/disabled by setting the NMIDF register
	Unassigned pin handling	VREF: Connect to VCC1	VREF: Connect to VSS
Timer	Timer A	Timer mode, Event counter mode, One-shot timer mode, Pulse width modulation (PWM) mode	Timer mode, event counter mode, one-shot timer mode, pulse width modulation (PWM) mode, programmable output mode
	Timer B	Pulse period/pulse width measurement modes: Counter value can not be read	Pulse period/pulse width measurement modes: Counter value can be read
	Real-time clock	No	Count: second, minute, hour, day of the week
	PWM function	No	8 bits x 2
	Remote control signal receive function	No	2 circuits
Serial Interface	Multi-master I^2C-bus interface	No	1 channel
	CEC function	No	Yes
A/D Converter	Open-circuit detection assist function	No	Yes
	ADST bit when using external trigger	The bit becomes 0 when A/D conversion is completed.	The bit remains 1 when A/D conversion is completed.
CRC Calculator	Generator polynomial	CRC-CCITT ($X^{16} + X^{12} + X^5 + 1$)	Selectable from CRC-CCITT ($X^{16} + X^{12} + X^5 + 1$) and CRC-16 ($X^{16} + X^{15} + X^2 + 1$)
	CRC snoop	No	Yes
Debug Function		Clock synchronous serial I/O (7-wire system)	Clock asynchronous serial I/O (2-wire system)
Supply Voltage		Power supply to VCC1 and VCC2 must be the same.	Power supply to VCC1 can be different from VCC2.

Notes:
1. Refer to the hardware manual for electrical characteristics and more details.
2. When f1, f8, or f32 is selected in single-chip mode.

3.2 Pin Characteristics

Table 3.2 lists Differences in Pin Characteristics.

Table 3.2 Differences in Pin Characteristics

M16C/64	M16C/64A	Changes from M16C/64
P9_4/TB4IN/DA1	P9_4/TB4IN/DA1/PWM1	Added: PWM1
P9_3/TB3IN/DA0	P9_3/TB3IN/DA0/PWM0	Added: PWM0
P9_2/TB2IN/SOUT3	P9_2/TB2IN/SOUT3/PMC0	Added: PMC0
P9_1/TB1IN/SIN3	P9_1/TB1IN/SIN3/PMC1	Added: PMC1
P8_5/$\overline{\text{NMI}}$/$\overline{\text{SD}}$	P8_5/$\overline{\text{NMI}}$/$\overline{\text{SD}}$/CEC	Added: CEC
P7_1/TA0IN/TB5IN/RXD2/SCL2	P7_1/TA0IN/TB5IN/RXD2/SCL2/SCLMM	Added: SCLMM
P7_0/TA0OUT/TXD2/SDA2	P7_0/TA0OUT/TXD2/SDA2/SDAMM	Added: SDAMM
P6_0/$\overline{\text{CTS0}}$/$\overline{\text{RTS0}}$	P6_0/$\overline{\text{CTS0}}$/$\overline{\text{RTS0}}$/RTCOUT	Added: RTCOUT
P4_7/$\overline{\text{CS3}}$/TXD7/SDA7	P4_7/$\overline{\text{CS3}}$/PWM1/TXD7/SDA7	Added: PWM1
P4_6/$\overline{\text{CS2}}$/RXD7/SCL7	P4_6/$\overline{\text{CS2}}$/PWM0/RXD7/SCL7	Added: PWM0
P1_7/$\overline{\text{INT5}}$/D15	P1_7/$\overline{\text{INT5}}$/D15/IDU	Added: IDU
P1_6/$\overline{\text{INT4}}$/D14	P1_6/$\overline{\text{INT4}}$/D14/IDW	Added: IDW
P1_5/$\overline{\text{INT3}}$/D13	P1_5/$\overline{\text{INT3}}$/D13/IDV	Added: IDV

4. Detailed Comparison

4.1 Differences in Protections

Table 4.1 lists Differences in Registers Associated with Protect Function.

Table 4.1 Differences in Registers Associated with Protect Function

Symbol	Address		Bit	Differences	
	M16C/64	M16C/64A		M16C/64	M16C/64A
PRCR	000Ah	000Ah	3	Protect bit 3 Enable write access to registers VCR2, D4INT, and VW0C	Protect bit 3 Enable write access to registers VCR2, VWCE, VD1LS, VW0C, VW1C, and VW2C

4.2 Differences in Resets

Table 4.2 lists Differences in Resets and Table 4.3 lists Differences in Registers Associated with Resets.

Table 4.2 Differences in Resets

Item	M16C/64	M16C/64A
Types of resets	Hardware reset 1 Software reset Watchdog timer reset Oscillation stop detection reset Brown-out reset	Hardware reset Software reset Watchdog timer reset Oscillator stop detect reset Voltage monitor 0 reset Voltage monitor 1 reset Voltage monitor 2 reset Power-on reset

Table 4.3 Differences in Registers Associated with Resets

Symbol	Address		Bit	Differences	
	M16C/64	M16C/64A		M16C/64	M16C/64A
RSTFR	0018h	0018h	1	Reserved bits	Hardware reset detection flag 0: Not detected 1: Detected
			2		Software reset detection flag 0: Not detected 1: Detected
			3		Watchdog timer reset detect flag 0: Not detected 1: Detected
			4		Voltage monitor 1 reset detection flag 0: Not detected 1: Detected
			5		Voltage monitor 2 reset detection flag 0: Not detected 1: Detected
			6		Oscillator stop detect reset detection flag 0: Not detected 1: Detected

4.3 Differences in Voltage Detectors

Table 4.4 lists Differences in Voltage Detectors and Table 4.5 lists Differences in Registers Associated with Voltage Detectors.

Table 4.4 Differences in Voltage Detectors

Item	M16C/64	M16C/64A
Voltage detection interrupt monitor level	Vdet2 (low-voltage detection circuit)	• Vdet1 (voltage detector 1) • Vdet2 (voltage detector 2)
Voltage detection reset monitor level	Vdet0 (voltage detection 0 circuit)	• Vdet0 (voltage detector 0) • Vdet1 (voltage detector 1) • Vdet2 (voltage detector 2)
Sampling clock	Selectable from CPU Clock and fOCO-S	fOCO-S

Refer to the hardware manual and electric characteristics for the detection voltage.

Table 4.5 Differences in Registers Associated with Voltage Detectors

Symbol	Address		Bit	Differences	
	M16C/64	M16C/64A		M16C/64	M16C/64A
VCR2	001Ah	001Ah	6	Reserved bit	Voltage detector 1 enable bit 0: Voltage detector 1 disabled 1: Voltage detector 1 enabled
D4INT	001Fh	—	—	M16C/64 only	—
VWCE	—	0026h	—	—	M16C/64A only
VD1LS	—	0028h	—	—	M16C/64A only
VW1C	—	002Bh	—	—	M16C/64A only
VW2C	—	002Ch	—	—	M16C/64A only
OFS1	FFFFFh	FFFFFh	5	Reserved bits Set to 1.	Vdet0 select bit 1 0: 2.85 V (Vdet0_2) 1: 1.90 V (Vdet0_0)
			6		Voltage detector 0 start bit 0: Voltage monitor 0 reset enabled after hardware reset. 1: Voltage monitor 0 reset disabled after hardware reset.

4.4 Differences in Clock Generator

Table 4.6 lists Differences in Clock Generators and Table 4.7 lists Differences in Registers Associated with Clock Generator.

Table 4.6 Differences in Clock Generators

Item	M16C/64	M16C/64A
Clock output function	Selectable from f8, f32, and fC	Selectable from f1, f8, f32, and fC
CLKOUT pin (1)	High is output in stop mode	State of the pin prior to entering stop mode is retained

Note:
1. When f1, f8, or f32 is selected in single-chip mode.

Table 4.7 Differences in Registers Associated with Clock Generator

Symbol	Address		Bit	Differences	
	M16C/64	M16C/64A		M16C/64	M16C/64A
CM1	0007h	0007h	3	Reserved bit	XIN-XOUT feedback resistor select bit 0: Internal feedback resistor connected 1: Internal feedback resistor not connected
PCLKR	0012h	0012h	5	Reserved bit	Clock output function expansion bit (enabled in single-chip mode) 0: Selected by bits CM01 to CM00 in the CM0 register 1: Output f1
PM2	001Eh	001Eh	0	Specifying wait when accessing SFR at PLL operation 0: 2 waits 1: 1 wait	Reserved bit Set to 1.

4.5 Differences in Programmable I/O Ports

Table 4.8 lists Differences in Programmable I/O Ports and Table 4.9 lists Differences in Registers Associated with Programmable I/O Ports.

Table 4.8 Differences in Programmable I/O Ports

Item	M16C/64	M16C/64A
$\overline{\text{NMI}}$/$\overline{\text{SD}}$ digital filter	No	The digital filter can be enabled/disabled by setting the NMIDF register
Unassigned pin handling	VREF: Connect to VCC1	VREF: Connect to VSS

Table 4.9 Differences in Registers Associated with Programmable I/O Ports

Symbol	Address		Bit	Differences	
	M16C/64	M16C/64A		M16C/64	M16C/64A
PCR	0366h	0366h	4	Reserved bit	CEC output enable bit 0: CEC output disabled 1: CEC output enabled
NMIDF	—	0369h	—	—	M16C/64A only

4.6 Differences in Interrupts

Table 4.10 to Table 4.11 list Differences in Interrupt Vectors, and Table 4.12 lists Differences in Registers Associated with Interrupt.

Table 4.10 Differences in Interrupt Vectors - (1/2)

Software Interrupt Number	Vector Address	M16C/64	M16C/64A
0	+0 to +3 (0000h to 0003h)	BRK instruction	BRK instruction
1	+4 to +7 (0004h to 0007h)	— (Reserved)	INT instruction interrupt
2	+8 to +11 (0008h to 000Bh)	$\overline{\text{INT7}}$	$\overline{\text{INT7}}$
3	+12 to +15 (000Ch to 000Fh)	$\overline{\text{INT6}}$	$\overline{\text{INT6}}$
4	+16 to +19 (0010h to 0013h)	$\overline{\text{INT3}}$	$\overline{\text{INT3}}$
5	+20 to +23 (0014h to 0017h)	Timer B5	Timer B5
6	+24 to +27 (0018h to 001Bh)	Timer B4, UART1 start/stop condition detection, bus collision detection	Timer B4, UART1 start/stop condition detection, bus collision detection
7	+28 to +31 (001Ch to 001Fh)	Timer B3, UART0 start/stop condition detection, bus collision detection	Timer B3, UART0 start/stop condition detection, bus collision detection
8	+32 to +35 (0020h to 0023h)	SI/O4, $\overline{\text{INT5}}$	SI/O4, $\overline{\text{INT5}}$
9	+36 to +39 (0024h to 0027h)	SI/O3, $\overline{\text{INT4}}$	SI/O3, $\overline{\text{INT4}}$
10	+40 to +43 (0028h to 002Bh)	UART2 start/stop condition detection, bus collision detection	UART2 start/stop condition detection, bus collision detection
11	+44 to +47 (002Ch to 002Fh)	DMA0	DMA0
12	+48 to +51 (0030h to 0033h)	DMA1	DMA1
13	+52 to +55 (0034h to 0037h)	Key input interrupt	Key input interrupt
14	+56 to +59 (0038h to 003Bh)	A/D converter	A/D converter
15	+60 to +63 (003Ch to 003Fh)	UART2 transmit, NACK2	UART2 transmit, NACK2
16	+64 to +67 (0040h to 0043h)	UART2 receive, ACK2	UART2 receive, ACK2
17	+68 to +71 (0044h to 0047h)	UART0 transmit, NACK0	UART0 transmit, NACK0
18	+72 to +75 (0048h to 004Bh)	UART0 receive, ACK0	UART0 receive, ACK0
19	+76 to +79 (004Ch to 004Fh)	UART1 transmit, NACK1	UART1 transmit, NACK1
20	+80 to +83 (0050h to 0053h)	UART1 receive, ACK1	UART1 receive, ACK1
21	+84 to +87 (0054h to 0057h)	Timer A0	Timer A0
22	+88 to +91 (0058h to 005Bh)	Timer A1	Timer A1
23	+92 to +95 (005Ch to 005Fh)	Timer A2	Timer A2
24	+96 to +99 (0060h to 0063h)	Timer A3	Timer A3
25	+100 to +103 (0064h to 0067h)	Timer A4	Timer A4
26	+104 to +107 (0068h to 006Bh)	Timer B0	Timer B0
27	+108 to +111 (006Ch to 006Fh)	Timer B1	Timer B1
28	+112 to +115 (0070h to 0073h)	Timer B2	Timer B2

Table 4.11 Differences in Interrupt Vectors - (2/2)

Software Interrupt Number	Vector Address	M16C/64	M16C/64A
29	+116 to +119 (0074h to 0077h)	$\overline{\text{INT0}}$	$\overline{\text{INT0}}$
30	+120 to +123 (0078h to 007Bh)	$\overline{\text{INT1}}$	$\overline{\text{INT1}}$
31	+124 to +127 (007Ch to 007Fh)	$\overline{\text{INT2}}$	$\overline{\text{INT2}}$
32 to 40	+128 to +131 (0080h to 0083h) to +160 to +163 (00A0h to 00A3h)	INT instruction interrupt	INT instruction interrupt
41	+164 to +167 (00A4h to 00A7h)	DMA2	DMA2
42	+168 to +171 (00A8h to 00ABh)	DMA3	DMA3
43	+172 to +175 (00ACh to 00AFh)	UART5 start/stop condition detection, bus collision detection	UART5 start/stop condition detection, bus collision detection, CEC1
44	+176 to +179 (00B0h to 00B3h)	UART5 transmit, NACK5	UART5 transmit, NACK5, CEC2
45	+180 to +183 (00B4h to 00B7h)	UART5 receive, ACK5	UART5 receive, ACK5
46	+184 to +187 (00B8h to 00BBh)	UART6 start/stop condition detection, bus collision detection	UART6 start/stop condition detection, bus collision detection, real-time clock period
47	+188 to +191 (00BCh to 00BFh)	UART6 transmit, NACK6	UART6 transmit, NACK6, real-time clock compare
48	+192 to +195 (00C0h to 00C3h)	UART6 receive, ACK6	UART6 receive, ACK6
49	+196 to +199 (00C4h to 00C7h)	UART7 start/stop condition detection, bus collision detection	UART7 start/stop condition detection, bus collision detection, remote control 0
50	+200 to +203 (00C8h to 00CBh)	UART7 transmit, NACK7	UART7 transmit, NACK7, remote control 1
51	+204 to +207 (00CCh to 00CFh)	UART7 receive, ACK7	UART7 receive, ACK7
52 to 58	+208 to +211 (00D0h to 00D3h) to +232 to +235 (00E8h to 00EBh)	INT instruction interrupt	INT instruction interrupt
59	+236 to +239 (00ECh to 00EFh)		I^2C-bus interface interrupt
60	+240 to +243 (00F0h to 00F3h)		SCL/SDA interrupt
61 to 63	+244 to +247 (00F4h to 00F7h) to +252 to +255 (00FCh to 00FFh)		INT instruction interrupt

Table 4.12 Differences in Registers Associated with Interrupt

Symbol	Address		Bit	Differences	
	M16C/64	M16C/64A		M16C/64	M16C/64A
IFSR3A	0205h	0205h	3	Reserved bits	Interrupt request source select bit 0: UART5 start/stop condition detection, bus collision detection 1: CEC1
			4		Interrupt request source select bit 0: UART5 transmission, NACK 1: CEC2
			5		Interrupt request source select bit 0: UART6 start/stop condition detection, bus collision detection 1: Real-time clock cycle
			6		Interrupt request source select bit 0: UART6 transmission, NACK 1: Real-time clock compare
IFSR2A	0206h	0206h	2	Reserved bits	Interrupt request source select bit 0: Not used 1: I^2C-bus interface
			3		Interrupt request source select bit 0: Not used 1: SCL/SDA
			4		Interrupt request source select bit 0: UART7 start/stop condition detection, bus collision detection 1: Remote control 0
			5		Interrupt request source select bit 0: UART7 transmission, NACK 1: Remote control 1
			6	Interrupt request source select bit 0: Timer B3 1: UART0 bus collision detection	Interrupt request source select bit 0: Timer B3 1: UART0 start/stop condition detection, bus collision detection
			7	Interrupt request source select bit 0: Timer B4 1: UART1 bus collision detection	Interrupt request source select bit 0: Timer B4 1: UART1 start/stop condition detection, bus collision detection

4.7 Differences in Timers

Table 4.13 lists Differences in Timers and Table 4.14 lists Differences in Registers Associated with Timer.

Table 4.13 Differences in Timers

Item	M16C/64	M16C/64A
Programmable output mode	No	Yes (3 channels)
Read from timer register in pulse period/pulse width measurement mode	Contents of the reload register (measurement result) can be read by reading the TBi register (i = 0 to 5).	When bits PPWFSk2 to PPWFSk0 in the PPWFSk register (k = 1 and 2) are 0: • Contents of the reload register (measurement result) can be read by reading the TBi register. When bits PPWFSk2 to PPWFSk0 in the PPWFSk register are 1: • Contents of the counter (counter value) can be read by reading the TBi register • Contents of the reload register (measurement result) can be read by reading the TBi1 register
Write to timer register in pulse period/pulse width measurement mode	Value written to the TBj register is written to neither reload register nor counter.	When not counting: Value written to the TBj register is written to both reload register and counter. • When counting: Value written to the TBj register is written to only reload register. (Transferred to counter when reloaded next.)

Table 4.14 Differences in Registers Associated with Timers

Symbol	Address		Bits	Differences	
	M16C/64	M16C/64A		M16C/64	M16C/64A
PWMFS	—	01D4h	—	—	M16C/64A only
TAOW	—	01D8h	—	—	M16C/64A only
TB01	—	01C0h to 01C1h	—	—	M16C/64A only
TB11	—	01C2h to 01C3h	—	—	M16C/64A only
TB21	—	01C4h to 01C5h	—	—	M16C/64A only
TB31	—	01E0h to 01E1h	—	—	M16C/64A only
TB41	—	01E2h to 01E3h	—	—	M16C/64A only
TB51	—	01E4h to 01E5h	—	—	M16C/64A only
PPWFS1	—	01C6h	—	—	M16C/64A only
PPWFS2	—	01E6h	—	—	M16C/64A only

4.8 Differences in Three-phase Motor Control Timer Functions

Table 4.15 lists Differences in Three-phase Motor Control Timer Functions and Table 4.16 lists Differences in Registers Associated with Three-phase Motor Control Timer Function.

Table 4.15 Differences in Three-phase Motor Control Timer Functions

Item	M16C/64	M16C/64A
Position-data-retain function	No	Yes
Three-phase PWM output pin select function	No	Yes

Table 4.16 Differences in Registers Associated with Three-phase Motor Control Timer Function

Symbol	Address		Bit	Differences	
	M16C/64	M16C/64A		M16C/64	M16C/64A
PDRF	—	030Eh	—	—	M16C/64A only
PFCR	—	0318h	—	—	M16C/64A only
TPRC	—	01DAh	—	—	M16C/64A only

4.9 Differences in A/D Converters

Table 4.17 lists Differences in A/D Converters and Table 4.18 lists Differences in Registers Associated with A/D Converter.

Table 4.17 Differences in A/D Converters

Item	M16C/64	M16C/64A
ADST bit in the ADCON0 register when using external trigger	The bit becomes 0 when A/D conversion is completed.	The bit remains 1 when A/D conversion is completed.
Open-circuit detection assist function	No	Yes

Table 4.18 Differences in Registers Associated with A/D Converter

Symbol	Address		Bit	Differences	
	M16C/64	M16C/64A		M16C/64	M16C/64A
AINRST	—	03A2h	—	—	M16C/64A only

4.10 Differences in CRC Calculators

Table 4.19 lists Differences in CRC Calculators and Table 4.20 lists Differences in Registers Associated with CRC Calculator.

Table 4.19 Differences in CRC Calculators

Item	M16C/64	M16C/64A
CRC generator polynomial	CRC-CCITT ($X^{16} + X^{12} + X^5 + 1$)	CRC-CCITT ($X^{16} + X^{12} + X^5 + 1$) or CRC-16 ($X^{16} + X^{15} + X^2 + 1$)
MSB/LSB selection	No	MSB/LSB selectable
CRC snoop	No	Yes

Table 4.20 Differences in Registers Associated with CRC Calculator

Symbol	Address		Bit	Differences	
	M16C/64	M16C/64A		M16C/64	M16C/64A
CRCMR	—	03B6h	—	—	M16C/64A only
CRCSAR	—	03B4h to 03B5h	—	—	M16C/64A only

4.11 Difference in Flash Memories

Table 4.21 lists Difference in Flash Memories.

Table 4.21 Difference in Flash Memories

Item	M16C/64	M16C/64A
Number of erase/write cycles	100 times (all area)	•10,000 times (data flash) •1,000 times (program ROM 1, program ROM 2)

4.12 New Functions in M16C/64A

The following functions have been added in the M16C/64A Group MCU:

- Real-time clock
- PWM function
- Remote control signal receiver
- Multi-master I^2C-bus interface
- CEC function

5. Reference Documents

Hardware Manual
M16C/64 Group Hardware Manual
M16C/64A Group Hardware Manual
(The latest version of these documents can be downloaded from the Renesas Technology Website.)

Technical News/Technical Update
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REVISION HISTORY	M16C/64 Group, M16C/64A Group Difference between M16C/64 and M16C/64A

Rev.	Date	Description	
		Page	Summary
1.00	Aug 31, 2009	–	First edition issued

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