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April 1st, 2010
Renesas Electronics Corporation

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38C2A Group, 38D2 Group

Difference between 38C2A Group and 38D2 Group

1. Difference between 38C2A Group and 38D2 Group

Table 1. Difference between 38C2A Group and 38D2 Group

	38C2A Group		38D2 Group
	Mask ROM	Flash Memory	QzROM
Related Products	M38C24M4A-XXXFP/HP M38C24M6A-XXXFP/HP M38C29MCA-XXXFP/HP	M38C29FFAFP/HP	M38D24G4FP/HP, M38D24G4-XXXFP/HP, M38D24G6FP/HP, M38D24G6-XXXFP/HP, M38D28G8FP/HP, M38D28G8-XXXFP/HP, M38D29GCFP/HP, M38D29GC-XXXFP/HP, M38D29GFFP/HP, M38D29GF-XXXFP/HP
Package	PLQP0064KB-A(Previous Code 64P6Q-A) : 64-pin LQFP(0.5mm pin-pitch) PLQP0064GA-A(Previous Code 64P6U-A) : 64-pin LQFP(0.8mm pin-pitch) (As for the comparison of pin configuration, refer to Page 3.)		
ROM Type : ROM/RAM Size	MASK: 16K/640, 24K/640, 48K/2048	Flash: 60K/2048	QzROM: 16K/640, 24K/640 32K/1536, 48K/2048, 60K/2048
ROM Correction Function	N/A		Included (Refer to 38D2 Group datasheet)
Watchdog Timer	Included (8 Bits x 1)		Included (8 Bits x 1) (On-Chip Oscillator selectable)
CPU Mode Register	Refer to Page 8 for details.		
Operating mode at reset, or when the stop mode returns	ϕ(XIN)/8 mode		Mode depends on OSCSEL(*1) OSCSEL=H : f(XIN)/8 mode OSCSEL=L : On-Chip Oscillator mode
Maximum Oscillation Frequency	10.0MHz		16.0MHz(*2)
Supply Voltage	Refer to Page 10 and Page 11 for details.		
ID-code Area	-	FFD4$_{16}$ to FFDA$_{16}$	-
Reserved ROM area	-	-	FFD0$_{16}$ to FFDB$_{16}$

*1 In the 38D2 group, Pin name of the 7th pin has been altered to OSCSEL from CNVSS.

*2 In the 38D2 group, f(XIN)/2 cannot be used at 12.5MHz $<$ f(XIN) $\leq$ 16MHz.

*3 Refer to the corresponding datasheet for the absolute maximum ratings, recommended operating conditions and electrical characteristics.

	38C2A Group		38D2 Group
	Mask ROM	Flash Memory	QzROM
8-bit timer: Count source	1/1, 1/2, 1/16, 1/32, 1/64, 1/128, 1/256, 1/1024 x f(XIN) or f(XCIN)		1/1, 1/2, 1/16, 1/256 x ϕSOURCE(*3)
16-bit timer: Count source	1/1, 1/2, 1/16, 1/32, 1/64, 1/128, 1/256, 1/1024 x f(XIN) or f(XCIN)		1/1, 1/2, 1/16, 1/256 x ϕSOURCE(*3)
Timer X: IGBT output mode/PWM mode	Compare register x 1		Compare register x 3
Timer X Output Port	1		2 (T_{XOUT2} pin added)
Timer Y: Real Time Port Control	Real time port control bits ($P4_6$, $P4_7$)		Real time port 1 control bit ($P4_6$) Real time port 2 control bit ($P4_7$)
ADKEY Function	Not included		Included (Refer to datasheet)
RRF Register	Not included		Included

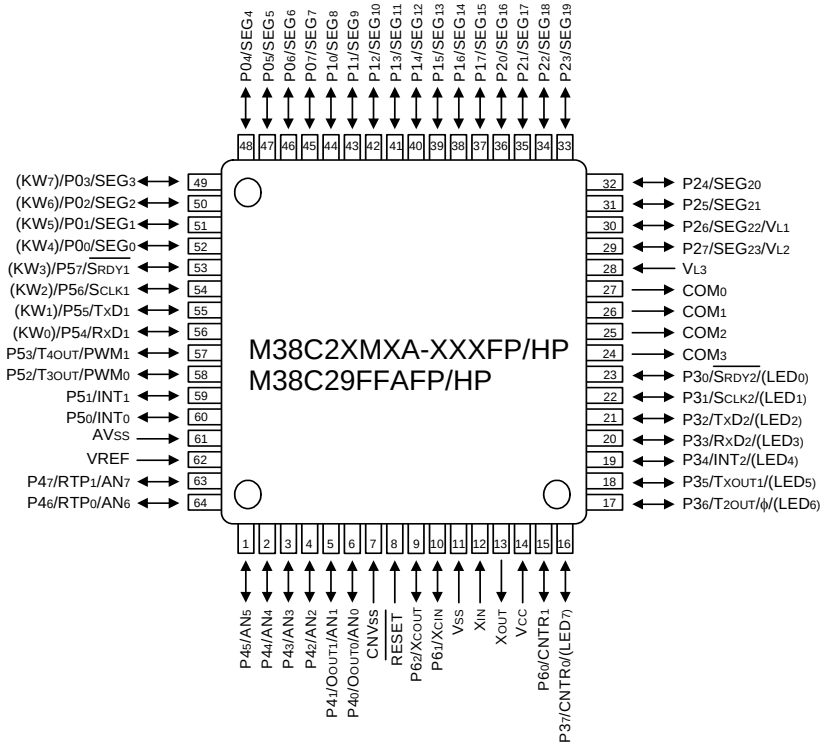
ϕSOURCE: the oscillation frequency of XIN input in the frequency/2, 4 or 8 mode,
on-chip oscillator divided by 4 in the on-chip oscillator mode,
and sub-clock in the low-speed mode.

(Refer to Figure 58 on 38D2 Group Datasheet.)

***** Refer to the corresponding datasheet for the absolute maximum ratings, recommended operating conditions and electrical characteristics.

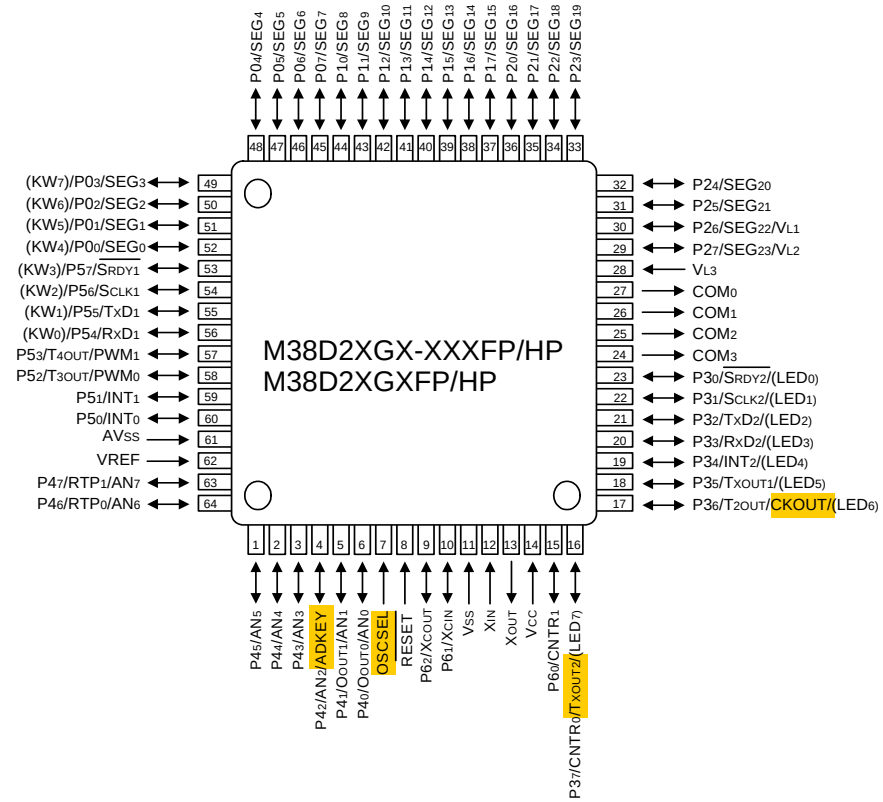
2. Pin Configuration

PIN CONFIGURATION
(TOP VIEW)



Package type : PLQP0064GA-A(64P6U-A)/PLQP0064KB-A(64P6Q-A)

PIN CONFIGURATION
(TOP VIEW)



Package type : PLQP0064GA-A(64P6U-A)/PLQP0064KB-A(64P6Q-A)

3. SFR Comparison between 38C2A Group and 38D2 Group

	38C2A Group	38D2 Group
0000_{16}	Port P0 (P0)	Port P0 (P0)
0001_{16}	Port P0 direction register (P0D)	Port P0 direction register (P0D)
0002_{16}	Port P1 (P1)	Port P1 (P1)
0003_{16}	Port P1 direction register (P1D)	Port P1 direction register (P1D)
0004_{16}	Port P2 (P2)	Port P2 (P2)
0005_{16}	Port P2 direction register (P2D)	Port P2 direction register (P2D)
0006_{16}	Port P3 (P3)	Port P3 (P3)
0007_{16}	Port P3 direction register (P3D)	Port P3 direction register (P3D)
0008_{16}	Port P4 (P4)	Port P4 (P4)
0009_{16}	Port P4 direction register (P4D)	Port P4 direction register (P4D)
$000A_{16}$	Port P5 (P5)	Port P5 (P5)
$000B_{16}$	Port P5 direction register (P5D)	Port P5 direction register (P5D)
$000C_{16}$	Port P6 (P6)	Port P6 (P6)
$000D_{16}$	Port P6 direction register (P6D)	Port P6 direction register (P6D)
$000E_{16}$		
$000F_{16}$		
0010_{16}		Oscillation output control register (OSCOUT)
0011_{16}		CPU mode register 2 (CPUM2)
0012_{16}		RRF register (RRFR)
0013_{16}		LCD mode register (LM)
0014_{16}		LCD power control register (VLCON)
0015_{16}		AD control register (ADCON)
0016_{16}		AD conversion register (low-order) (ADL)
0017_{16}		AD conversion register (high-order) (ADH)
0018_{16}	Clock output control register (CKOUT)	Transmit/receive buffer register 1 (TB1/RB1)
0019_{16}	A-D control register (ADCON)	Serial I/O1 status register (SIO1STS)
$001A_{16}$	A-D conversion register (low-order) (ADL)	Serial I/O1 control register (SIO1CON)
$001B_{16}$	A-D conversion register (high-order) (ADH)	UART control register (UARTCON)
$001C_{16}$	Transmit/receive buffer register 1 (TB1/RB1)	Baudrate generator (BRG1)
$001D_{16}$	Serial I/O1 status register (SIO1STS)	Transmit/receive buffer register 2 (TB2/RB2)
$001E_{16}$	Transmit/receive buffer register 2 (TB2/RB2)	Serial I/O2 status register (SIO2STS)
$001F_{16}$	Serial I/O2 status register (SIO2STS)	Serial I/O2 control register (SIO2CON)

Note: Do not access to the SFR area including nothing.

: Addition or difference

: Only addresses are changed

(Register contents and bit assign are the same.)

	38C2A Group	38D2 Group
0020₁₆	Timer 1 (T1)	Timer 1 (T1)
0021₁₆	Timer 2 (T2)	Timer 2 (T2)
0022₁₆	Timer 3 (T3)	Timer 3 (T3)
0023₁₆	Timer 4 (T4)	Timer 4 (T4)
0024₁₆	PWM01 register (PWM01)	PWM01 register (PWM01)
0025₁₆	Timer 12 mode register (T12M)	Timer 12 mode register (T12M)
0026₁₆	Timer 34 mode register (T34M)	Timer 34 mode register (T34M)
0027₁₆		Timer 1234 mode register (T1234M)
0028₁₆	Compare register (low-order) (COMPL)	Timer 1234 frequency division selection register (PRE1234)
0029₁₆	Compare register (high-order) (COMPH)	Watchdog timer control register (WDTCON)
002A₁₆	Timer X (low-order) (TXL)	Timer X (low-order) (TXL)
002B₁₆	Timer X (high-order) (TXH)	Timer X (high-order) (TXH)
002C₁₆	Timer X (extension) (TXEX)	Timer X (extension) (TXEX)
002D₁₆	Timer Y (low-order) (TYL)	Timer X mode register (TXM)
002E₁₆	Timer Y (high-order) (TYH)	Timer X control register 1 (TXCON1)
002F₁₆	Timer X mode register (TXM)	Timer X control register 2 (TXCON2)
0030₁₆	Timer Y mode register (TYM)	Compare register 1 (low-order) (COMP1L)
0031₁₆		Compare register 1 (high-order) (COMP1H)
0032₁₆		Compare register 2 (low-order) (COMP2L)
0033₁₆		Compare register 2 (high-order) (COMP2H)
0034₁₆		Compare register 3 (low-order) (COMP3L)
0035₁₆		Compare register 3 (high-order) (COMP3H)
0036₁₆		Timer Y (low-order) (TYL)
0037₁₆	Watchdog timer control register (WDTCON)	Timer Y (high-order) (TYH)
0038₁₆	LCD power control register (VLCON)	Timer Y mode register (TYM)
0039₁₆	LCD mode register (LM)	Timer Y control register (TYCON)
003A₁₆	Interrupt edge selection register (INTEDGE)	Interrupt edge selection register (INTEDGE)
003B₁₆	CPU mode register (CPUM)	CPU mode register (CPUM)
003C₁₆	Interrupt request register 1 (IREQ1)	Interrupt request register 1 (IREQ1)
003D₁₆	Interrupt request register 2 (IREQ2)	Interrupt request register 2 (IREQ2)
003E₁₆	Interrupt control register 1 (ICON1)	Interrupt control register 1 (ICON1)
003F₁₆	Interrupt control register 2 (ICON2)	Interrupt control register 2 (ICON2)

Note: Do not access to the SFR area including nothing.

: Addition or difference

: Same register name, but bit assign changed

: Only addresses are changed

(Register contents and bit assign are the same.)

	38C2A Group	38D2 Group
0FE0₁₆	Serial I/O1 control register (SIO1CON)	
0FE1₁₆	UART1 control register (UART1CON)	
0FE2₁₆	Baudrate generator 1 (BRG1)	
0FE3₁₆	Serial I/O2 control register (SIO2CON)	
0FE4₁₆	UART2 control register (UART2CON)	
0FE5₁₆	Baudrate generator 2 (BRG2)	
0FE6₁₆		
0FE7₁₆		
0FE8₁₆		
0FE9₁₆		
0FEA₁₆		
0FEB₁₆		
0FEC₁₆		
0FED₁₆		
0FEE₁₆		
0FEF₁₆		
0FF0₁₆	Oscillation output control register 1 (OSCOUT)	PULL register (PULL)
0FF1₁₆	PULL register (PULL)	UART2 control register (UART2CON)
0FF2₁₆	Key input control register (KIC)	Baudrate generator 2 (BRG2)
0FF3₁₆	Timer 1234 mode register (T1234M)	Clock output control register (CKOUT)
0FF4₁₆	Timer X control register (TXCON)	Segment output disable register 0 (SEG0)
0FF5₁₆	Timer 12 frequency division selection register (PRE12)	Segment output disable register 1 (SEG1)
0FF6₁₆	Timer 34 frequency division selection register (PRE34)	Segment output disable register 2 (SEG2)
0FF7₁₆	Timer XY frequency division selection register (PREXY)	Key input control register (KIC)
0FF8₁₆	Segment output disable register 0 (SEG0)	ROM correction address 1 high-order register (RCA1H)
0FF9₁₆	Segment output disable register 1 (SEG1)	ROM correction address 1 low-order register (RCA1L)
0FFA₁₆	Segment output disable register 2 (SEG2)	ROM correction address 2 high-order register (RCA2H)
0FFB₁₆	Timer Y mode register 2 (TYM2)	ROM correction address 2 low-order register (RCA2L)
0FFC₁₆		ROM correction enable register
0FFD₁₆		Reserved area (access disabled)
0FFE₁₆	Flash memory control register (FMCR)(*1)	Reserved area (access disabled)
0FFF₁₆	Reserved area (access disabled)	Reserved area (access disabled)

Note: Do not access to the SFR area including nothing.

: Addition or difference

: Only addresses are changed

(Register contents and bit assign are the same.)

4.Interrupt Vector Comparison Between 38C2A Group and 38D2 Group

: Differences between 38C2A Group and 38D2 Group

Vector Addresses		Priority	38C2A Group Interrupt Source	38D2 Group Interrupt Source
High	Low			
FFFD16	FFFC16	1	Reset	Reset
FFFB16	FFFA16	2	INT0	INT0
FFF916	FFF816	3	INT1	INT1
FFF716	FFF616	4	INT2 / key input (key-on wakeup)	INT2 / key input (key-on wakeup)
FFF516	FFF416	5	Serial I/O1 receive	CNTR0
FFF316	FFF216	6	Serial I/O1 transmit	Timer X
FFF116	FFF016	7	Serial I/O2 receive	Timer 1
FFEF16	FFEE16	8	Serial I/O2 transmit	Timer 2
FFED16	FFEC16	9	Timer X	Timer 3
FFEB16	FFEA16	10	Timer 1	Timer 4
FFE916	FFE816	11	Timer 2	Serial I/O1 receive
FFE716	FFE616	12	Timer 3	Serial I/O1 transmit
FFE516	FFE416	13	Timer 4	Serial I/O2 receive
FFE316	FFE216	14	CNTR0	Serial I/O2transmit
FFE116	FFE016	15	Timer Y / CNTR1	Timer Y / CNTR1
FFDF16	FFDE16	16	A/D conversion	A/D conversion
FFDD16	FFDC16	17	BRK instruction	BRK instruction

5. CPUM Mode Register

In addition the on-chip oscillator can be selected not used / used by setting the on-chip oscillator stop bit in the CPU mode register 2.

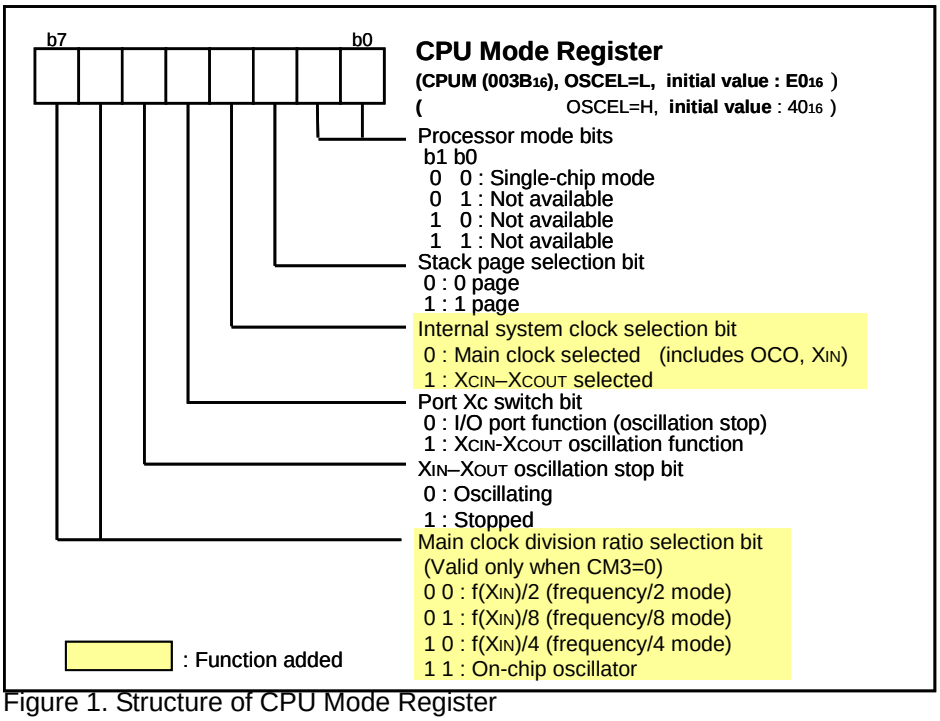


Figure 1. Structure of CPU Mode Register

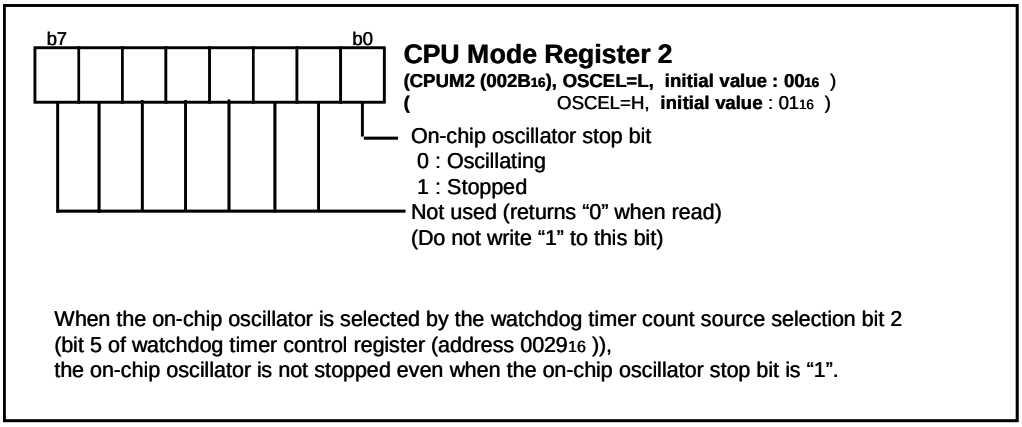


Figure 2. Structure of CPU Mode Register 2

In the 38D2 group, the operating mode can be selected by setting the OSCSEL pin at reset, or when the stop mode returns.

OSCSEL= H, frequency / 8 mode
OSCSEL= L, On-chip oscillator mode

6. Watchdog timer function

In the 38D2 Group, the on-chip oscillator can be selected by setting the Watchdog timer count source selection bit 2.
In this time, set “1” to the STP instruction function selection bit.

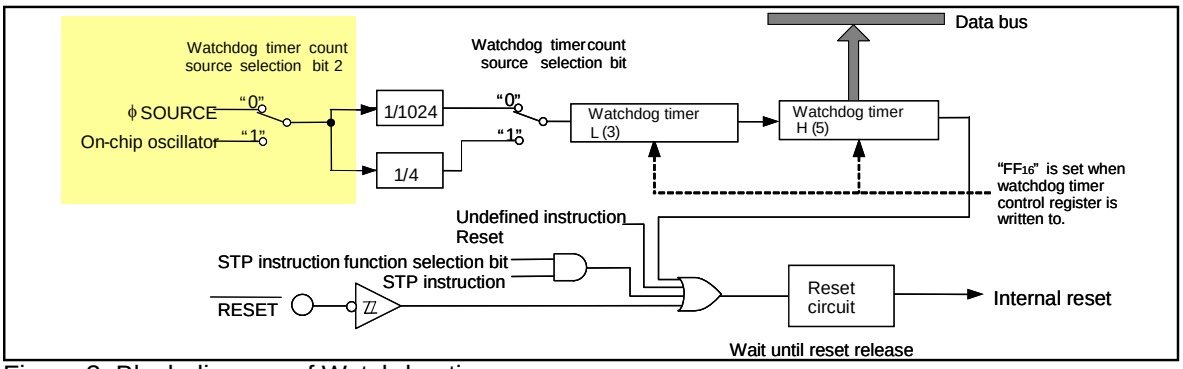


Figure 3. Block diagram of Watchdog timer

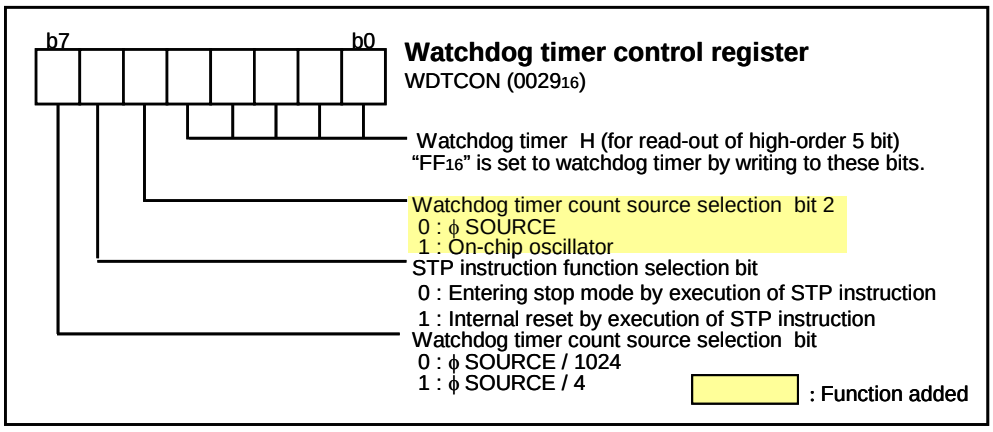


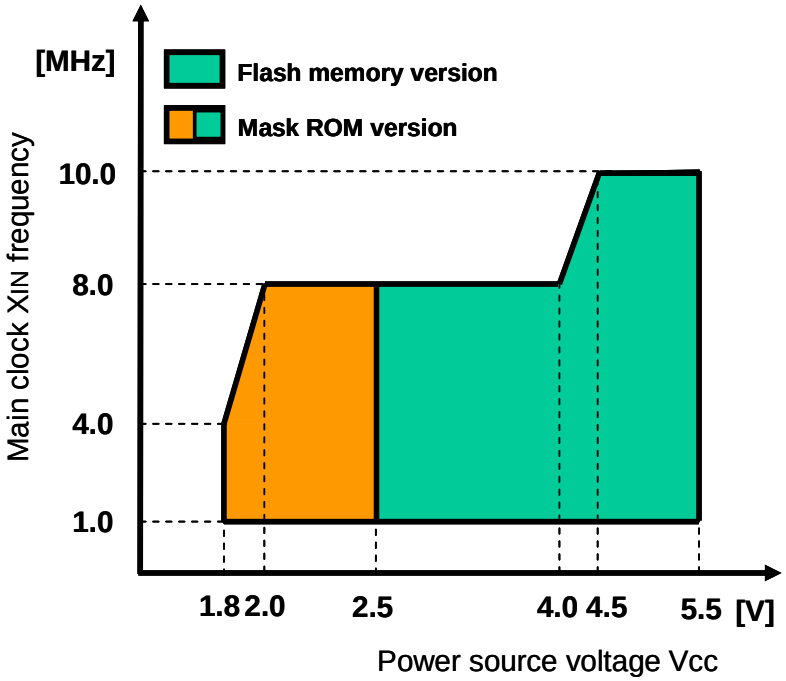
Figure 4. Structure of Watchdog timer control register

1: ϕSOURCE represents the supply source of internal clock ϕ.
XIN input: in the middle- or high-speed mode.
Internal on-chip oscillator divided by 4 in the on-chip oscillator mode,
and Sub clock in the low-speed mode.
2: When the on-chip oscillator is selected by the watchdog timer count source selection bit 2 ,
set the STP instruction function selection bit to “1”.
3: Bits 7 to 5 can be rewritten only once after releasing reset.
After rewriting it is disable to write any data to this bit.

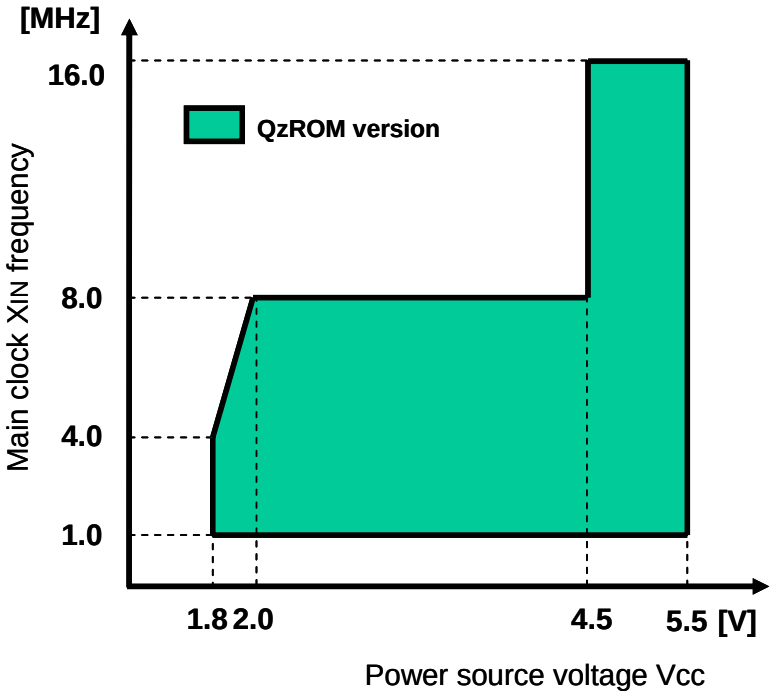
7. 38C2A Group and 38D2 Group Operating Power Source Voltage 1

(A/D operation excluded)

38C2A Group



38D2 Group

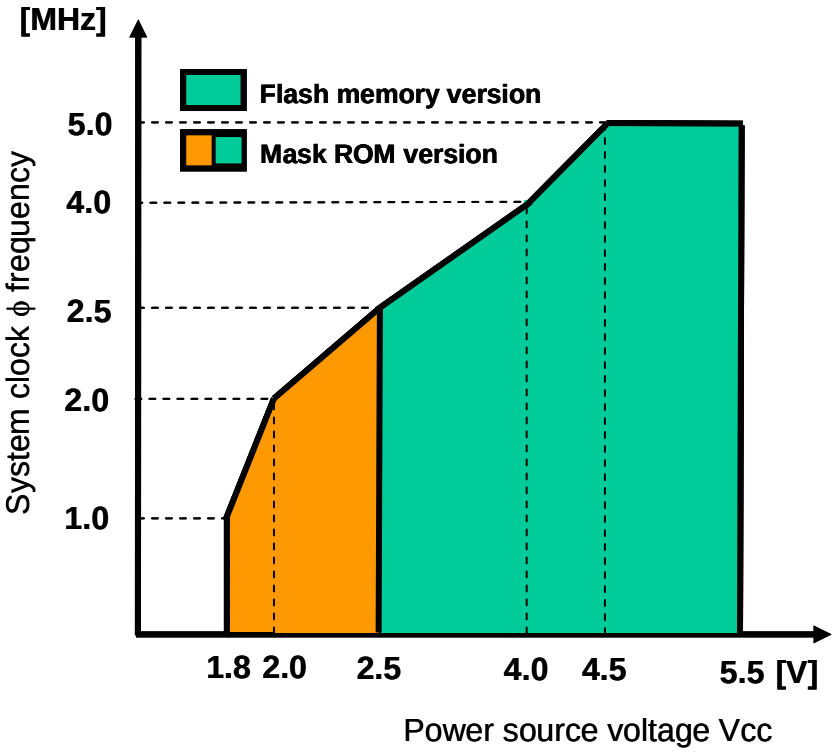


* In the 38D2 group, f(XIN)/2 cannot be used at 12.5MHz< f(XIN)≤16MHz.

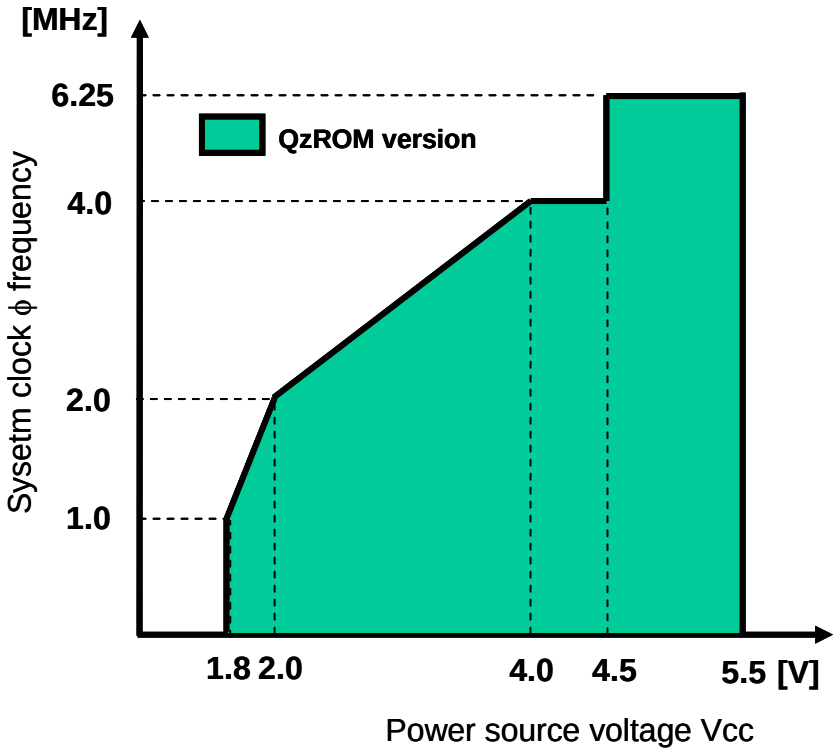
8. 38C2A Group and 38D2 Group Operating Power Source Voltage 2

(A/D operation excluded)

38C2A Group

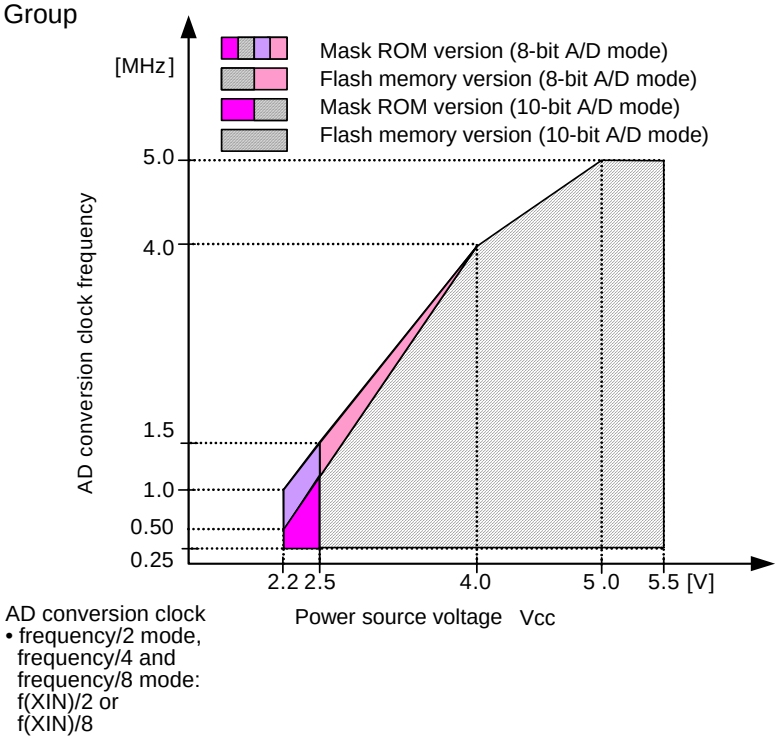


38D2 Group

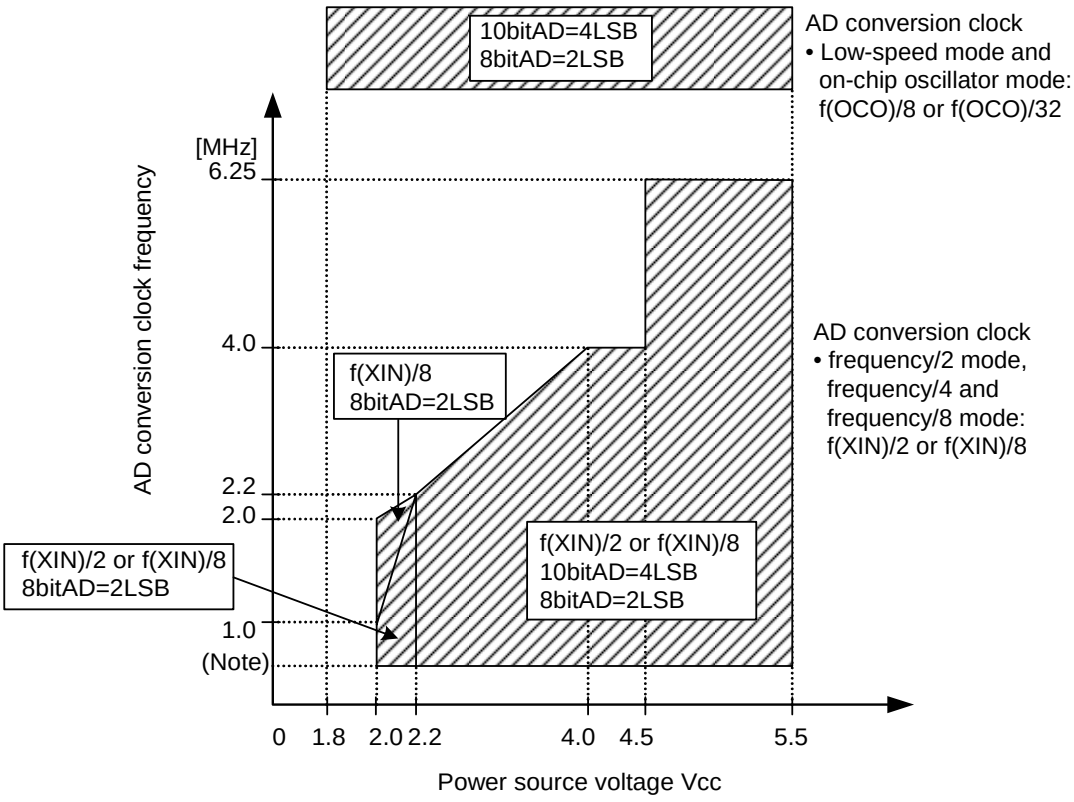


9. 38C2A Group and 38D2 Group A/D Operating Power Source Voltage

38C2A Group



38D2 Group



Note: f(XIN) ≥ 500 kHz

10. Writing for the OSCSEL i

The OSCSEL pin is the power source input pin for the built-in QzROM.
When programming in the QzROM, the impedance of the OSCSEL pin is low to allow the electric current for writing to flow into the built-in QzROM. Because of this, noise can enter easily. If noise enters the OSCSEL pin, abnormal instruction codes or data are read from the QzROM, which may cause a program runaway.

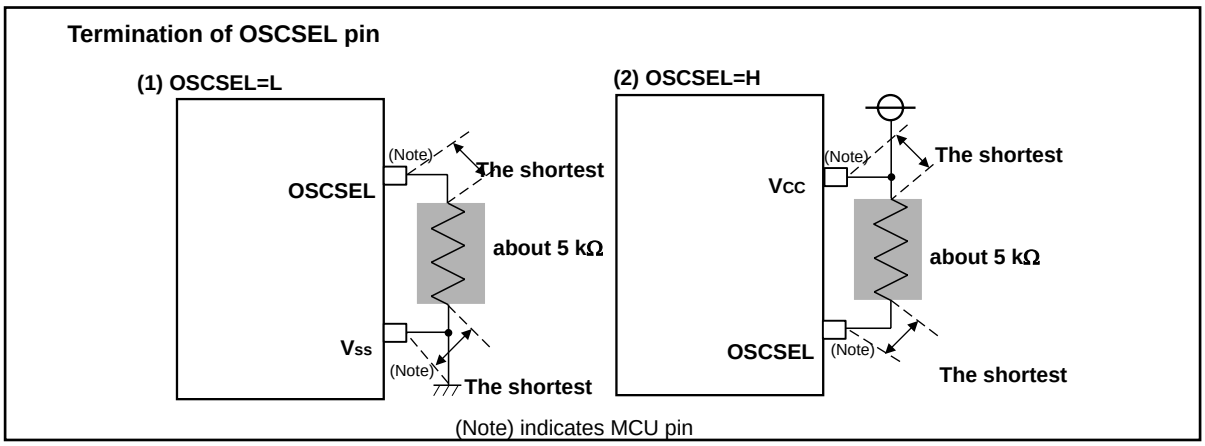


Figure 5. Wiring for the OSCSEL pin

(1)OSCSEL=L
Connect the OSCSEL pin the shortest possible to the GND pattern which is supplied to the VSS pin of the microcomputer.
In addition connecting an approximately 5 kΩ resistor in series to the GND could improve noise immunity. In this case as well as the above mention, connect the pin the shortest possible to the GND pattern which is supplied to the Vss pin of the microcomputer.

(2)OSCSEL=H
Connect the OSCSEL pin the shortest possible to the VCC pattern which is supplied to the VCC pin of the microcomputer.
In addition connecting an approximately 5 kΩ resistor in series to the VCC could improve noise immunity. In this case as well as the above mention, connect the pin the shortest possible to the VCC pattern which is supplied to the Vcc pin of the microcomputer.

11. Notes on Replacement

Contact an oscillator manufacturer. Select an oscillator and oscillation circuit constants to obtain the stabilized operation clock on the user system and its condition for mass-production since the oscillation circuits are different between the 38C2A Group and 38D2 Group, and oscillation circuit constants of XIN-XOUT, XCIN-XCOUT are different every product.

Be careful especially when range of voltage and temperature is wide.

We recommend to design the circuit in consideration of the wiring pattern of the feed-back resistor, the dumping resistor and the load capacity in advance.

The 38D2 Group has been considered compatibility and designed for characteristics, actual values such as operation margin, A/D conversion accuracy, noise immunity, and noise radiation in electrical characteristics depending on the differences in the manufacturing processes may be different.

In the 38D2 Group, noise radiation is decreased compared with the 38C2A Group. Perform sufficient evaluations every individual product.

12. Reference

Data Sheet

38C2 Group Datasheet (A version)

38D2 Group Datasheet

Technical News/Technical Update

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REVISION HISTORY	Difference between 38C2A Group and 38D2 Group

Rev.	Date	Description	
		Page	Summary
1.00	2006.04.15	-	First Edition issued
1.01	2006.05.22	12	A/D Operating Power Source Voltage added
1.02	2006.06.12	1-17	Revision of clerical errors
1.03	2006.06.21	1 2-3	QzROM ROM/RAM size revised Revision of clerical erros

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