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Renesas Electronics Corporation

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3822A Group, 3823 Group

Difference between 3822A Group and 3823 Group

1. Difference between 3822 Group (A Version) and 3823 Group

Table 1. Difference between 3822 Group (A Version) and 3823 Group

	3822 Group (A Version)	3823 Group
	Mask ROM	QzROM
Related Products	M38223M4A-XXXFP/HP M38224M6A-XXXFP/HP M38227M8A-XXXFP/HP M38227MCA-XXXFP/HP	M38234G4-XXXFP/HP, M38234G4FP/HP M38235G6-XXXFP/HP, M38235G6FP/HP M38238G8-XXXFP/HP, M38238G8FP/HP M38239GC-XXXFP/HP, M38239GCFP/HP M3823AGE-XXXFP/HP, M3823AGEFP/HP
Package	PLQP0080KB-A (Previous Code 80P6Q-A) : 80-pin LQFP(0.5mm pin-pitch) PRQP0080GB-A (Previous Code 80P6N-A) : 80-pin QFP(0.8mm pin-pitch)	
ROM Type : ROM/RAM Size	MASK : 16K/512, 24K/640, 32K/1024, 48K/1024	QzROM : 16K/ <u>640</u> , 24K/ <u>768</u> , 32K/ <u>1536</u> , 48K/ <u>2048</u> , <u>60K/2560</u>
Programmable I/O Port	49	
A/D Converter	8 Bits×8ch	8 Bits×8ch <u>10 Bits×8ch</u>
ROM Correction Function	N/A	Included
Watchdog Timer	N/A	Included
On-Chip Oscillator	N/A	Included
CPU Mode Register	Refer to P4 for details	
Peripheral Function Extension Register	N/A	Included
Supply Voltage	1.8 ~ 5.5 V	1.8 ~ 5.5 V

- The 3823 group is pin-compatible with the 3822 group (A version). Electrical characteristics may be different from the one in the 3822 group (A version).

2. SFR Comparison between 3822 Group (A Version) and 3823 Group (1)

	3822 Group (A Version)	3823 Group
0000 ₁₆	Port P0 (P0)	Port P0 (P0)
0001 ₁₆	Port P0 direction register (P0D)	Port P0 direction register (P0D)
0002 ₁₆	Port P1 (P1)	Port P1 (P1)
0003 ₁₆	Port P1 direction register (P1D)	Port P1 direction register (P1D)
0004 ₁₆	Port P2 (P2)	Port P2 (P2)
0005 ₁₆	Port P2 direction register (P2D)	Port P2 direction register (P2D)
0006 ₁₆	Port P3 (P3)	Port P3 (P3)
0007 ₁₆		
0008 ₁₆	Port P4 (P4)	Port P4 (P4)
0009 ₁₆	Port P4 direction register (P4D)	Port P4 direction register (P4D)
000A ₁₆	Port P5 (P5)	Port P5 (P5)
000B ₁₆	Port P5 direction register (P5D)	Port P5 direction register (P5D)
000C ₁₆	Port P6 (P6)	Port P6 (P6)
000D ₁₆	Port P6 direction register (P6D)	Port P6 direction register (P6D)
000E ₁₆	Port P7 (P7)	Port P7 (P7)
000F ₁₆	Port P7 direction register (P7D)	Port P7 direction register (P7D)
0010 ₁₆		ROM correction address 1 high-order register (RCA1H)
0011 ₁₆		ROM correction address 1 low-order register (RCA1L)
0012 ₁₆		ROM correction address 2 high-order register (RCA2H)
0013 ₁₆		ROM correction address 2 low-order register (RCA2L)
0014 ₁₆		ROM correction enable register (RCR)
0015 ₁₆		
0016 ₁₆	Pull register A (PULLA)	Pull register A (PULLA)
0017 ₁₆	Pull register B (PULLB)	Pull register B (PULLB)
0018 ₁₆	Transmit/Receive buffer register (TB/RB)	Transmit/Receive buffer register (TB/RB)
0019 ₁₆	Serial I/O status register (SIOSTS)	Serial I/O status register (SIOSTS)
001A ₁₆	Serial I/O control register (SIOCON)	Serial I/O control register (SIOCON)
001B ₁₆	UART control register (UARTCON)	UART control register (UARTCON)
001C ₁₆	Baud rate generator (BRG)	Baud rate generator (BRG)
001D ₁₆		
001E ₁₆		
001F ₁₆		

NOTES:

Do not access memory in free space of SFR.

: Additional function register

: Different name with same function

3822 Group (A Version)		3823 Group
0020 ₁₆	Timer X low-order register (TXL)	Timer X low-order register (TXL)
0021 ₁₆	Timer X high-order register (TXH)	Timer X high-order register (TXH)
0022 ₁₆	Timer Y low-order register (TYL)	Timer Y low-order register (TYL)
0023 ₁₆	Timer Y high-order register (TYH)	Timer Y high-order register (TYH)
0024 ₁₆	Timer 1 register (T1)	Timer 1 register (T1)
0025 ₁₆	Timer 2 register (T2)	Timer 2 register (T2)
0026 ₁₆	Timer 3 register (T3)	Timer 3 register (T3)
0027 ₁₆	Timer X mode register (TXM)	Timer X mode register (TXM)
0028 ₁₆	Timer Y mode register (TYM)	Timer Y mode register (TYM)
0029 ₁₆	Timer 123 mode register (T123M)	Timer 123 mode register (T123M)
002A ₁₆	φ output control register (CKOUT)	φ output control register (CKOUT)
002B ₁₆		CPU mode expansion register (EXPCM)
002C ₁₆		Temporary data register 0 (TD0)
002D ₁₆		Temporary data register 1 (TD1)
002E ₁₆		Temporary data register 2 (TD2)
002F ₁₆		RRF register (RRFR)
0030 ₁₆		Peripheral function extension register (EXP)
0031 ₁₆		
0032 ₁₆		
0033 ₁₆		
0034 ₁₆	A/D control register (ADCON)	A/D control register (ADCON)
0035 ₁₆	A-D conversion register (AD)	A/D conversion high-order register (ADH)
0036 ₁₆		A/D conversion low-order register (ADL)
0037 ₁₆		Watchdog timer control register (WDTCN)
0038 ₁₆	Segment output enable register (SEG)	Segment output enable register (SEG)
0039 ₁₆	LCD mode register (LM)	LCD mode register (LM)
003A ₁₆	Interrupt edge selection register (INTEDGE)	Interrupt edge selection register (INTEDGE)
003B ₁₆	CPU mode register (CPUM)	CPU mode register (CPUM)
003C ₁₆	Interrupt request register 1 (IREQ1)	Interrupt request register 1 (IREQ1)
003D ₁₆	Interrupt request register 2 (IREQ2)	Interrupt request register 2 (IREQ2)
003E ₁₆	Interrupt control register 1 (ICON1)	Interrupt control register 1 (ICON1)
003F ₁₆	Interrupt control register 2 (ICON2)	Interrupt control register 2 (ICON2)

NOTES:

Do not access memory in free space of SFR.

: Additional function register

: Different name with same function

3. CPUM Mode Register

In the 3823 group, $f(XIN)$ divided by 4 for the system clock ϕ and the on-chip oscillator for the system clock ϕ in low-speed mode can be selected by setting the CPU mode expansion register.

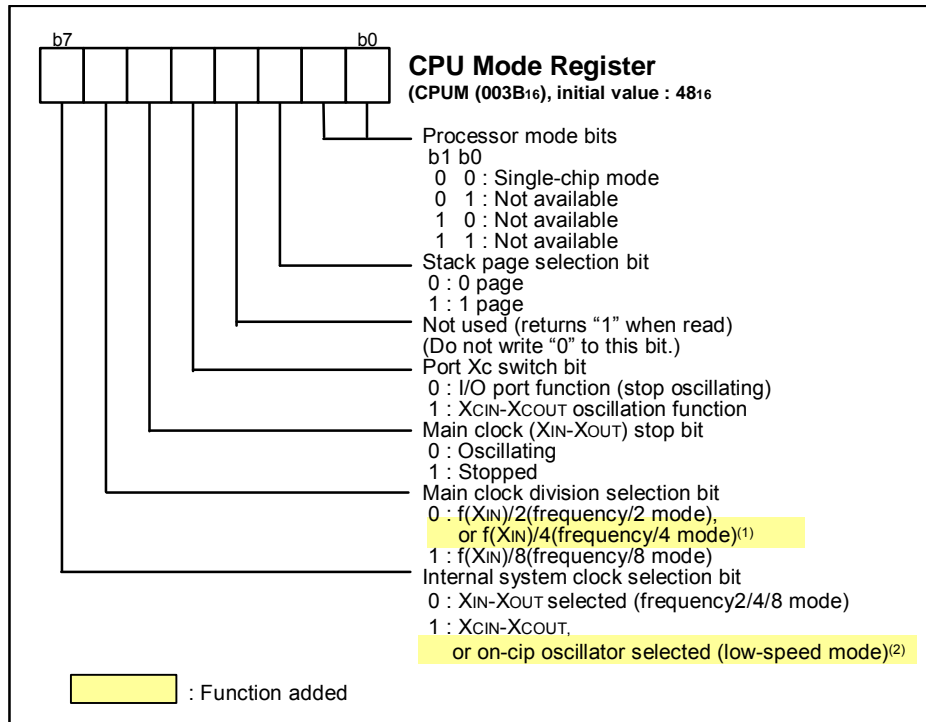


Figure 1. Structure of CPU Mode Register

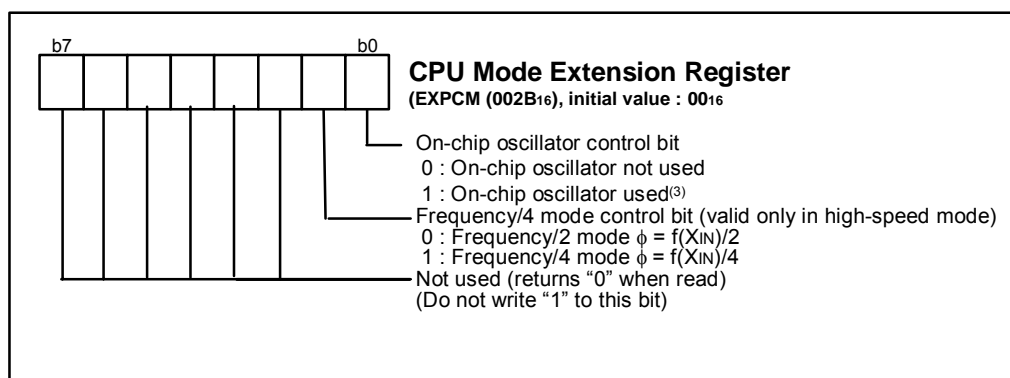


Figure 2. Structure of CPU Mode Extension Register

NOTES:

1. When the system clock ϕ is divided by 4 of $f(XIN)$, set the bit 6 in the CPU mode register to "0" after setting the bit 1 in the CPU mode extension register to "0" after setting the bit 1 in the CPU mode extension register to "1".
2. When using the on-chip oscillator in low-speed mode, set the bit 7 in the CPU mode register to "1" after setting the bit 0 in the CPU mode extension register to "1".
3. The on-chip oscillator is selected for the operation clock in low-speed mode regardless of XCIN-XCOUT.

4. Wiring to P40/(V_{PP})

In the 3823 group, when using P40/(V_{PP}) pin as an input port, connect an approximately 5 kΩ resistor to the P40/(V_{PP}) pin the shortest possible in series.
When not using P40/(V_{PP}) pin, connect the pin the shortest possible to the GND pattern which is supplied to the Vss pin of the microcomputer.

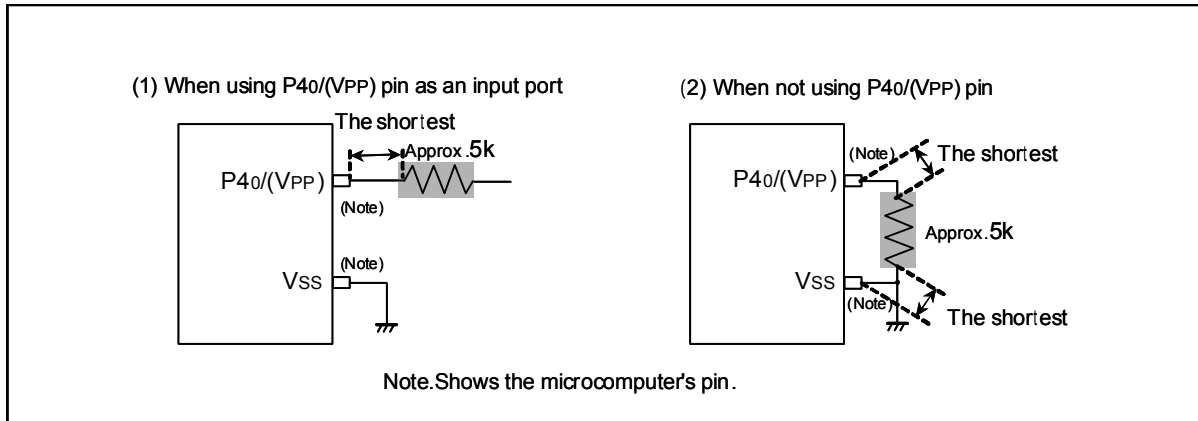


Figure 3. Wiring to P40/(V_{PP})

The P40/(V_{PP}) pin of the QzROM version is the power source input pin for the built-in QzROM. When programming in the QzROM, the impedance of the VPP pin is low to allow the electric current for writing to flow into the built-in QzROM. Because of this, noise can enter easily. If noise enters the P40/(V_{PP}) pin, abnormal instruction codes or data are read from the QzROM, which may cause a program runaway.

Connecting an approximately 5 kΩ resistor in series to the GND could improve noise immunity. Connect the pin the shortest possible to the GND pattern which is supplied to the Vss pin of the microcomputer.

5. Notes on Replacement

The 3823 group is pin-compatible with the 3822 group (A version).

Registers have added with functions of ROM correction, watchdog timer and on-chip oscillator added (Refer to P3,P4 for details.)

When these added functions are not used, process the added registers (bits) as follows:

- (1) Do not write anything to the added registers (bits) (Hold an initial value after reset)
- (2) Write the initial value to the added registers (bits) after reset.

If nothing is written to an address in the above added registers (blank area in 3822 group (A version)) in a program, the program of the 3822 group (A version) specification can be operated in the 3823 group specifications without modifying the program.

Although the 3823 group has been considered compatibility and designed for characteristics, actual values such as operation margin, A/D conversion accuracy, noise immunity, and noise radiation in electrical characteristics depending on the differences in the manufacturing processes may be different. Perform sufficient evaluations every individual product.

Contact an oscillator manufacturer. Select an oscillator and oscillation circuit constants to obtain the stabilized operation clock on the user system and its condition for mass-production since oscillation circuit constants of XIN-XOUT, XCIN-XCOUT are different every product.

6 Reference

Data Sheet

3823 Group Datasheet

3822 Group (A. version) Datasheet

Technical News/Technical Update

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7. Website and Support

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REVISION HISTORY	Difference between 3822A Group and 3823 Group
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Rev.	Date	Description	
		Page	Summary
1.00	2005.09.10	-	First Edition issued
1.10	2005.12.15	5	Wiring to P40/(VPP) added

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