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SH7080 Group

Data Transfer Controller (DTC) in Block Transfer Mode

Introduction

This application note describes the block transfer mode of the data transfer controller (DTC). It is intended as reference material to help in the design of user software.

Target Device

SH7086

Contents

1. Specification

In this sample application, ADI interrupt requests from the A/D converter of the SH7086 activate the DTC for data transfer in block transfer mode.

A/D conversion is performed on analog input channels 0 to 3 (AN0 to AN3) in continuous scan mode. On each round of A/D conversion, the DTC regards the converted data from all four channels as a block and transfer them collectively to the on-chip RAM. This operation is repeated four times. An overview of the operation is presented in figure 1. The flow of data is shown in figure 2.

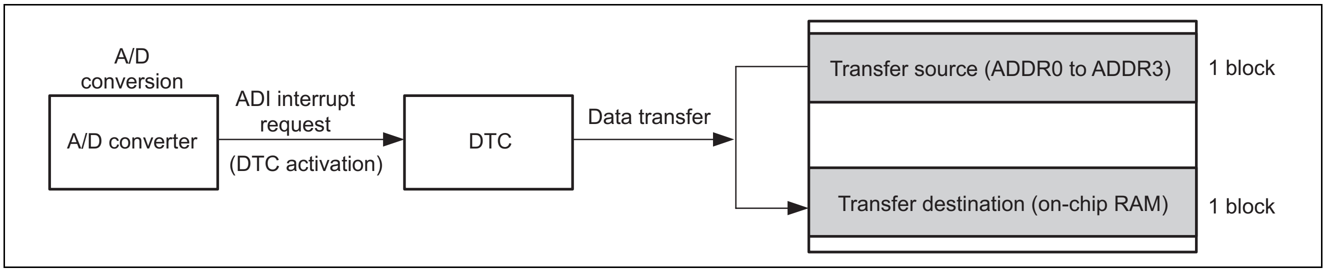


Figure 1 Overview of DTC Operation

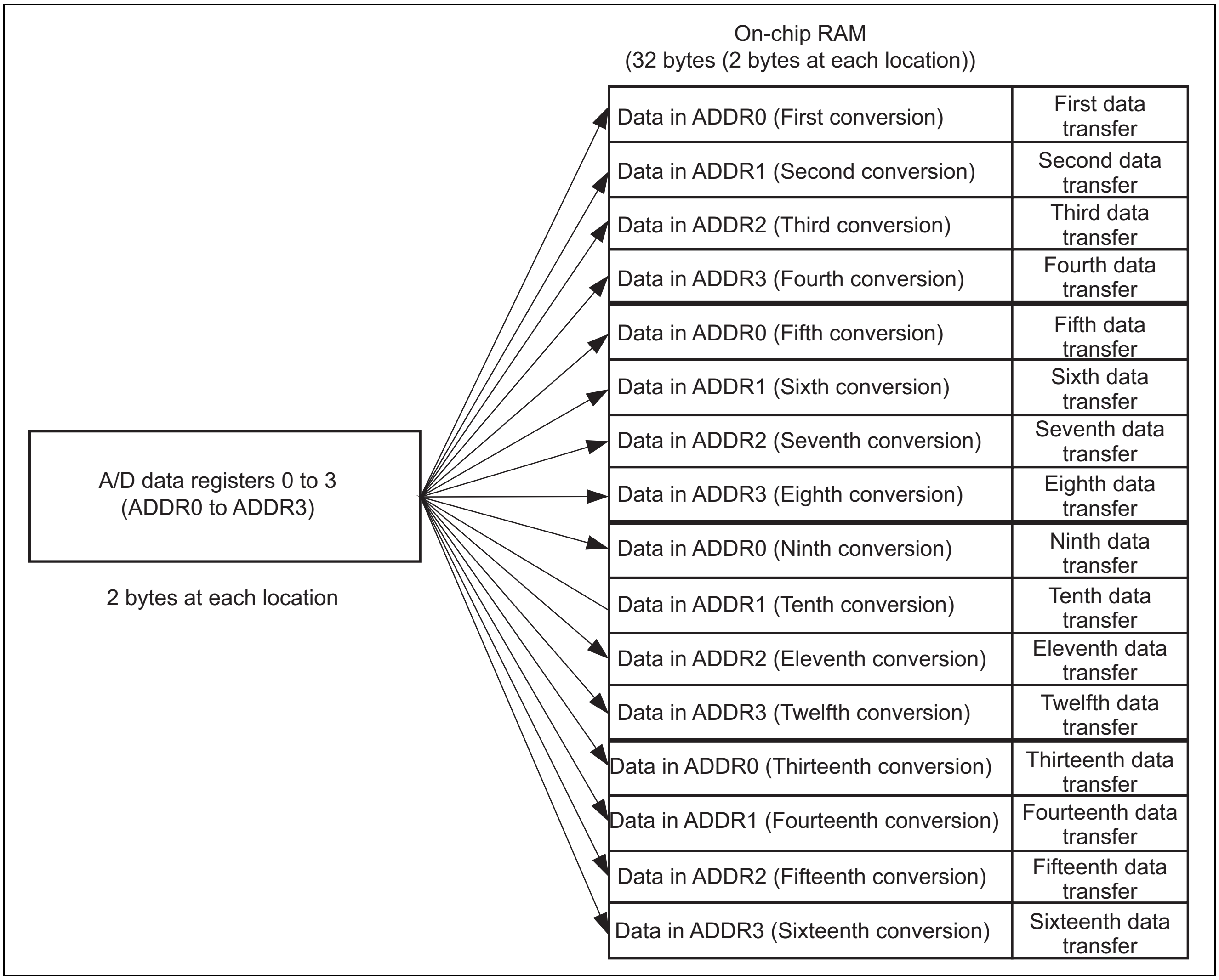


Figure 2 Flow of Data in Block Transfer Mode

2. Applicable Conditions

The applicable conditions for this sample application are shown in table 1.

Table 1 Applicable Conditions

Item	Setting	
Device	SH7086 (R5F70865)	
Operating frequency	Internal clock	Iϕ = 80 MHz
	Bus clock	Bϕ = 40 MHz
	Peripheral clock	Pϕ = 40 MHz
	MTU2 clock	MPϕ = 40 MHz
	MTU2S clock	MIϕ = 80 MHz
Operating mode	Single-chip mode	
Development environment	High-performance Embedded Workshop Ver.4.03.00.001 (integrated development environment) SuperH RISC engine Standard Toolchain (V.9.1.1.0) SuperH RISC engine C/C++ Compiler (V.9.01.01) (manufactured by Renesas Technology)	
C compiler options	High-performance Embedded Workshop default settings: [-cpu=sh2 -object="$(CONFIGDIR)\$(FILELEAF).obj" -debug -gbr=auto -chgincpath -errorpath -global_volatile=0 -opt_range=all -infinite_loop=0 -del_vacant_loop=0 -struct_alloc=1 -nologo]	

3. Description of Modules Used

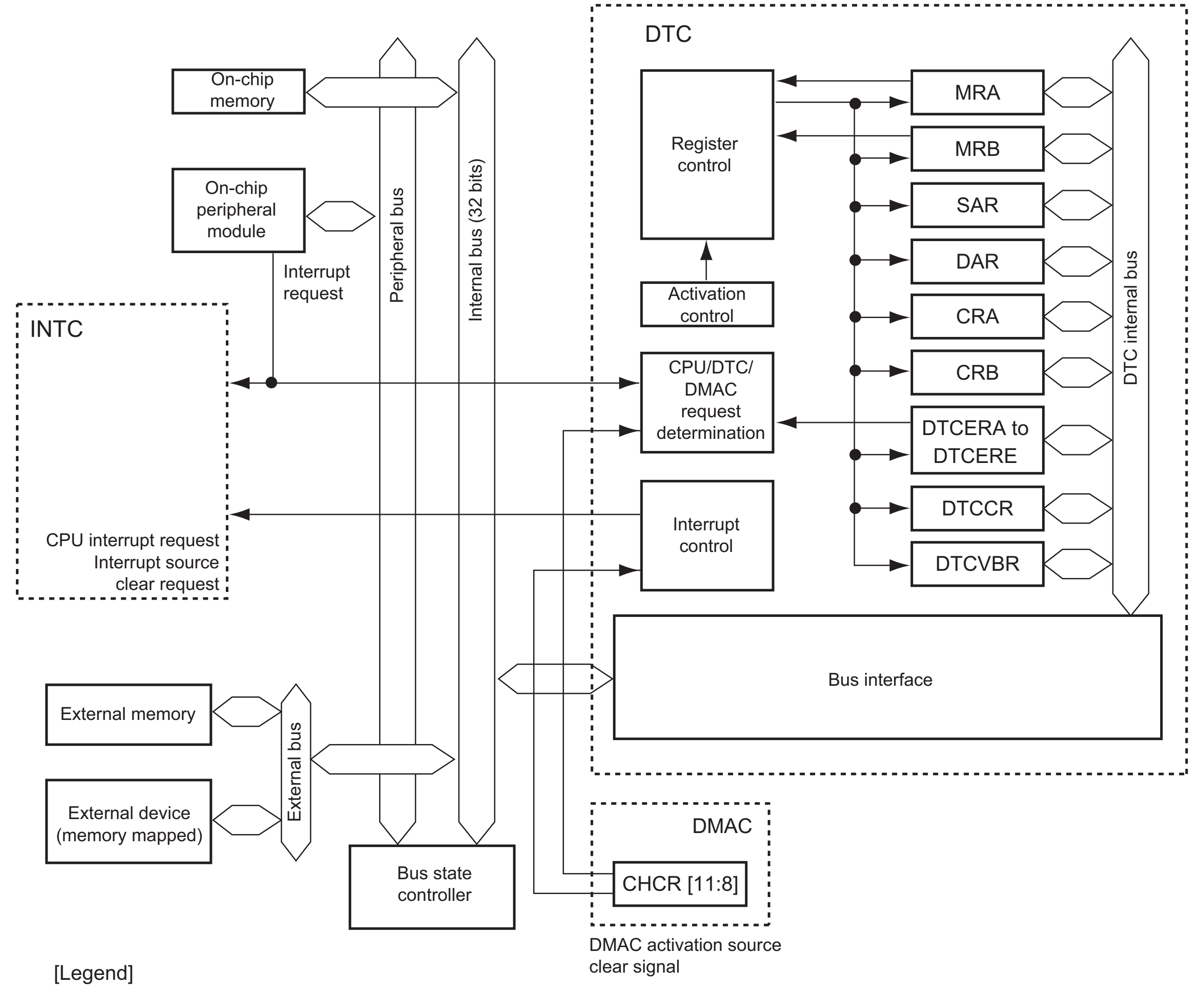
In this sample application, the DTC transfers data to the on-chip RAM when activated by an ADI interrupt request.

The functions of the DTC of SH7080 Group products are outlined in table 2.

Table 2 DTC Function Overview

Item	Overview
Number of channels	Transfer is possible any number of channels.
Chain transfer	Chain transfer is possible (data transfer can be performed multiple times in response to a single activation source). • Chain transfer is only possible after data transfer has been performed for the specified number of times (when the counter = 0).
Transfer mode	• Normal transfer, repeat transfer or block transfer mode can be selected. • Increment decrement or fixed can be selected for the source and destination addresses.
Address space	The transfer source and destination addresses can be specified by 32 bits to select a 4-Gbyte address space directly.
Transfer data size	Data transfer size can be specified by one byte, word or longword.
Interrupt source	• An interrupt request can be issued to the CPU after one data transfer completion. • An interrupt request can be issued to the CPU after all specified data transfer completion.
Bus release timing	Timing is selected from five types.
Priority of DTC activation	Priority of the DTC activation can be selected fro two types.
Others	• Read skip of the transfer-control information can be specified. • Writeback skip is executed for the fixed transfer source and destination addresses. • Module stop mode can be set. • Short address mode can be set.

A block diagram of the DTC is shown in figure 3.



[Legend]

MRA, MRB	: DTC mode registers A and B
SAR	: DTC source address register
DAR	: DTC destination address register
CRA, CRB	: DTC transfer count registers A and B
DTCERA to DTCERE	: DTC enable registers A to E
DTCCR	: DTC control register
DTCVBR	: DTC vector base register
CHCR	: DMA channel control register

Figure 3 Block Diagram of the DTC

- DTC mode register A (MRA) and DTC mode register B (MRB)
  MRA and MRB are 8-bit registers that control the operating mode of the DTC.
- DTC source address register (SAR)
  SAR is a 32-bit register that designates the source address of data to be transferred by the DTC.
- DTC destination address register (DAR)
  DAR is a 32-bit register that designates the destination address of data to be transferred by the DTC.
- DTC transfer count register A (CRA)
  CRA is a 16-bit register that designates the number of times data is to be transferred by the DTC. In normal transfer mode, CRA functions as a 16-bit transfer counter (1 to 65,536). In repeat transfer mode, CRA is divided into two parts: the upper eight bits (CRAH) and the lower eight bits (CRAL). CRAH holds the number of transfers while CRAL functions as an 8-bit transfer counter. In block transfer mode, CRA is divided into tow parts: the upper eight bits (CRAH) and the lower eight bits (CRAL). CRAH holds the block size while CRAL functions as an 8-bit block-size counter.
- DTC transfer count register B (CRB)
  CRB is a 16-bit register that designates the number of times blocks are to be transferred by the DTC in block transfer mode.
- The DTC enable register (DTCER)
  DTCER which is comprised of eight registers, DTCERA to DTCERE, is a 16-bit register that specifies DTC activation interrupt sources.
- The DTC control register (DTCCR)
  DTCCR is an 8-bit register that specifies transfer information read skip.
- The DTC vector base register (DTCVBR)
  DTCVBR is a 32-bit register that specifies the base address for vector table address calculation.
- Six registers, the DTC mode register (MRA), DTC mode register B (MRB), DTC source address register (SAR), DTC destination address register (DAR), DTC transfer count register A (CRA) and DTC transfer count register B (CRB) are not directly accessible from the CPU. When an event corresponding to a DTC activation source occurs, the necessary information for these registers is selected from the set of register information stored in the on-chip RAM and then transferred to the registers so that the DTC transfer can proceed. On completion of the transfer, the contents of these registers are written back to the on-chip RAM. Accordingly, you can have the user program store information for these registers in desired addresses within the on-chip RAM.

Note: For details on the operational specifications, see the section on the data transfer controller (DTC) in the SH7080 Group Hardware Manual.

4. Principles of Operation

Operations for this sample application are described below.

Figure 4 is a timing diagram for A/D conversion, DTC activation and data transfer. The processes are shown in table 3.

In this sample application, the ADI interrupt request is the DTC activation source.

Firstly, the ADI interrupt is enabled, and then the ADST bit is set to 1 to start A/D conversion (figure 4, (1)). When the ADF bit is set to 1 automatically at the end of the A/D conversion, an ADI interrupt request is generated and the DTC is activated (figure 4, (2)). Even if an ADI interrupt request is generated, no interrupt occurs if the DTC is activated. Then, the DTC transfers the converted data in ADDR0 to ADDR3 collectively (as a block) to the previously reserved area in RAM (figure 4, (3)). When the data transfer ends, the ADF bit is automatically cleared (figure 4, (4)). The A/D conversion in this sample application is performed in continuous scan mode. Therefore, the ADST bit is not automatically cleared. The A/D conversion and DTC transfer are repeated three times without the ADST bit being manipulated (figure 4, (5)). When the last (fourth) DTC transfer ends and the ADF bit is set to 1, the DTCE bit is cleared automatically, thereby causing an ADI interrupt (figure 4, (6)). In the processing routine for this interrupt, the ADST bit is cleared to stop the A/D converter (figure 4, (7)).

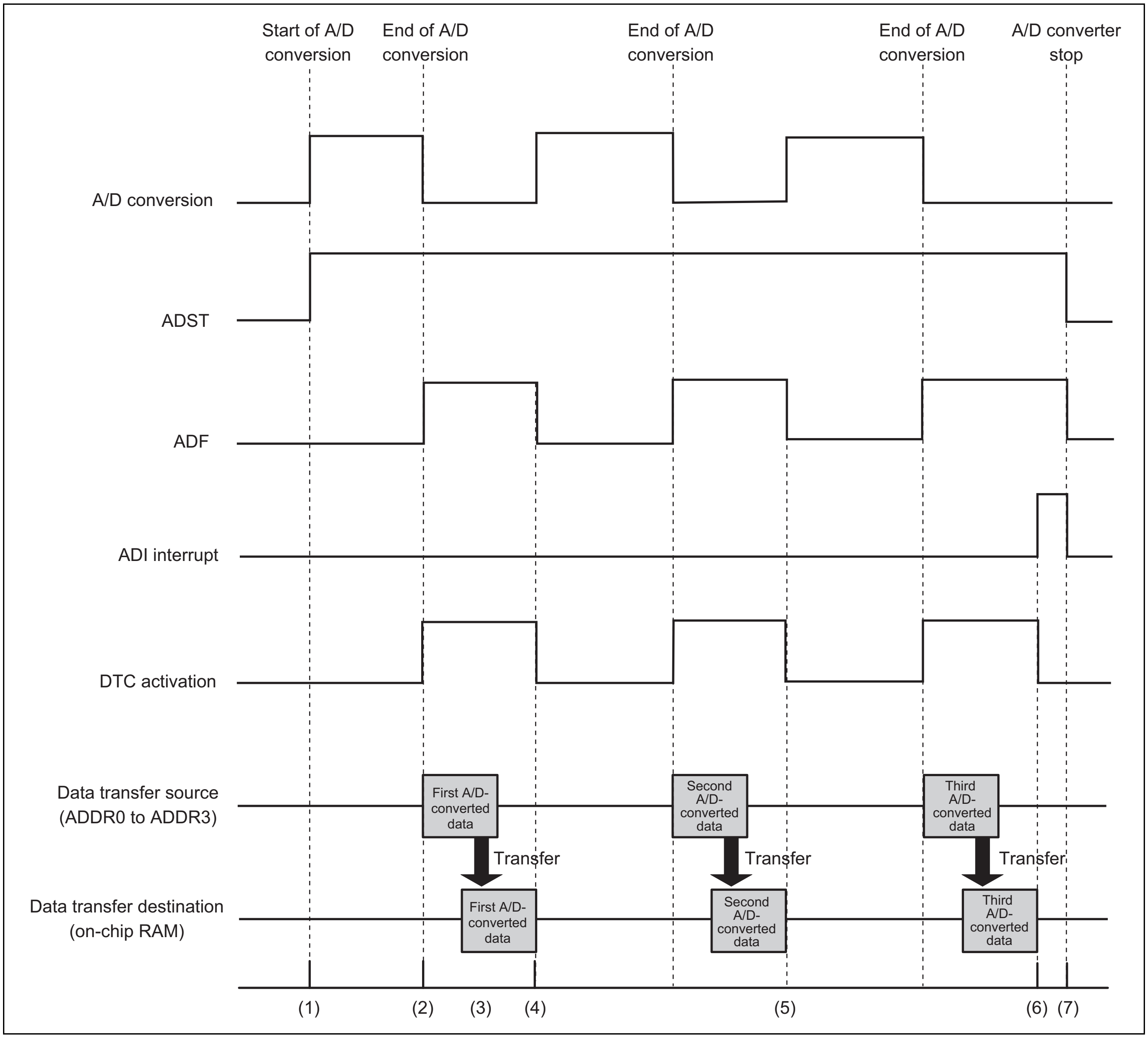


Figure 4 Timing of A/D Conversion and DTC Transfer

Table 3 Processes

	Software Process	Hardware Process
(1)	Enables an ADI interrupt Sets the ADST bit to 1 (for starting A/D conversion)	—
(2)	—	Sets the ADF bit to 1 Generates an ADI interrupt request Activates the DTC
(3)	—	Collective transfer of data in ADDR0 to ADDR3 as a single block to the RAM area
(4)	—	Clears the ADF bit
(5)	Repeats steps (2) to (4), three times	Repetition of steps (2) to (4), three times
(6)	—	Sets the ADF bit to 1 Clears the DTCE bit Generates an ADI interrupt
(7)	Clears the ADST bit (to stop the A/D converter)	—

A more detailed timing diagram of one DTC transfer operations is given as figure 5.

In DTC transfer, DTC activation sources (in this case, ADI interrupt requests) generates DTC request. Mastership of the internal bus is secured and the DTC is activated (figure 5 (1)). The address where the control information for the transfer starts is read from the vector table of ADI activation sources (figure 5 (2)) that has been set up for this example. The information is then read, starting at the given address (figure 5 (3)). After that, a single block of data (ADDR0 to ADDR3) is transferred from the source address (ADDR0) to the destination address (on-chip RAM) (figure 5 (4)). The ADF bit is automatically cleared in response to reading of the ADDR (figure 5 (5)).

Finally, the destination address for the transfer is incremented, and the control information for the transfer is written back (figure 5 (6)). The DTC releases the bus after the writeback operation (figure 5 (7)).

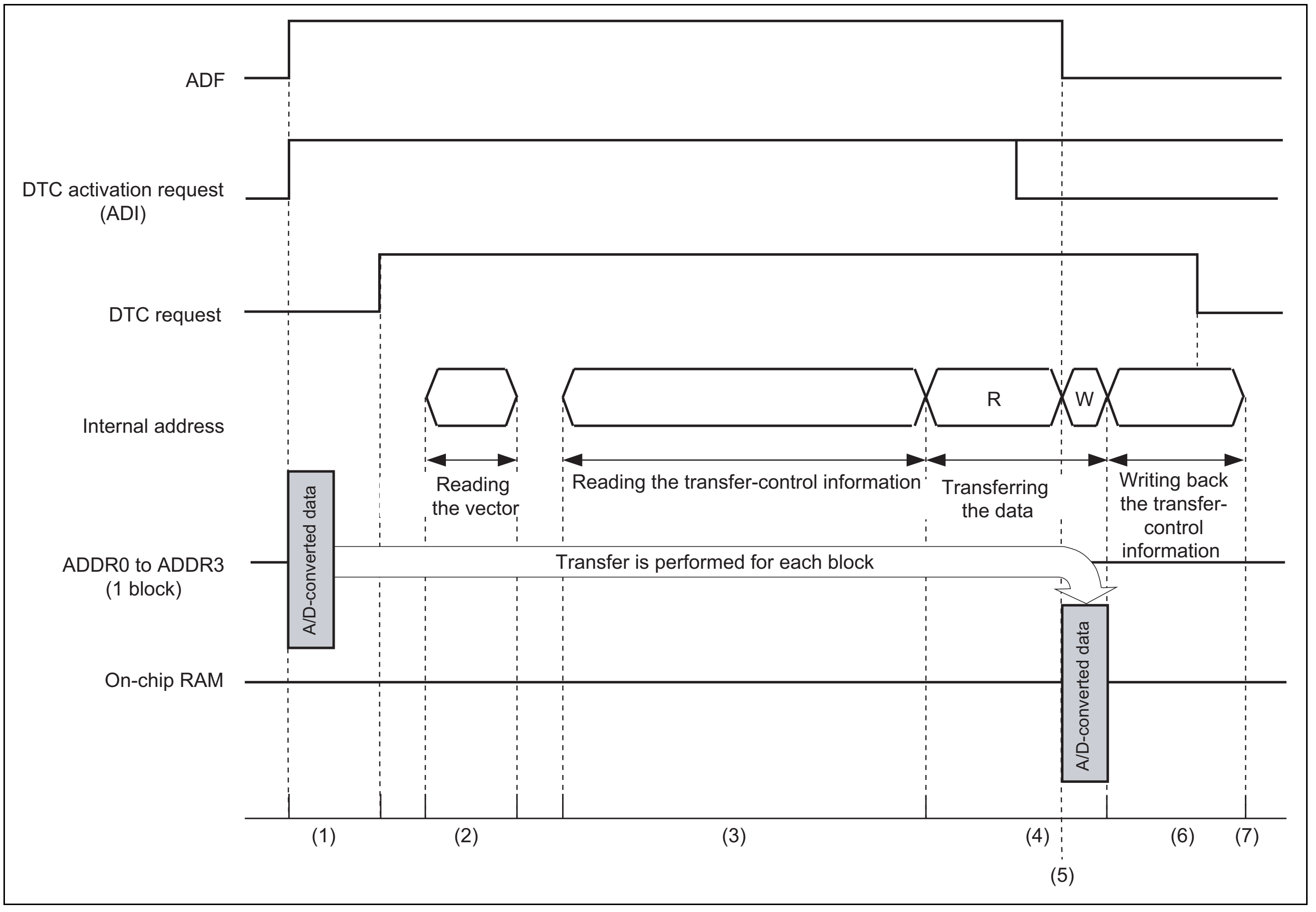


Figure 5 Detailed Timing Chart of DTC Transfer

The flow of data in memory for the operations shown in steps (2) to (4) of figure 5 is illustrated in figure 6 and described in table 4.

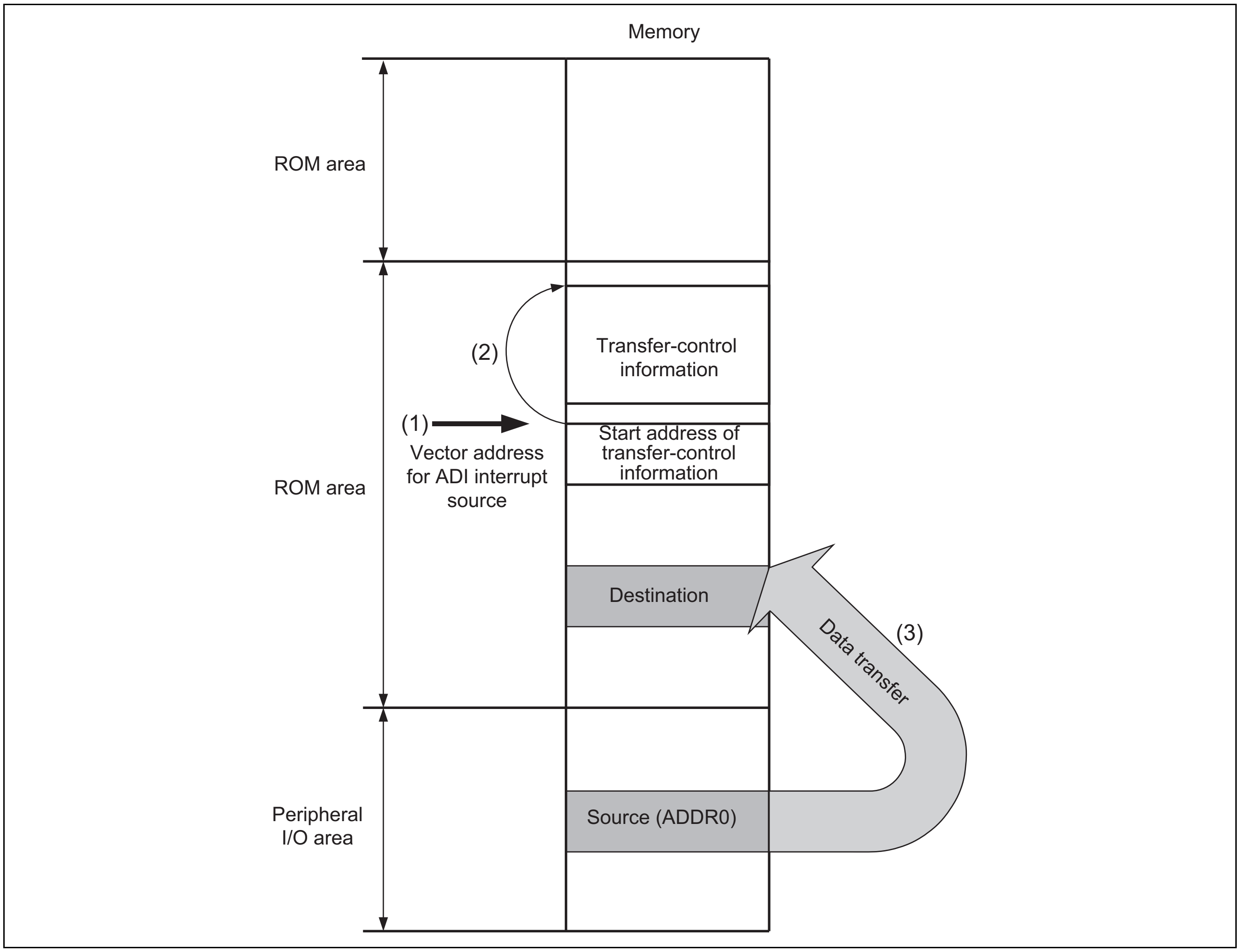


Figure 6 Flow of Data in Memory

Table 4 Description of Figure 6

	DTC Function
(1)	Reads the address (base address + H'400 + interrupt source (ADI) vector number × 4) of the transfer-control information from the vector for this activation source (ADI).
(2)	Reading of the transfer-control information This information specifies the data size, source address, destination address, etc. for the transfer
(3)	Transfers the amount of data specified as the size by the transfer-control information from the source address (ADDR0) to the destination address (in RAM).

5. Description of Software

5.1 List of Functions

The functions used in this sample application are listed below.

Table 5 List of Functions

Function Name	Description
main()	Performs DTC transfer and calls the A/D conversion routine.
ad_conv()	A/D conversion routine
INT_AD0_ADI0 ()	ADI interrupt routine

5.2 Variables Used

The variables used in this sample application are listed below.

Table 6 List of Variables

Variable/Label Name	Description	Reference Function
unsigned short D_data[DTC_COUNT]	Array (of 2-byte elements) for storing transferred data. DTC_COUNT is the number of times transfer is to proceed, i.e. 16 (4 channels (1 block) × 4 times) for this sample application.	main()
unsigned short dummy	Variable for reading the interrupt source bit	main()

5.3 Section Settings

The sections of the program for this sample application are assigned as shown below.

The vector for a DTC activation source used in this sample application is as follows.

Table 7 Section Settings

Address	Section Name	Description
H'00000000	DVECTTBL, DINTTBL, PIntPRG	DVECTTBL: Exception vector table DINTTBL: Interrupt vector table PIntPRG: Interrupt program
H'00000800	PResetPRG	Reset program
H'00001000	P, C$BSEC, C$DEC, D	P: Program area C$BSEC: Holds an address for B section initialization. C$DEC: Holds an address for D section initialization. D: Holds data.
H'FFFF4000	B, R	B: Uninitalized data area R: Initalized data area
H'FFFF6720	DDTC_AD0_ADI	Vector for the DTC activation source (ADI interrupt requests)
H'FFFFBC00	S	Stack area

5.4 Register Settings

The registers used in this sample application are described below. The settings below are the values used in this application and differ from the initial values.

5.4.1 Clock Oscillator (CPG) Settings

1. Frequency Control Register (FRQCR)

Function: Specifies the frequency division ratios for the internal clock (Iϕ), bus clock (Bϕ), peripheral clock (Pϕ), MTU2S clock (MIϕ), and MTU2 clock (MPϕ).

Set value: H'0241

Bit	Bit Name	Set Value	Description
15	—	0	Reserved
14 to 12	IFC[2:0]	000	Internal Clock (Iϕ) Frequency Division Ratio 000: × 1 (Iϕ = 80 MHz for an input clock frequency of 10 MHz)
11 to 9	BFC[2:0]	001	Bus Clock (Bϕ) Frequency Division Ratio 001: × 1/2 (Bϕ = 40 MHz for an input clock frequency of 10 MHz)
8 to 6	PFC[2:0]	001	Peripheral Clock (Pϕ) Frequency Division Ratio 001: × 1/2 (Pϕ = 40 MHz for an input clock frequency of 10 MHz)
5 to 3	MIFC[2:0]	000	MTU2S Clock (MIϕ) Frequency Division Ratio 000: × 1 (MIϕ = 80 MHz for an input clock frequency of 10 MHz)
2 to 0	MPFC[2:0]	001	MTU2 Clock (MPϕ) Frequency Division Ratio 001: × 1/2 (MPϕ = 40 MHz for an input clock frequency of 10 MHz)

5.4.2 Power-Down Mode Settings

1. Standby Control Register 2 (STBCR2)

Function: Controls the operation of individual modules in power-down mode.
Set value: H'28

Bit	Bit Name	Set Value	Description
7	MSTP7	0	Module Stop Bit 7 When set to 1, stops the clock supply to the to the on-chip RAM. When set to 0, activates the on-chip RAM.
6	MSTP6	0	Module Stop Bit 6 When set to 1, stops the clock supply to the to the ROM. When set to 0, activates the ROM.
5	—	1	Reserved
4	MSTP4	0	Module Stop Bit 4 When set to 1, stops the clock supply to the to the DTC. When set to 0, activates the DTC.
3	MSTP3	1	Module Stop Bit 3 When set to 1, stops the clock supply to the to the DMAC. When set to 0, activates the DMAC.
2 to 0	—	All 0	Reserved

2. Standby Control Register 4 (STBCR4)
   Function: Controls the operation of individual modules in power-down mode.
   Set value: H'FE

Bit	Bit Name	Set Value	Description
7	MSTP23	1	Module Stop Bit 23 When set to 1, stops the clock supply to the to the MTU2S. When set to 0, activates the MTU2S.
6	MSTP22	1	Module Stop Bit 22 When set to 1, stops the clock supply to the to the MTU2. When set to 0, activates the MTU2.
5	MSTP21	1	Module Stop Bit 21 When set to 1, stops the clock supply to the to the CMT. When set to 0, activates the CMT.
4, 3	—	All 1	Reserved
2	MSTP18	1	Module Stop Bit 18 When set to 1, stops the clock supply to the to the AD_2. When set to 0, activates the AD_2.
1	MSTP17	1	Module Stop Bit 17 When set to 1, stops the clock supply to the to the AD_1. When set to 0, activates the AD_1.
0	MSTP16	0	Module Stop Bit 16 When set to 1, stops the clock supply to the to the AD_0. When set to 0, activates the AD_0.

5.4.3 Interrupt Controller Settings

1. Interrupt Priority Register K (IPRK)
   Function: Sets priority levels for interrupt sources.
   Set value: H'F000

Bit	Bit Name	Set Value	Description
15 to 12	A/D0, 1	All 1	Set the priority level of the A/D0 and A/D1 interrupt sources. (The maximum value, 15, is set in this sample application).
11 to 8	A/D2	All 0	Set the priority level of the A/D2 interrupt source. (The initial value is set in this sample application).
7 to 0	—	All 0	Reserved

5.4.4 DTC Settings

1. DTC Mode Register A (MRA)
   Function: Selects DTC operating mode. MRA cannot be accessed directly by the CPU. Transfer-control information should be stored in the on-chip RAM.

   Set value: H'10

Bit	Bit Name	Set Value	Description
7, 6	MD[1:0]	10	DTC Mode 1 and 0 Specifies the DTC transfer mode. (Block transfer mode is specified in this sample application.)
5, 4	Sz[1:0]	01	DTC data transfer size 1 and 0 Specifies the size of data to be transferred. (One word is specified in this sample application.)
3, 2	SM[1:0]	10	Source Address Mode 1 and 0 Specifies an SAR operation after a data transfer. (SAR is incremented after transfer in this sample application.)
1, 0	—	All 0	Reserved

2. DTC Mode Register B (MRB)

Function: Selects operating mode. MRB cannot be accessed directly by the CPU. Transfer-control information should be stored in the on-chip RAM.

Set value: H'08

Bit	Bit Name	Set Value	Description
7	CHNE	0	DTC Chain Transfer Enable Specifies the chain transfer. (Chain transfer is disabled for this sample application.)
6	CHNS	0	DTC Chain Transfer Select Specifies the chain transfer condition. (Used in case of chain transfer.)
5	DISEL	0	DTC Interrupt Select When this bit is set to 1, an interrupt request is issued to the CPU after each data transfer or block transfer. When this bit is set to 0, an interrupt request is issued to the CPU after data transfer has been completed for the specified number of times.
4	DTS	0	DTC Transfer Mode Select Specifies either the source or destination as repeat or block area during repeat or block transfer mode. (Used in the case of repeat transfer and block transfer modes.) (The block area is on the source side for this sample application.)
3, 2	DM[1:0]	10	Destination Address Mode 1 and 0 Specifies the DAR operation after data transfer. (The DAR is incremented after transfer in case of this sample application.)
1, 0	—	00	Reserved

. DTC Source Address Register (SAR)

Function: Designates the source address of data to be transferred by the DTC. SAR cannot be accessed directly by the CPU. Transfer-control information should be stored in the on-chip RAM.

Set value: H'FFFFC900 (&AD0.ADDR0)

4. DTC Destination Address Register (DAR)

Function: Designates the source address of data to be transferred by the DTC. DAR cannot be accessed directly by the CPU. Transfer-control information should be stored in the on-chip RAM.

Set value: H'FFFF4410 (&(D_data[0]))

5. DTC Transfer Count Register (CRA)

Function: Specifies the DTC data transfer count.

In repeat transfer mode, CRA is divided into two parts: the upper eight bits (CRAH) and the lower eight bits (CRAL). CRAH holds the number of transfers while CRAL functions as an 8-bit transfer counter (1 to 256). CRAL is decremented by 1 every time data is transferred, and the contents of CRAH are sent to CRAL when the count reaches H'00. The transfer count is 1 when CRAH = CRAL = H'01, 255 when CRAH = CRAL = H'FF, and 256 when CRAH = CRAL = H'00.

This register cannot be accessed directly from the CPU. Transfer control information should be stored in the on-chip RAM.

Set value: H'0404 (4 words)

6. DTC Transfer Count Register B (CRB)

Function: Designates the number of times data is to be transferred by the DTC in block transfer mode. CRB cannot be accessed directly by the CPU. Transfer-control information should be stored in the on-chip RAM.
Since there is no block transfer in this sample application, the initial values are left intact.

Set value: H'0004 (4 times)

7. DTC Enable Register D (DTCERD)

Function: Selects an interrupt source for activating the DTC. The other DTC enable registers are not used for this sample application.

The clearing and setting conditions for each bit in the DTECERD are shown below.

[Clearing conditions]

- Writing 0 to the it after reading it as 1
- Completion of one data transfer and the DISEL bit in MRB = 1
- Completion of the specified number of transfers

[Setting conditions]

- Writing 1 to the bit after reading it as 0

Set value: H'0020

Bit	Bit Name	Set Value	Description
15	DTCERD15	0	When set to 1, selects TGIA_4S as the DTC activation source.
14	DTCERD14	0	When set to 1, selects TGIB_4S as the DTC activation source.
13	DTCERD13	0	When set to 1, selects TGIC_4S as the DTC activation source.
12	DTCERD12	0	When set to 1, selects TGID_4S as the DTC activation source.
11	DTCERD11	0	When set to 1, selects TGIV_4S as the DTC activation source.
10	DTCERD10	0	When set to 1, selects TGIU_4S as the DTC activation source.
9	DTCERD9	0	When set to 1, selects TGIV_4S as the DTC activation source.
8	DTCERD8	0	When set to 1, selects TGIW_4S as the DTC activation source.
7	DTCERD7	0	When set to 1, selects CMI_0 as the DTC activation source.
6	DTCERD6	0	When set to 1, selects CMI_1 as the DTC activation source.
5	DTCERD5	1	When set to 1, selects ADI_0 as the DTC activation source.
4	DTCERD4	0	When set to 1, selects ADI_1 as the DTC activation source.
3	DTCERD3	0	When set to 1, selects ADI_2 as the DTC activation source.
2 to 0	—	All 0	Reserved

8. DTC Control Register (DTCCR)
   Function: Specifies transfer-control information read skip.
   Set value: H'00

Bit	Bit Name	Set Value	Description
7 to 5	—	All 0	Reserved
4	RRS	0	DTC Transfer-Control information Read Skip Enable Controls the vector address read and transfer-control information read. A DTC vector number is always compared with the vector number for the previous activation. If the vector numbers match and this bit is set to 1, the DTC data transfer is started without reading a vector address and Transfer-control information. If the previous DTC activation is a chain transfer, the vector address read and transfer-control information read are always performed.
3	RCHNE	0	Chain Transfer Enable After DTC Repeat Transfer Enables or disables chain transfer while transfer counter is 0 in repeat transfer mode.
2, 1	—	All 0	Reserved
0	ERR	0	Transfer Stop Flag Indicates that the DTC address error or NMI request has occurred. If a DTC address error or NMI occurs while the DTC is active, address error handling or NMI handling processing is executed after the DTC has released the bus mastership. The DTC stops in the transfer-control information writing state after transferring data. [Clearing condition] • Writing of 0 to this bit after reading it as 1

9. DTC Vector Base Register (DTCVBR)
   Function: Specifies the base address for vector table address calculation.
   Set value: H'FFFF6000

10. Bus Function Extending Register (BSCEHR)

Function: This register sets the DTC bus release timing, etc.
Set value: BSCEHR is not set in this sample application and the initial values are used on an as-is basis.

Bit	Bit Name	Initial Value	Description
15	DTLOCK	0	DTC Lock Enable Specifies the timing of bus release by the DTC.
14	CSSTP1	0	Select Bus Release on NOP Cycle Generation by DTC Specifies whether or not the bus is released in response to requests from the CPU for external space access on generation of the NOP cycle that follows reading of the vector address.
13	—	0	Reserved
12	CSSTP2	0	Select Bus Release during Burst-Mode-DMAC/DTC Transfer
11	DTBST	0	DTC Burst Enable Selects whether or not the DTC retains the bus mastership and remains continuously active until all transfer operations are complete when multiple DTC activation requests have been generated.
10	DTSA	0	DTC Short Address Mode Designates whether the information that specifies a DTC transfer takes up 3 or 4 longwords.
9	CSSTP3	0	Select Priority for External Memory Access by CPU
8	DTPR	0	Application of Priority in DTC Activation When multiple DTC activation requests are generated before the DTC is activated, specify whether transfer starts from the first request to have been generated or is in accord with the priority order for DTC activation requests. However, when multiple DTC
7 to 5	—	All 0	Reserved
4	DMMTU4	0	Enable Burst-Mode DMAC Transfer with TGIA_4 Activation Source
3	DMMTU3	0	Enable Burst-Mode DMAC Transfer with TGIA_3 Activation Source
2	DMMTU2	0	Enable Burst-Mode DMAC Transfer with TGIA_2 Activation Source
1	DMMTU1	0	Enable Burst-Mode DMAC Transfer with TGIA_1 Activation Source
0	DMMTU0	0	Enable Burst-Mode DMAC Transfer with TGIA_0 Activation Source

5.4.5 A/D Conversion Settings

1. A/D Control/Status Register_0 (ADCSR_0)
   Function: Controls A/D conversion and sets A/D conversion time.
   Set value: H'401B

Bit	Bit Name	Set Value	Description
15	ADF	0	A/D End Flag A status flag that indicates the end of A/D conversion. [Setting condition] • Completion of A/D conversion on all channels in scan mode [Clearing conditions] • Writing of 0 to this it after reading it as 1 • DMAC or DTC activation by an ADI interrupt to read ADDR
14	ADIE	1	A/D Interrupt Enable The A/D conversion end interrupt (ADI) request is enabled when 1 is set.
13, 12	—	All 0	Reserved
11	TRGE	0	Trigger Enable Disables triggering of A/D conversion when TRGE = 1.
10	—	0	Reserved
9	CONADF	0	ADF Control Controls setting of the ADF bit in 2-channel scan mode.
8	STC	0	State Control Sets the A/D conversion time. (50 cycles is set in this sample application.)
7, 6	CKSL[1:0]	00	Clock Select 1 and 0 Select the A/D conversion time. (Pϕ/4 is set in this sample application.)
5, 4	ADM[1:0]	01	A/D Mode 1 and 0 Select the A/D conversion mode. (4-channel scan mode is selected in this sample application.)
3	ADCS	1	A/D Continuous Scan Continuous scan mode is selected in this sample application.
2 to 0	CH[2:0]	011	Channel Select 2 to 0 Select analog input channels for A/D conversion. (Channels AN0 to AN3 are selected in this sample application.)

2. A/D Control Register _0 (ADCR_0)
   Function: Controls A/D conversion.
   Set value: H'0000

Bit	Bit Name	Set Value	Description
15, 14	—	All 0	Reserved
13	ADST	0	A/D Start When cleared to 0, A/D conversion is stopped and the A/D converter enters the idle state. When set to 1, A/D conversion is started. Cleared to 0 automatically in single mode when A/D conversion end on the selected single channel.
12 to 0	—	All 0	Reserved

3. A/D Trigger Select Register_0 (ADTSR_0)
   Function: Enables an A/D conversion started by an external trigger signal.
   Set value: H'0000 (initial value)

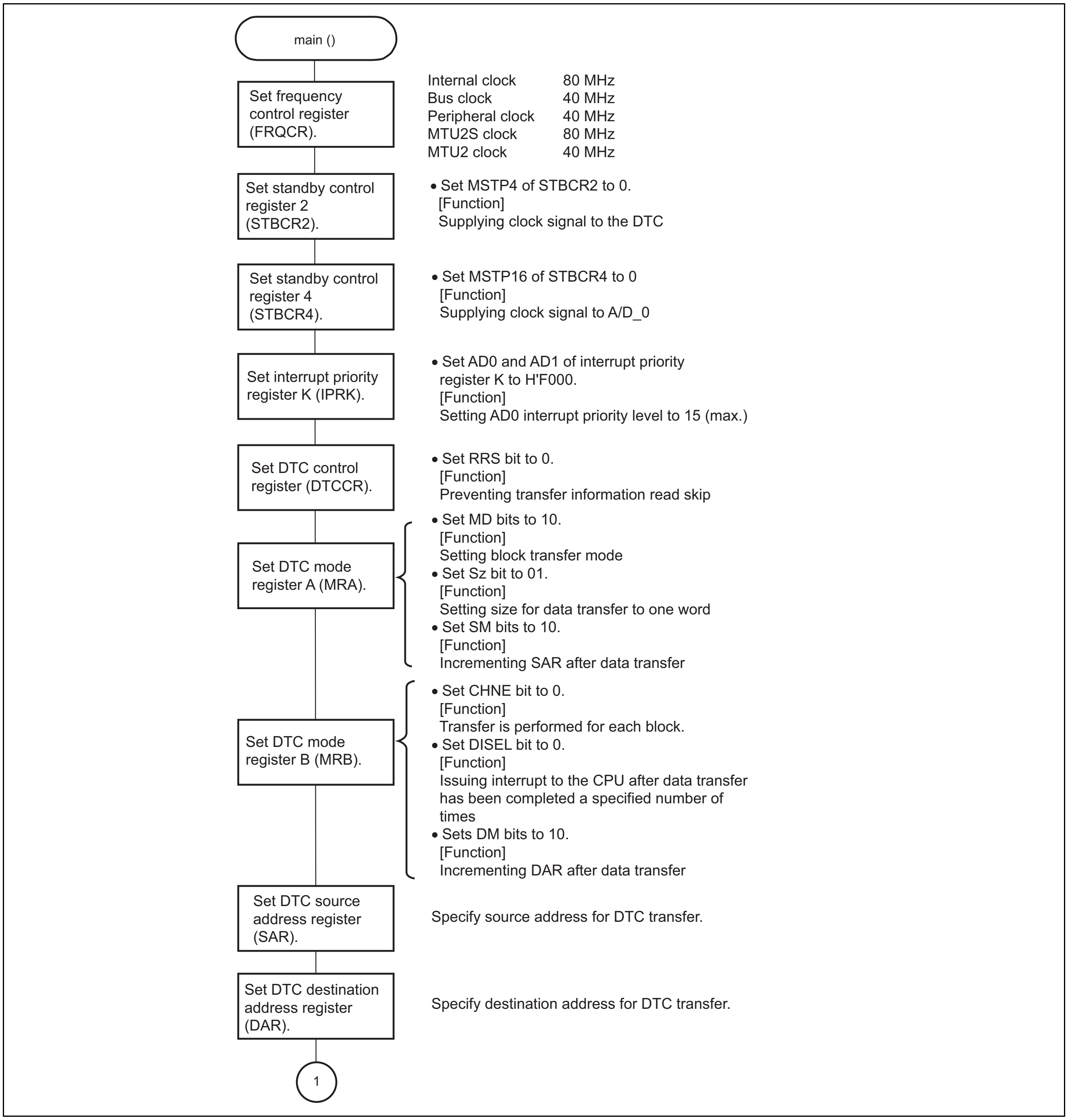
   An external trigger signal is not used in this sample application. Thus, ADSTR_0 is not set and its the values are used on an as-is basis.

Bit	Bit Name	Initial Value	Description
15 to 12	TRG11S[3:0]	0000	A/D Trigger 1 Group 1 Select 3 to 0 Select an external trigger, MTU2 trigger or MTU2S trigger to start A/D conversion for group 1 when A/D module 1 is in 2-channel scan mode.
11 to 8	TRG01S[3:0]	0000	A/D Trigger 0 Group 1 Select 3 to 0 Select an external trigger, MTU2 trigger or MTU2S trigger to start A/D conversion for group 1 when A/D module 0 is in 2-channel scan mode.
7 to 4	TRG1S[3:0]	0000	A/D Trigger 1 Select 3 to 0 Select an external trigger, MTU2 trigger or MTU2S trigger to start A/D conversion for A/D module 1.
3 to 0	TRG0S[3:0]	0000	A/D Trigger 0 Select 3 to 0 Select an external trigger, MTU2 trigger or MTU2S trigger to start A/D conversion for A/D module 1.

6. Flowcharts

Flowcharts for this sample application are given below.

6.1 Main Routine



Internal clock	80 MHz
Bus clock	40 MHz
Peripheral clock	40 MHz
MTU2S clock	80 MHz
MTU2 clock	40 MHz

- Set MSTP4 of STBCR2 to 0.
  [Function]
  Supplying clock signal to the DTC

- Set MSTP16 of STBCR4 to 0
  [Function]
  Supplying clock signal to A/D_0

- Set AD0 and AD1 of interrupt priority register K to H'F000.
  [Function]
  Setting AD0 interrupt priority level to 15 (max.)

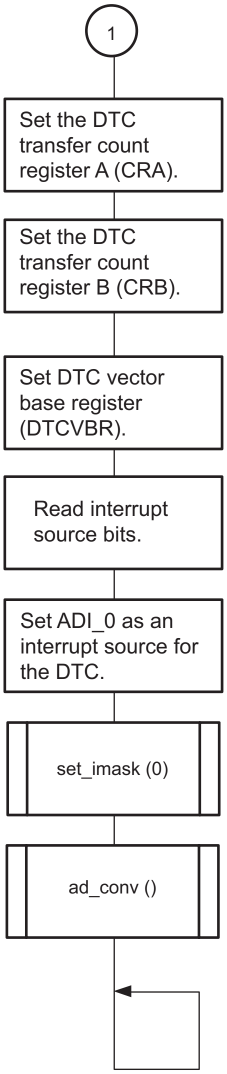
- Set RRS bit to 0.
  [Function]
  Preventing transfer information read skip

- Set MD bits to 10.
  [Function]
  Setting block transfer mode
- Set Sz bit to 01.
  [Function]
  Setting size for data transfer to one word
- Set SM bits to 10.
  [Function]
  Incrementing SAR after data transfer

- Set CHNE bit to 0.
  [Function]
  Transfer is performed for each block.
- Set DISEL bit to 0.
  [Function]
  Issuing interrupt to the CPU after data transfer has been completed a specified number of times
- Sets DM bits to 10.
  [Function]
  Incrementing DAR after data transfer

Specify source address for DTC transfer.

Specify destination address for DTC transfer.



- Set CRA to H'0404.
  [Function]
  Setting the block size to 4 words

- Set CRB to H'0004.
  [Function]
  Setting the block-data transfer count to 4 words

Specify DTC base address in RAM.

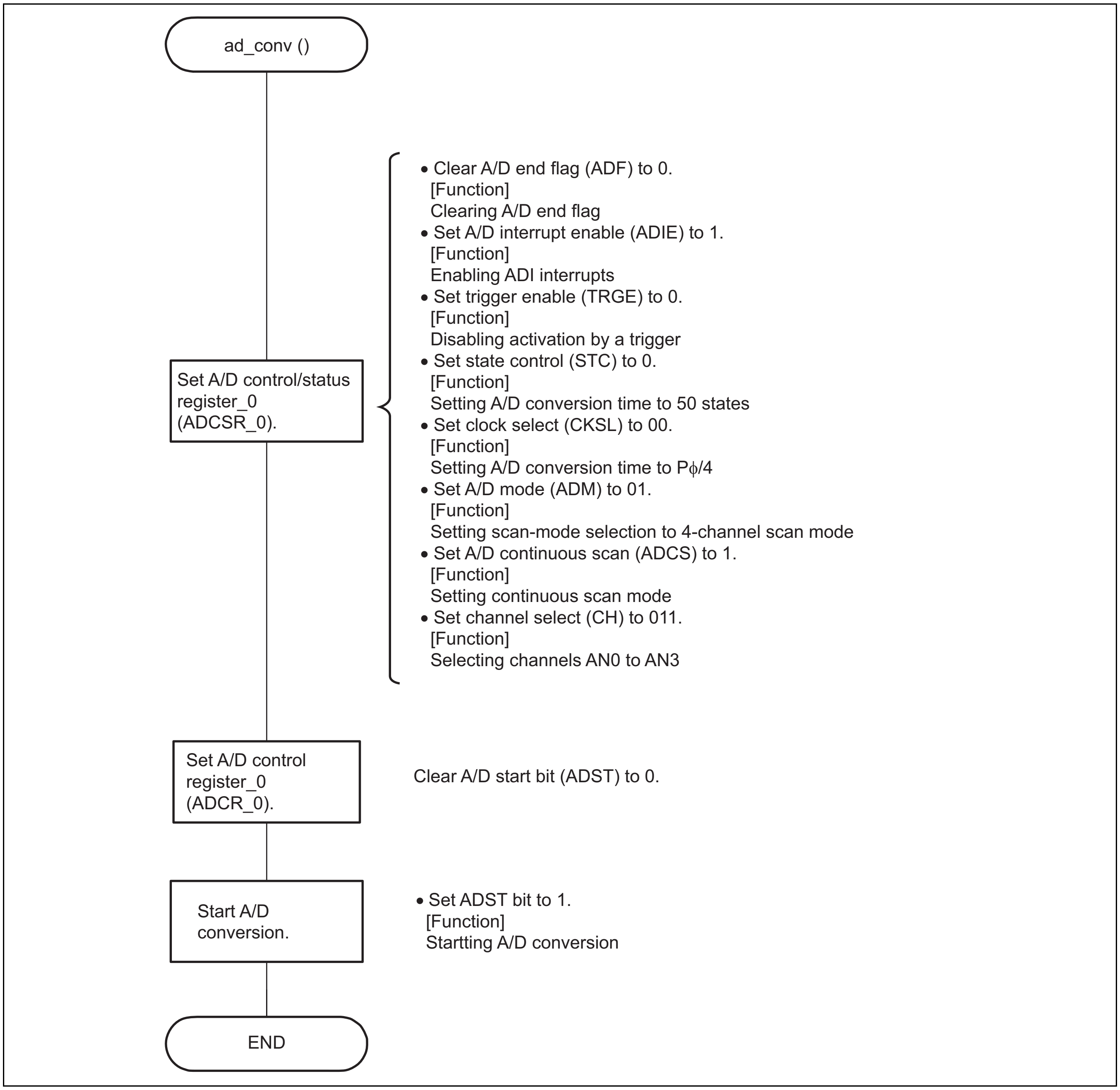
Prepare for writing interrupt source bits.

Set ADI_0 as an interrupt source that initiates transfer by the DTC.

Clear the interrupt mask level to enable interrupts.

Perform A/D conversion.

6.2 A/D Conversion Routine

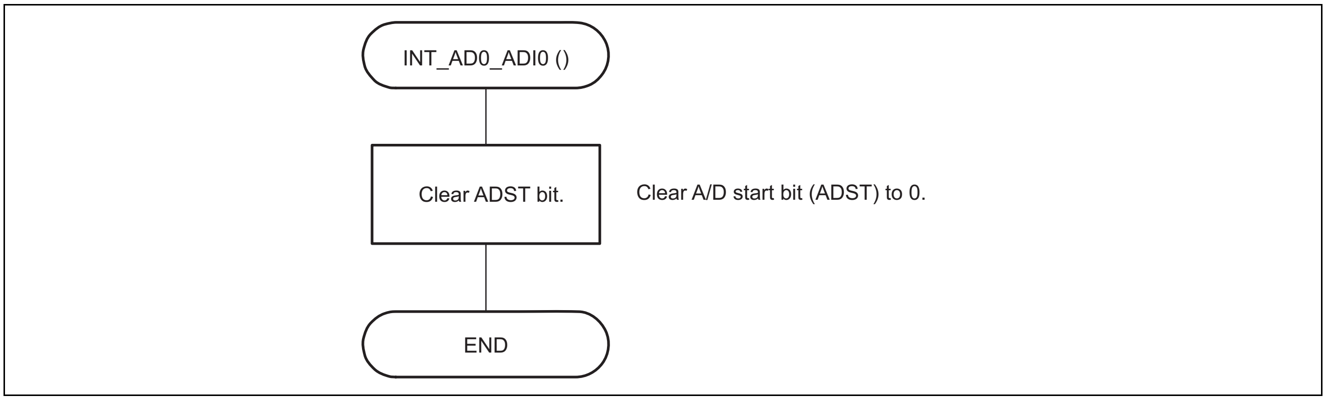


- Clear A/D end flag (ADF) to 0.
  [Function]
  Clearing A/D end flag
- Set A/D interrupt enable (ADIE) to 1.
  [Function]
  Enabling ADI interrupts
- Set trigger enable (TRGE) to 0.
  [Function]
  Disabling activation by a trigger
- Set state control (STC) to 0.
  [Function]
  Setting A/D conversion time to 50 states
- Set clock select (CKSL) to 00.
  [Function]
  Setting A/D conversion time to Pϕ/4
- Set A/D mode (ADM) to 01.
  [Function]
  Setting scan-mode selection to 4-channel scan mode
- Set A/D continuous scan (ADCS) to 1.
  [Function]
  Setting continuous scan mode
- Set channel select (CH) to 011.
  [Function]
  Selecting channels AN0 to AN3

Clear A/D start bit (ADST) to 0.

- Set ADST bit to 1.
  [Function]
  Startting A/D conversion

6.3 ADI Interrupt Routine



7. Documents for Reference

- Software Manual
  SH-1/SH-2/SH-DSP Software Manual
  The most up-to-date version of this document is available on the Renesas Technology Website.

- Hardware Manual
  SH7080 Group Hardware Manual
  The most up-to-date version of this document is available on the Renesas Technology Website.

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Revision Record

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