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Renesas Electronics Corporation

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H8/300H Tiny Series

Counting Timer Z External Input Clocks

Introduction

Timer Z is used to count the rising edges of the external clock signal that is input through the FTIOA0 pin.

Target Device

H8/3687

Contents

1. Specifications

1. Timer Z is used to count the rising edges of the external clock signal that is input through the FTIOA0 pin.
2. Timer counter 0 (TCNT0) is configured to count at the rising edges of an external clock and continues counting until it reaches 1024.
3. If TCNT0 reaches 1024, the external clock supply to TCNT0 is stopped and processing ends.

2. Description of Functions

1. In this sample task, timer Z0 is used to count the rising edges of the pulses input through the FTIOA0 pin. Figure 2.1 is a block diagram of timer Z. The elements in the block diagram are described below.

- Timer control register 0 (TCR0) selects TCNT0 input clock and clearing method. In this sample task, this register is set so that the TCNT0 counts the rising edges of an external clock and is cleared on a compare-match/input-capture with GRA0.
- Timer I/O control register A0 (TIORA0) controls GRA0. In this sample task, GRA0 is used as an input-capture register and the output on the FTIOA0 pin upon a compare-match is disabled.
- Timer status register 0 (TSR0) indicates the timer Z status. In this sample task, the input-capture/compare-match flag A (IMFA) is set to 1 on a compare-match with GRA.
- Timer interrupt enable register (TIER0) enables or disables various interrupt requests. In this sample task, interrupt requests by the IMFA flag of TSR0 is enabled and other interrupt requests are disabled.
- Timer counter 0 (TCNT0) is a 16-bit readable/writable upward counter that is incremented by an internal clock or external clock input. In this sample task, TCNT0 is incremented at the rising edge of an external clock.
- General register A0 (GRA0) a 16-bit readable/writable register. In this sample task, the value of GRA0 is always compared with that of TCNT0 and the IMFA flag of TSR0 is set to 1 if GRA0 matches TCNT0. If IMIEA of TIER0 is set to 1 while IMFA is set to 1, an interrupt is requested to the CPU.
- Timer start register (TSTR) starts or stops the TCNT0 and TCNT1 operation. In this sample task, TCNT0 is specified to start counting and TCNT1 is specified to stop counting.
- Timer mode register (TMDR) selects synchronous or independent operation of TCNT0 and TCNT1. In this sample task, TCNT0 operates independently of TCNT1.
- Timer function control register (TFCR) specifies operation modes and selects an output level. In this sample task, an external clock input is enabled and channels 0 and 1 are specified for normal operation.
- Timer output master enable register (TOER) enables or disables outputs on channels 0 and 1. In this sample task, the FTIOA0 output is disabled.

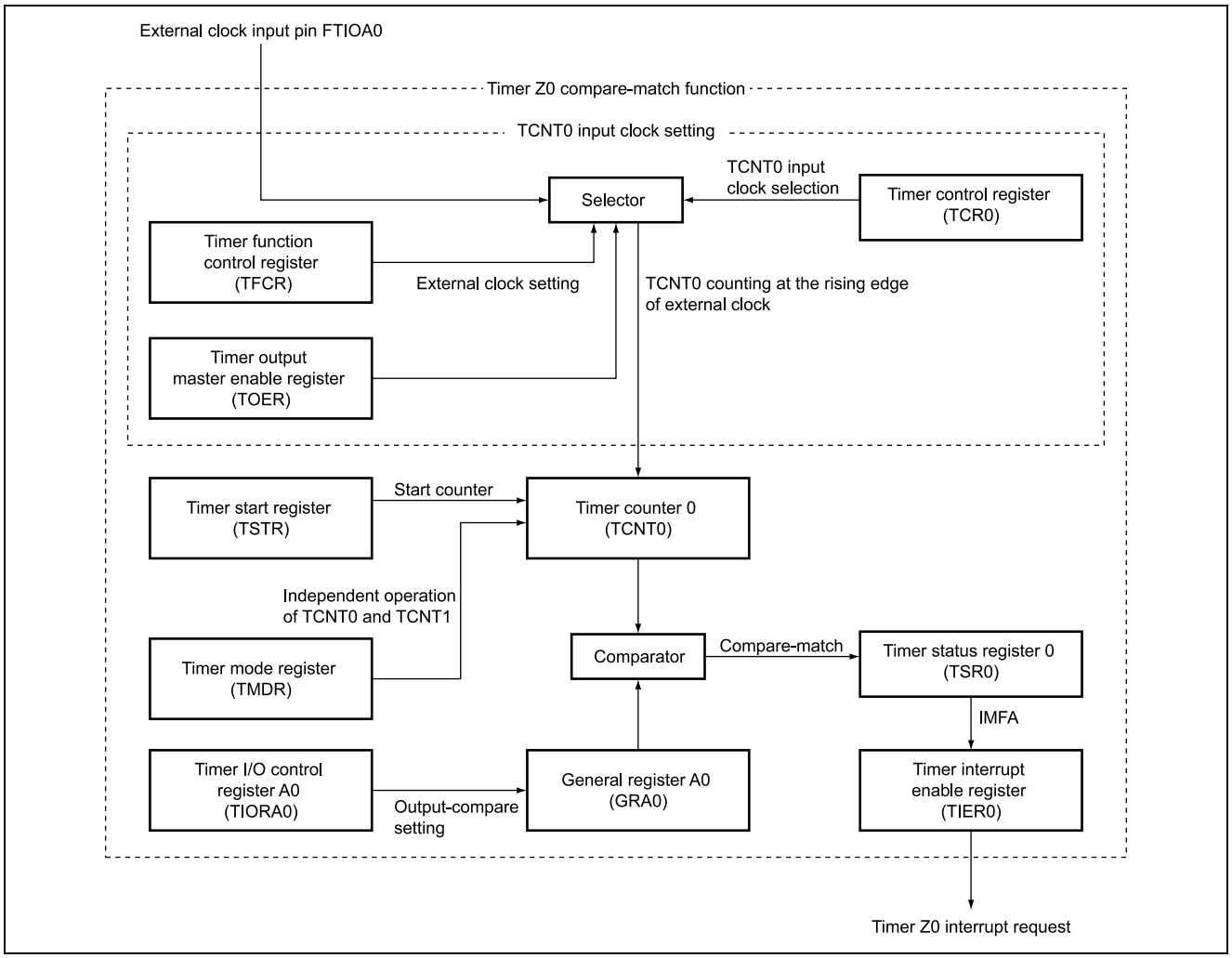


Figure 2.1 Block Diagram of Timer Z0 Counting Externally Input Clock

2. Table 2.1 lists the function allocation for this sample task. The functions listed in this table are allocated so that the timer Z counts cycles of an external input clock.

Table 2.1 Function Allocation

Function	Description
TCR0	Specifies the TCNT0 input clock.
TIORA0	Specifies GRA0 as an output-compare register.
TSR0	Flag control by compare-match with GRA0.
TIER0	Enables GRA0 compare-match interrupt requests.
TCNT0	16-bit counter that is incremented at the rising edge of an external clock.
GRA0	Stores the external input clock count.
TSTR	Controls TCNT0 count start and stop.
TMDR	Selects independent operation of TCNT0 and TCNT1.
TFCR	Specifies external clock input, and specifies channels 0 and 1 for normal operation.
TOER	Disables the FTIOA0 pin output.
FTIOA0 pin	External clock input pin

3. Description of Operation

Operation of this sample task is described in figure 3.1. Hardware and software processing are applied in the way shown in figure 3.1 to count cycles of an external input clock supplied to timer Z0.

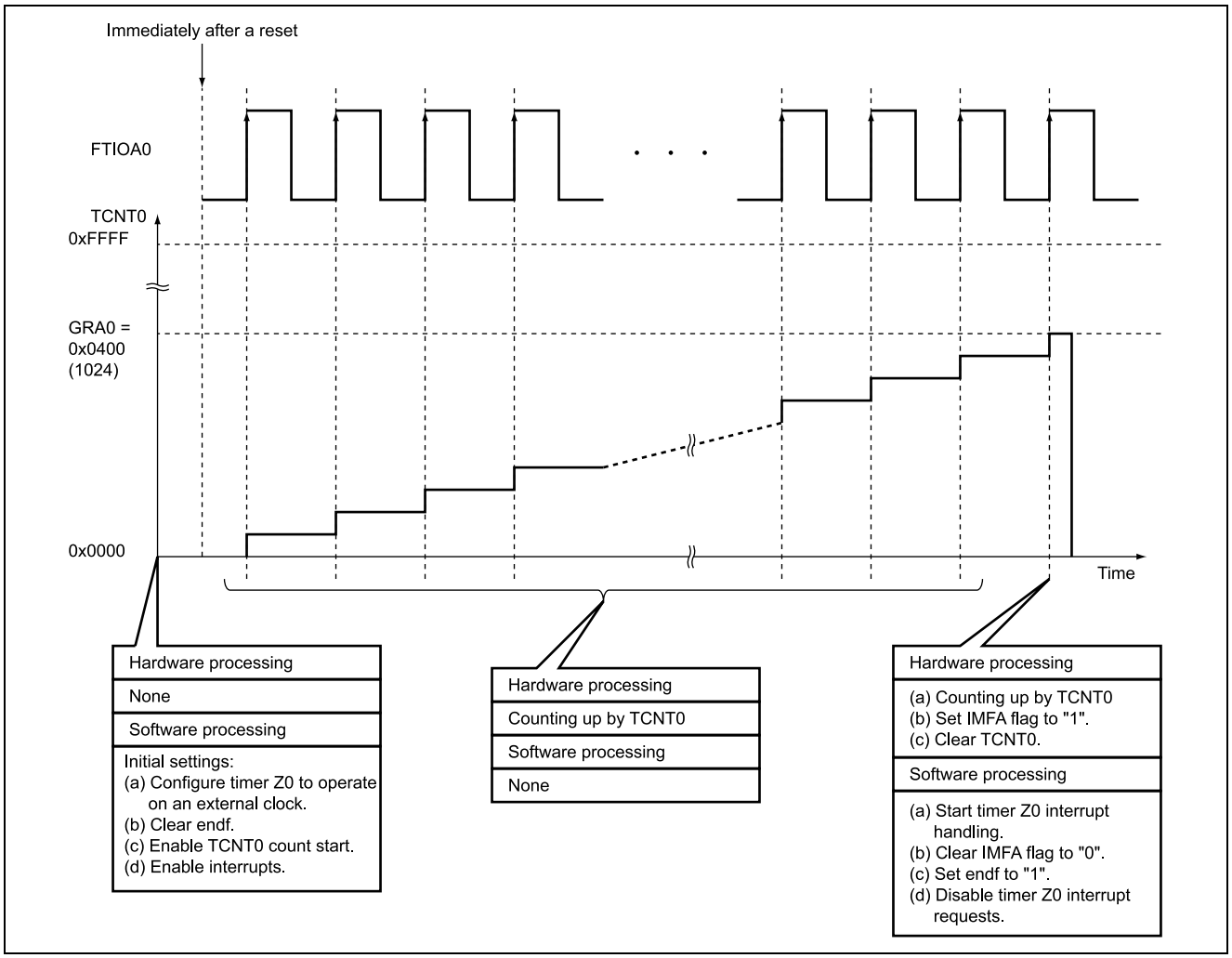


Figure 3.1 Principle of Operation

4. Description of Software

4.1 Modules

Table 4.1 lists the modules used in this sample task.

Table 4.1 Description of Modules

Module Name	Label Name	Function
Main routine	main	Selects an external clock for timer Z0 and compare-match function, starts counting by TCNT0, and provides settings for interrupts.
Measurement end	tz0int	Performs timer Z0 interrupt handling. Sets endf to 1 and disables timer Z0 interrupts.

4.2 Arguments

This sample task uses no arguments.

4.3 Internal Registers

The internal registers used in this sample task are described below.

- TCR0 Timer control register 0 Address: 0xF700

Bit	Bit Name	Setting	Function
7	CCLR2	CCLR2 = 0	Counter clear 2 to 0
6	CCLR1	CCLR1 = 0	CCLR2 = 0, CCLR1 = 0, CCLR0 = 1:
5	CCLR0	CCLR0 = 1	Clears the TCNT0 on compare-match/input-capture with GRA0.
4	CKEG1	CKEG1 = 0	Clock edge 1 to 0
3	CKEG0	CKEG0 = 0	CKEG1 = 0, CKEG0 = 0: Counts at the rising edge of the clock
2	TPSC2	TPSC2 = 1	Timer prescaler 2 to 0
1	TPSC1	TPSC1 = 0	TPSC2 = 1, TPSC1 = x, TPSC0 = x:
0	TPSC0	TPSC0 = 0	Counts by an external clock (x: Don't care).

- TIORA0 Timer I/O control register A0 Address: 0xF701

Bit	Bit Name	Setting	Function
2	IOA2	IOA2 = 0	I/O control A2 to A0
1	IOA1	IOA1 = 0	IOA2 = 0, IOA1 = 0, IOA0 = 0:
0	IOA0	IOA0 = 0	Specifies the GRA as an output-compare register and disables the pin output on a compare-match.

- TSR0 Timer status register 0 Address: 0xF703

Bit	Bit Name	Setting	Function
0	IMFA	0	Input-capture/compare-match flag A IMFA = 0: Indicates that the GRA0 does not match TCNT0. IMFA = 1: Indicates that the GRA0 matches TCNT0.

- TIER0 Timer interrupt enable register 0 Address: 0xF704

Bit	Bit Name	Setting	Function
0	IMIEA	1	Input-capture/compare-match interrupt enable A When IOA2 of TIORA0 is set to 0 (i.e. output-compare is selected), IMIEA = 0: Disables interrupts by the IMFA flag of TSR0. IMIEA = 1: Enables interrupts by the IMFA flag of TSR0.

- TCNT0 Timer counter 0 Address: 0xF706

  Function: A 16-bit upward counter that is incremented at the rising edge of an external clock.

  Setting: 0x0000

- GRA0 General register A0 Address: 0xF708

  Function: A compare-match is generated if the GRA0 value matches TCNT0 counter value.

  Setting: 0x04000

- TSTR Timer start register Address: 0xF720

Bit	Bit Name	Setting	Function
0	STR0	0	Channel 0 counter start STR0 = 0: Stops counting by TCNT0. STR0 = 1: Starts counting by TCNT0.

- TMDR Timer mode register Address: 0xF721

Bit	Bit Name	Setting	Function
0	SYNC	0	Timer synchronization SYNC = 0: TCNT0 operates independently of TCNT1. SYNC = 1: TCNT0 operates synchronously with TCNT1.

- TFCR Timer function control register Address: 0xF723

Bit	Bit Name	Setting	Function
6	STCLK	1	External clock input select STCLK = 0: Disables external clock input. STCLK = 1: Enables external clock input.
1	CMD1	CMD1 = 0	Combination mode 1 to 0
0	CMD0	CMD0 = 0	CMD1 = 0, CMDk0 = 0: Channels 0 and 1 operates in normal operation mode.

- TOER Timer output master enable register Address: 0xF724

Bit	Bit Name	Setting	Function
0	EA0	1	Master enable A0 EA0 = 0: Enables the FTIOA0 pin output. EA0 = 1: Disables the FTIOA0 pin output.

- PCR6 Port control register 6 Address: 0xFFE9

Bit	Bit Name	Setting	Function
0	PCR60	0	Port control register 60 PCR60 = 0: Specifies P60/FTIOA0 pin as an input pin. PCR60 = 1: Specifies P60/FTIOA0 pin as an output pin.

4.4 Description of RAM

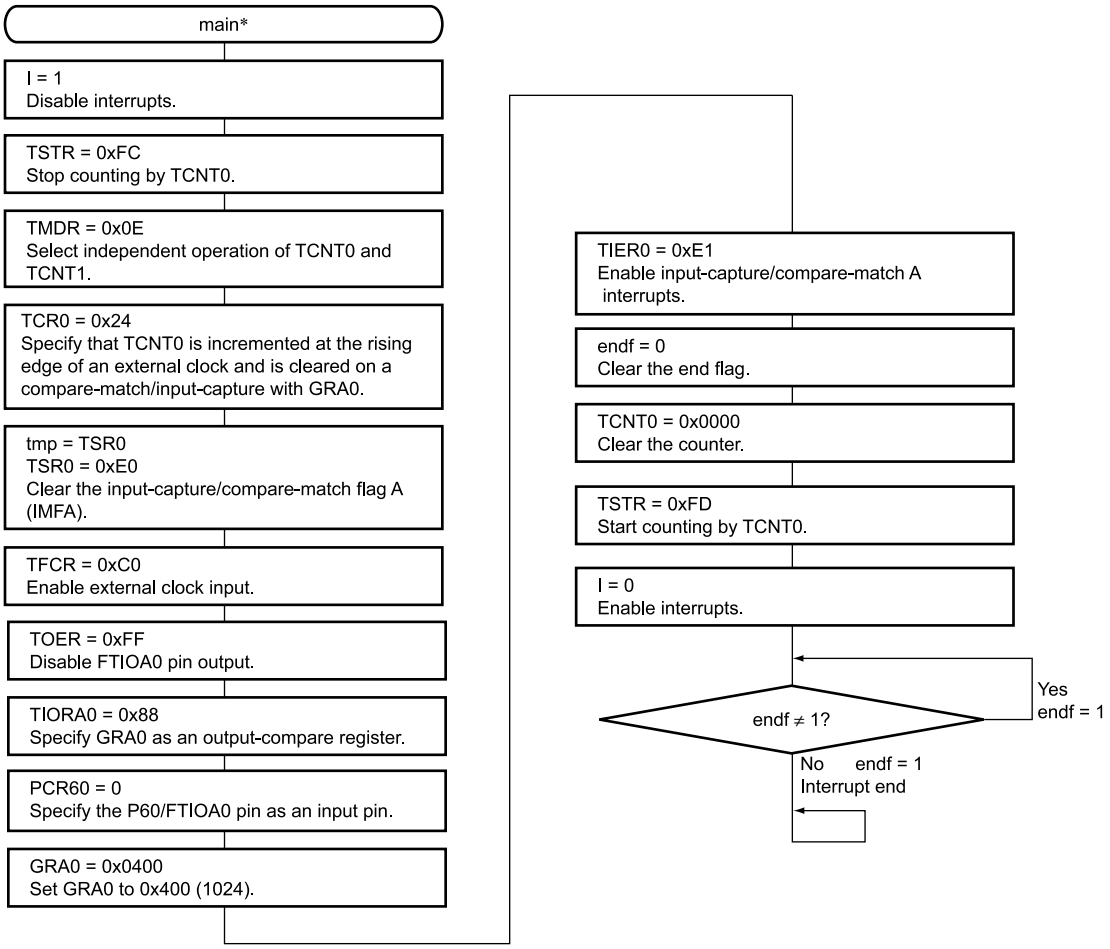
Table 4.2 describes the RAM used in this sample task.

Table 4.2 Description of RAM

Label Name	Function	Size	Used in
endf	A flag indicating that the rising edge of the input clock has been detected 1024 times.	1 byte	Main routine Measurement end

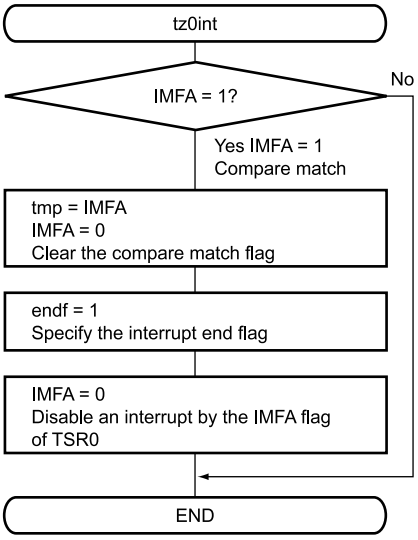
5. Flowcharts

1. Main routine



Note: * The stack pointer is specified by INIT.SRC (assembly language).

2. Cycle measurement end



6. Program List

```
/************************************************************************************************************************/
/*                                                                                                                      */
/*   H8/300HN Series -H8/3687-                                                                                          */
/*   Application Note                                                                                                   */
/*                                                                                                                      */
/*   'External clock count Function'                                                                                    */
/*                                                                                                                      */
/*   Function                                                                                                           */
/*   : Timer Z 16bit External clock count                                                                               */
/*                                                                                                                      */
/*   External Clock :    16MHz                                                                                          */
/*   Internal Clock :    16MHz                                                                                          */
/*   Sub Clock :         32.768kHz                                                                                      */
/*                                                                                                                      */
/************************************************************************************************************************/

#include    <machine.h>

/************************************************************************************************************************/
/*   Symbol Definition                                                                                                  */
/************************************************************************************************************************/
struct BIT {
     unsigned char   b7:1;         /* bit7 */
     unsigned char   b6:1;         /* bit6 */
     unsigned char   b5:1;         /* bit5 */
     unsigned char   b4:1;         /* bit4 */
     unsigned char   b3:1;         /* bit3 */
     unsigned char   b2:1;         /* bit2 */
     unsigned char   b1:1;         /* bit1 */
     unsigned char   b0:1;         /* bit0 */
};

#define        TCR0           *(volatile unsigned char *)0xF700                  /* Timer control register_0                */
#define        TIORA0         *(volatile unsigned char *)0xF701                  /* Timer I/O Control Register A_0          */
#define        TSR0           *(volatile unsigned char *)0xF703                  /* Timer status register_0                 */
#define        TSR0_BIT       (*(struct BIT *)0xF703)                            /* Timer status register_0                 */
#define        IMFA           TSR0_BIT.b0                                        /* Input Capture/Compare Match FlagA       */
#define        TIER0          *(volatile unsigned char *)0xF704                  /* Timer interrupt enable register0        */
#define        TIER0_BIT      (*(struct BIT *)0xF704)                            /* Timer interrupt enable register0        */
#define        IMIEA          TIER0_BIT.b0                                       /* Input Capture/Compare Match             */
                                                                                 /* Interrupt Enable A                      */
#define        TCNT0          *(volatile unsigned short *)0xF706                 /* Timer counter_0                         */
#define        GRA0           *(volatile unsigned short *)0xF708                 /* General register A_0                    */
#define        TSTR           *(volatile unsigned char *)0xF720                  /* Timer start register                    */
#define        TMDR           *(volatile unsigned char *)0xF721                  /* Timer mode register                     */
#define        TFCR           *(volatile unsigned char *)0xF723                  /* Timer function control register         */
#define        TOER           *(volatile unsigned char *)0xF724                  /* Timer output master enable register     */
#define        PCR6           *(volatile unsigned char *)0xFFE9                  /* Port Control Register 6                 */
#define        PCR6_BIT       (*(struct BIT *)0xFFE9)                            /* Port Control Register 6                 */
#define        PCR60          PCR6_BIT.b0                                        /* Port Control Register 60                */

#pragma interrupt   (tz0int)
```

```
/************************************************************************************************************************/
/*   Function define                                                                                                    */
/************************************************************************************************************************/
extern void INIT ( void );                                          /* SP Set                                           */
void main ( void );
void tz0int ( void );

/************************************************************************************************************************/
/*   RAM define                                                                                                         */
/************************************************************************************************************************/
volatile unsigned char  endf;                                       /* End Flag                                         */

/************************************************************************************************************************/
/*   Vector Address                                                                                                     */
/************************************************************************************************************************/
#pragma section     V1                                              /* VECTOR SECTOIN SET                               */
void (*const VEC_TBL1[])(void) = {                                  /* 0x00 - 0x0f                                      */
     INIT                                                           /* 00 Reset                                         */
};
#pragma section     V2                                              /* VECTOR SECTOIN SET                               */
void (*const VEC_TBL2[])(void) = {
     tz0int                                                         /* 34 Timer Z0 Interrupt                            */
};

#pragma section                                                     /* P                                                */
/************************************************************************************************************************/
/*   Main Program                                                                                                       */
/************************************************************************************************************************/
void main ( void )
{
     unsigned char tmp;

     set_imask_ccr(1);                                              /* Interrupt Disable                                */

     TSTR = 0xFC;                                                   /* TCNT0 count stop                                 */
     TMDR = 0x0E;                                                   /* TCNT0,TCNT1 Single Mode                          */
     TCR0 = 0x24;                                                   /* Rising edge, Outside Clock count                 */
     tmp = TSR0;
     TSR0 = 0xE0;                                                   /* Interrupt Flag Clear                             */
     TFCR = 0xC0;                                                   /* External clock input is enabled                  */
     TOER = 0xFF;                                                   /* FTIOA0 Input Enable                              */
     TIORA0 = 0x88;                                                 /* Disables FTIOA0 output                           */
     PCR60 = 0;                                                     /* P60 input/FTIOA0 input pin                       */
     GRA0 = 0x0400;                                                 /* Set input clock maximum value                    */
     TIER0 = 0xE1;                                                  /* IMFA Interrupt Enable                            */
     endf = 0;                                                      /* Clear end flag                                   */
     TCNT0 = 0x0000;                                                /* Clear TCNT0                                      */
     TSTR = 0xFD;                                                   /* TCNT0 count start                                */

     set_imask_ccr(0);                                              /* Interrupt Enable                                 */
     while(endf != 1);

     while(1);
}
```

```
/************************************************************************************************************************************/
/*   Timer Z0 Interrupt                                                                                                             */
/************************************************************************************************************************************/
void tz0int ( void )
{
     unsigned char tmp;

     if(IMFA == 1){                                                    /* Interrupt by IMFA flag                  */
          tmp = IMFA;
          IMFA = 0;                                                    /* Clear IMFA flag                         */
          endf = 1;                                                    /* Set end flag                            */
          IMIEA = 0;                                                   /* IMFA Interrupt Disable                  */
     }
}
```

Link address specifications

Section Name	Address
CV1	0x0000
CV2	0x0034
P	0x0100
B	0xFB80

Revision Record

		Description	
Rev.	Date	Page	Summary
1.00	Sep.29.03	—	First edition issued

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