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Renesas Electronics Corporation

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H8/300H Tiny Series

Conversion from Single-Precision Floating-Point to Signed 32-bit Binary (FKTR)

Introduction

Converts a single-precision floating-point number in general registers to a signed 32-bit binary number.

Target Device

H8/300H Tiny Series

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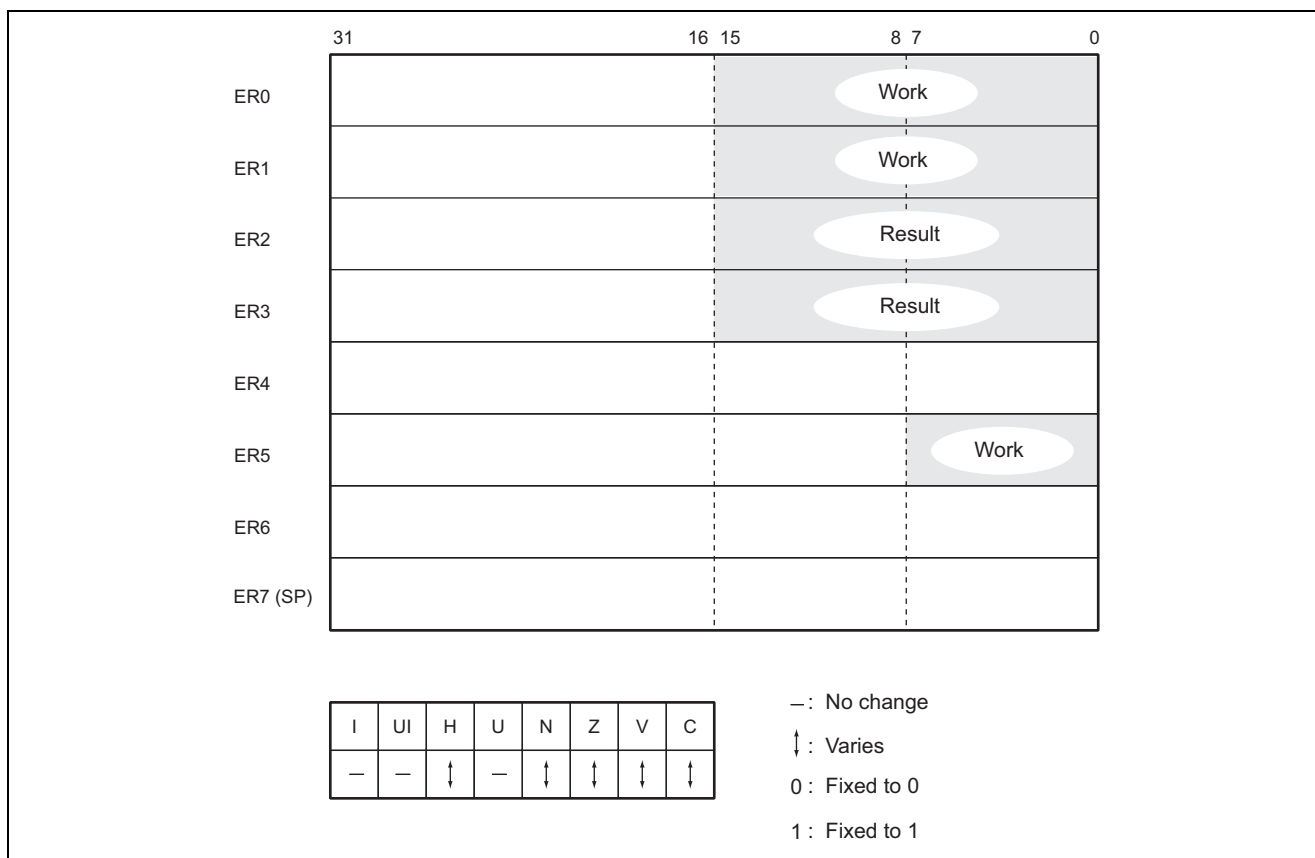
1. Function

1. Converts a single-precision floating-point number in general registers to a signed 32-bit binary number.
2. When the single-precision floating-point number is a zero, the output is also zero.
3. When the single-precision floating-point number has an absolute value greater than or equal to 2^{31} , the maximum value with the corresponding sign ($2^{31} - 1$ or -2^{31}) is output. Zero is output in response to absolute values less than one.

2. Arguments

Contents		Storage Location	Data Length (Bytes)
Input	Single-precision floating-point number	R0, R1	4
Output	Signed 32-bit binary number	R2, R3	4

3. Changes to Internal Registers and Flags



4. Programming Specifications:

Program memory (bytes)	100
Data memory (bytes)	0
Stack (bytes)	0
Number of cycles	108
Re-entrant	Yes
Relocatable	Yes
Interrupts during execution	Yes

5. Note

The number of cycles given in the programming specifications is the value for execution of the example in figure 1. For details on the floating-point data format, refer to Reference: Description of Single-Precision Floating-Point Formats.

6. Descriptions

6.1 Descriptions of Functions

1. The arguments are listed below.
 - 1) Set the input argument.
 - R0: higher-order two bytes of the single-precision floating-point number
 - R1: lower-order two bytes of the single-precision floating-point number
 - 2) The FKTR subroutine sets the output argument.
 - R2: higher-order two bytes of the signed 32-bit binary number
 - R3: lower-order two bytes of the signed 32-bit binary number
2. The following figure illustrates the execution of the FKTR subroutine. When the input argument is set as shown below, the subroutine places the result of conversion in R2 and R3.

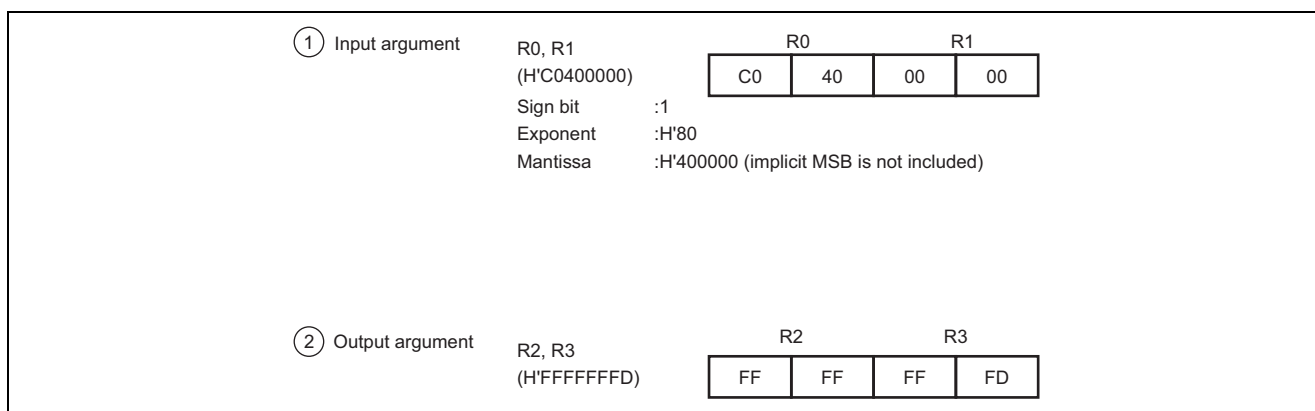


Figure 1 Example of FKTR Execution

6.2 Usage Notes

1. Zero is the output when the single-precision floating-point number is zero or has an absolute value smaller than one.
2. When the absolute value of the single-precision floating-point number is 2^{31} or greater, the maximum value with the same sign (H'7FFFFFFF or H'80000000) is output.
3. The input argument set in R0 and R1 is lost in the execution of FKTR. When you will still require the input argument, save it elsewhere in memory before executing FKTR.

6.3 Description of Data Memory

No data memory is used by FKTR.

6.4 Example of Usage

After setting a single-precision floating-point number in the general registers, call the FKTR subroutine.

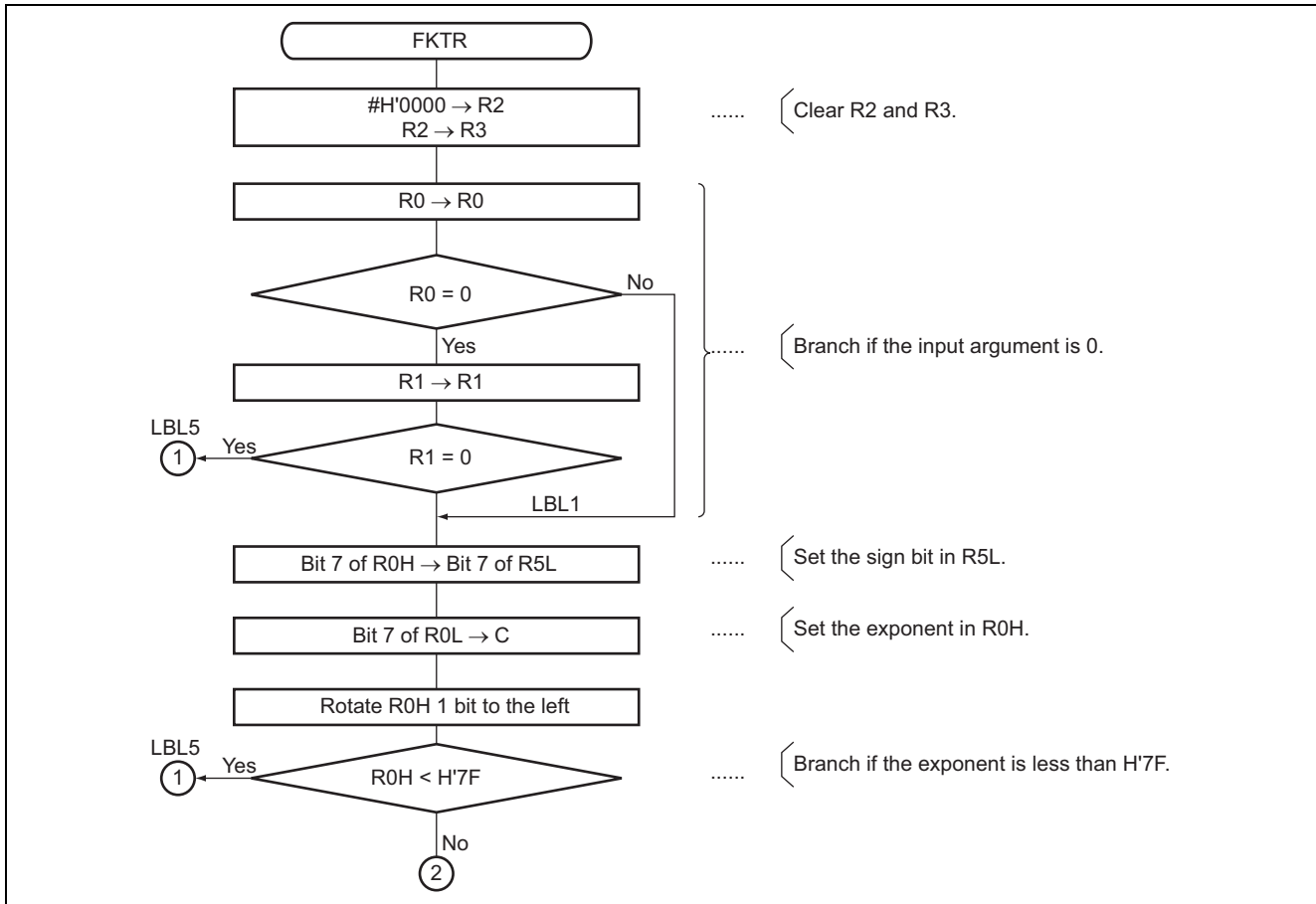
WORK1	. RES. W 2, 0	Reservation of the data memory area for setting of the single-precision floating point number by the user program.
WORK2	. RES. W 2, 0	Reservation of the data memory area where the signed 32-bit binary number will be placed for the user program.
	.		
	.		
	MOV. W @WORK1, R0	Sets the single-precision floating point number specified by the user program as the input argument
	MOV. B @WORK1+2, R1		
	JSR @FKTR	Subroutine call of the software FKTR
	MOV. W R2, @WORK2	Transfers the signed 32-bit binary number from the output argument to the data memory area.
	MOV. W R3, @WORK2+2		

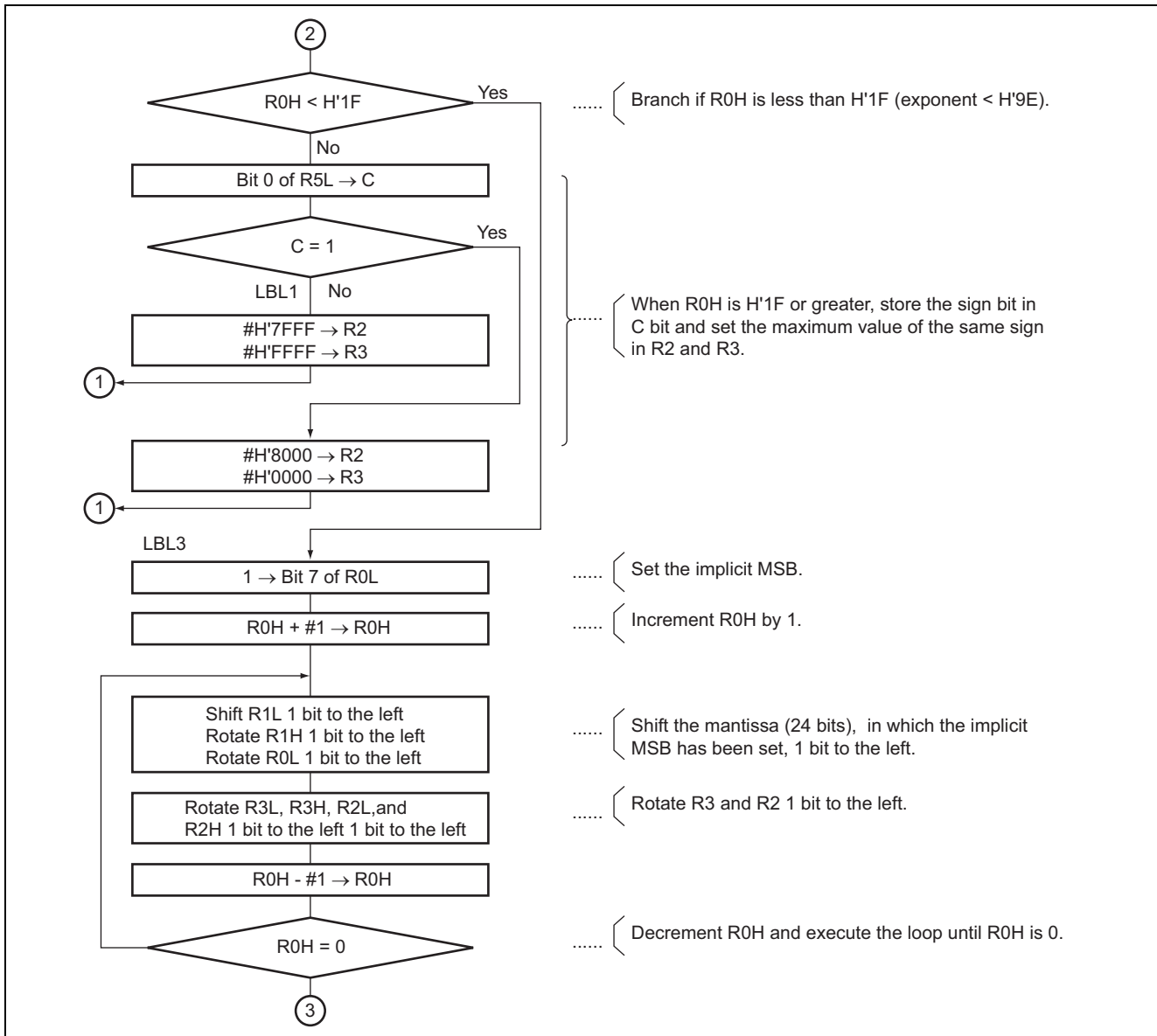
6.5 Principles of Operation

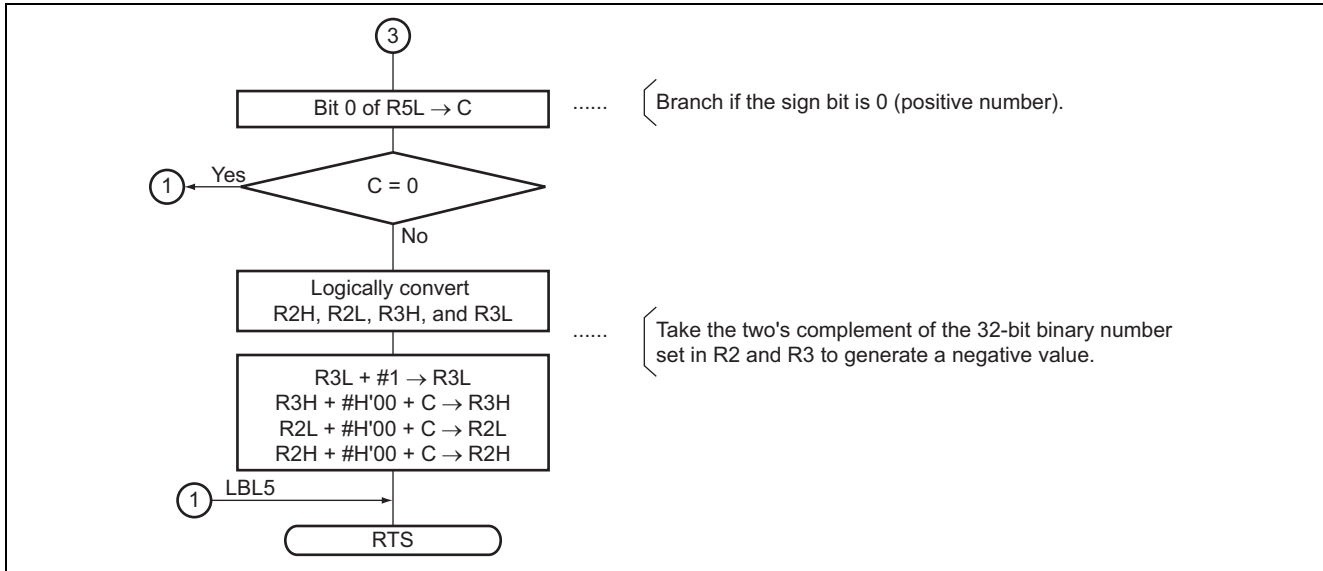
The FKTR subroutine converts the single-precision floating-point number to a signed 32-bit binary number in the following sequence.

1. Firstly, FKTR checks the input argument.
 - 1) If the single-precision floating-point number is zero, zero is output.
 - 2) If the exponent is less than H'7F, zero is output.
 - 3) If the exponent is H'9E or greater, the maximum value with the same sign is output.
2. When the input argument is not zero and its absolute value is one or greater (i.e., exponent is at least H'7F) but less than 2^{31} (i.e., exponent is less than H'9E), the subroutine:
 - 1) sets the implicit MSB;
 - 2) shift the mantissa (24 bits), in which the implicit MSB has been set, 1 bit to the left;
 - 3) rotates R3 and R2 one bit to the left;
 - 4) repeats steps 2) and 3) (R0H +1) times;
 - 5) tests the sign bit—if it is negative, takes the two's complement to make the number negative.

7. Flowchart







8. Program Listing

```

1          1          ;*****
2          2          ;*
3          3          ;*      NAME:  CHANGE FLOATING POINT TO 32 BIT BINARY  *
4          4          ;*      (FKTR)
5          5          ;*
6          6          ;*****
7          7          ;*
8          8          ;*      ENTRY:  R0      SINGLE PREC. NO. (UPPER 2 BYTES) *
9          9          ;*      R1      (LOWER 2 BYTES)
10         10         ;*
11         11         ;*      RETURNS: R2      SIGNED 32-BIT NO. (UPPER 2 BYTES) *
12         12         ;*      R3      (LOWER 2 BYTES)
13         13         ;*
14         14         ;*****
15         15         ;
16         16         .CPU      300HN
17 0000     17         .SECTION  FKTR_code, CODE, ALIGN=2
18         18         .EXPORT   FKTR
19         19         ;
20         20         FKTR     .EQU      $          ;Entry point
21 0000 79020000  21         MOV.W   #H'0000,R2    ;Clear R2
22 0004 0D23     22         MOV.W   R2,R3      ;Clear R3
23         23         ;
24 0006 0D00     24         MOV.W   R0,R0
25 0008 4604     25         BNE     LBL1
26 000A 0D11     26         MOV.W   R1,R1
27 000C 4754     27         BEQ     LBL5      ;Branch if R0=R1=0
28 000E         28         LBL1
29 000E 7770     29         BLD     #7,R0H
30 0010 670D     30         BST     #0,R5L      ;Set sign bit to bit0 of R5L
31 0012 7778     31         BLD     #7,R0L
32 0014 1200     32         ROTXL.B  R0H      ;Set exponent
33 0016 F57F     33         MOV.B   #H'7F,R5H
34 0018 1850     34         SUB.B   R5H,R0H
35 001A 4546     35         BCS     LBL5      ;Branch if R0<H'7F
36 001C A01F     36         CMP.B   #H'1F,R0H
37 001E 4518     37         BCS     LBL3      ;Branch if R0<H'1F
38 0020 770D     38         BLD     #0,R5L
39 0022 450A     39         BCS     LBL2      ;Branch if sign bit = 1
40 0024 79027FFF  40         MOV.W   #H'7FFF,R2
41 0028 7903FFFF  41         MOV.W   #H'FFFF,R3    ;Set H'7FFFFFFF
42 002C 4034     42         BRA     LBL5      ;Always branch
43 002E         43         LBL2
44 002E 79028000  44         MOV.W   #H'8000,R2
45 0032 79030000  45         MOV.W   #H'0000,R3    ;Set H'80000000
46 0036 402A     46         BRA     LBL5
47         47         ;
48 0038         48         LBL3
49 0038 7078     49         BSET   #7,R0L      ;Set implicit MSB
50 003A 8001     50         ADD.B   #1,R0H      ;R0H + #1 -> R0H
51 003C         51         LBL4
52 003C 1009     52         SHLL.B  R1L      ;Shift mantissa 1 bit left

```

```

53  003E 1201      53      ROTXL.B  R1H
54  0040 1208      54      ROTXL.B  R0L
55                55      ;
56  0042 120B      56      ROTXL.B  R3L      ;Rotate 32 bit binary 1 bit left
57  0044 1203      57      ROTXL.B  R3H
58  0046 120A      58      ROTXL.B  R2L
59  0048 1202      59      ROTXL.B  R2H
60  004A 1A00      60      DEC.B   R0H      ;Decrement R0H
61  004C 46EE      61      BNE    LBL4      ;Branch if Z=0
62                62      ;
63  004E 770D      63      BLD    #0,R5L     ;Bit load sign bit to C flag
64  0050 4410      64      BCC    LBL5      ;Branch if C=0
65  0052 1702      65      NOT   R2H      ;2's complement 32 bit binary
66  0054 170A      66      NOT   R2L
67  0056 1703      67      NOT   R3H
68  0058 170B      68      NOT   R3L
69  005A 8B01      69      ADD.B  #'01,R3L
70  005C 9300      70      ADDX.B #'00,R3H
71  005E 9A00      71      ADDX.B #'00,R2L
72  0060 9200      72      ADDX.B #'00,R2H
73                73      ;
74  0062            74      LBL5
75  0062 5470      75      RTS
76                76      ;
77                77      .END

*****TOTAL ERRORS      0
*****TOTAL WARNINGS    0

```

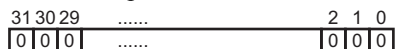
<Reference> Description of Single-Precision Floating-Point Formats

Single-Precision Floating-Point Formats:

1. Internal Representation of Single-Precision Floating Point Numbers

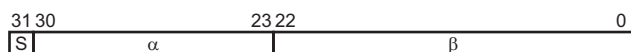
One of the following formats is used depending on the value of the single-precision floating-point data in this application note (a real number is indicated as R).

1) Internal Representation When R=0



All the 32 bits are 0.

2) Normalized Format



α is an index number with an 8-bit-long field. β is a mantissa with a 23-bit-long field. Here, the R value can be represented by the expression below (when $1 \leq \alpha \leq 254$).

↓Implicit MSB

$$R = 2^S \times 2^{\alpha-126} \times (1 + 2^{-1} \times \beta_{22} + 2^{-2} \times \beta_{21} + \dots + 2^{-23} \times \beta_0)$$

where, β_i is the value of the i-th bit of β ($0 \leq i \leq 22$), and S is the sign bit.

3) Denormalized Format



β is a mantissa with a 23-bit-long field. This format is used to represent a real number that is too small to be represented by the normalized format.

Here, the R value can be represented by the expression below.

$$R = 2^S \times 2^{-126} \times (2^{-1} \times \beta_{22} + 2^{-2} \times \beta_{21} + \dots + 2^{-23} \times \beta_0)$$

4) Infinity



β is a mantissa with a 23-bit-long field. Note that if all the bits in the index part are 1, the R value is handled as follows, in this application note.

When S = 0: Plus infinity

$$R = +\infty$$

When S = 1: Minus infinity

$$R = -\infty$$

2. Internal Representation Examples

$$S = B'0 \quad (\text{binary})$$

$$\alpha = B'10000011 \quad (\text{binary})$$

$$\beta = B'1011100\dots\dots 0 \quad (\text{binary})$$

Under the above conditions, the corresponding R value is represented as follows.

$$R = 2^0 \times 2^{131-126} \times (1 + 2^{-1} + 2^{-3} + 2^{-4} + 2^{-5})$$

$$= 16 + 8 + 2 + 1 + 0.5 = 27.5$$

1) Maximum and Minimum Values

Here, the maximum and minimum values are absolute values. The maximum value is indicated as R_{MAX} and the minimum value is indicated as R_{MIN}. Up to the following values can be represented.

$$R_{MAX} = 2^{254-127} \times (1 + 2^{-1} + 2^{-2} + 2^{-3} + \dots + 2^{-23})$$

$$\approx 3.27 \times 10^{38}$$

$$R_{MIN} = 2^{-126} \times 2^{-23} = 2^{-140} \approx 1.40 \times 10^{-45}$$

Revision Record

Rev.	Date	Description	
		Page	Summary
2.00	Feb.28.06	—	Format has been changed from Hitachi version to Renesas version.

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