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R8C/2F Group

Comparator

1. Abstract

This document describes a program for the comparator.

2. Introduction

The application example described in this document applies to the following MCU and condition(s):

- MCU : R8C/2F Group
- VCC, AVCC/VREF : 5 V

This program can be used with other R8C/Tiny Series MCUs which have analogous special function registers (SFRs) as the R8C/2F Group. Check the manual for any additions and modifications to functions. Careful evaluation is recommended before using this application note.



3. Application Example Description

The comparators compare reference input voltage and an analog input voltages. Comparator 0 and comparator 1 are two independent comparators.

The method for comparing a reference input voltage and an analog input voltage using comparator 0 is described here. Other conditions are as follows:

- ACOUT0 output
- Comparator 0 reference input
- :D/A converter 0 output, 3 V setting
 - :Filter with f32 sampling

:Output enabled

- :Interrupt by CM0F bit enabled
- :Non-inverted comparator 0 comparison result output to ACOUT0
- Comparator 0 digital filterComparator 0 interrupt
- ACOUT0 output polarity

REJ05B1089-0100/Rev.1.00



Figure 3.1 shows an Operating Example of Comparator i (i = 0 or 1).

If the analog input voltage is higher than the reference input voltage, the CMiLV bit in the ACCRi register is set to 1. If the analog input voltage is lower than the reference input voltage, the CMiLV bit is set to 0.

When the comparison result changes, the CMiF bit in the ACCRi register is set to 1. If the value of the CMiIE bit in the ACCRi register is 1 (interrupt by CMiF bit enabled) at this time, a comparator i interrupt request is generated. Refer to the **R8C/2F Group Hardware Manual** for information on interrupts.

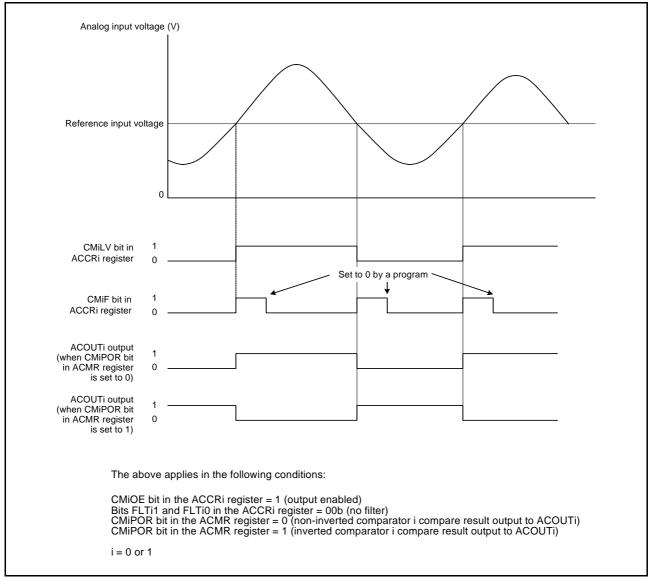


Figure 3.1 Operating Example of Comparator i (i = 0 or 1)

This sample program may include bit operations of unused functions for the SFR bit layout. Set these values according to the operating conditions of the user system.



3.1 Pins Used

Table 3.1Pins Used and Their Function

Pin Name	I/O	Function
P0_4/AN3/TREO/ACMP0	Input	Comparator 0 analog pin
P5_3/TRCIOC/ACOUT0	Output	Comparator 0 comparison result output pin

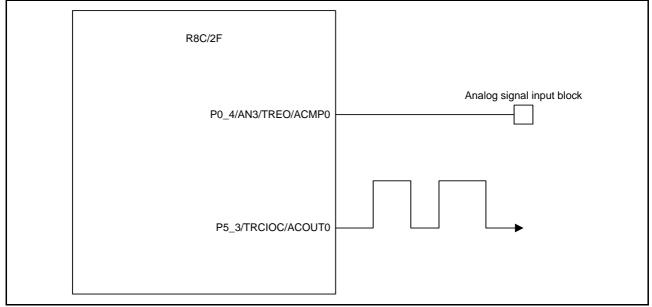


Figure 3.2 Analog Signal Input and Comparison Result Output

3.2 Memory Usage

Table 3.2 Memory Usage

Memory Usage	Size	Remarks
ROM	179 bytes	In main.c module
RAM	0 bytes	In main.c module
Maximum user stack usage	13 bytes	main function: 7 bytes comparator_init function: 6 bytes
Maximum interrupt stack usage	19 bytes	CM0_int function: 19 bytes

Memory usage varies depending on the C compiler version and the compile option. The above applies under the following conditions:

- C compiler: M16C/60, 30, 20, 10, Tiny, R8C/Tiny Series Compiler V.5.40 Release 00
- Compile option: -c -finfo; NOTE: -dir "\$(CONFIGDIR)" -R8C

NOTE: Not available in the R8C/Tiny-exclusive free version.



4. Setup

This section shows the initial setting procedures and values to perform the example described in **3. Application Example Description**. Refer to the **R8C/2F Group Hardware Manual** for details on individual registers.

4.1 System Clock Setting

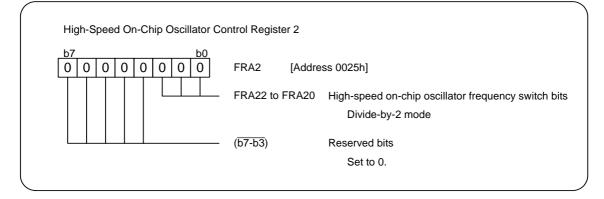
(1) Enable writing to registers CM0, CM1, OCD, FRA0, FRA1, and FRA2.

(
	Protect Register				
	b7	b0	PRCR	[Address 000Ah]	
			PRC0	Protect bit 0	
				Writing to registers CM0, CM1, OCD, FRA0, FRA1, and FRA2 enabled	

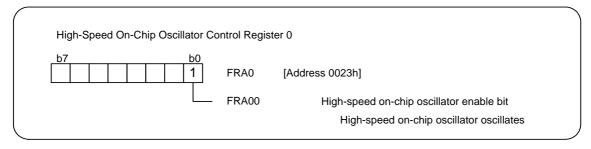
(2) Start the low-speed on-chip oscilltor.

Svstem	Clock Control Register 1			
b7		CM1 - CM14	[Address 0007h] Low-speed on-chip oscillator oscillation stop bit Low-speed on-chip oscillator oscillates	

(3) Set the division ratio of the high-speed on-chip oscillator clock.



(4) Start the high-speed on-chip oscilltor.

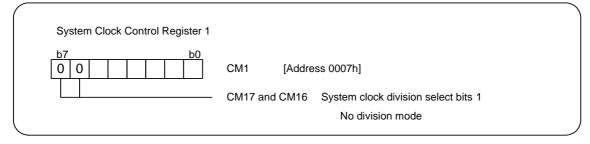




- (5) Wait until oscillation stabilizes.
- (6) Select the high-speed on-chip oscillator.

High-Speed On-Chip	Oscillator Co	ontrol Regis	ter 0
b7	b0	FRA0	[Address 0023h]
		FRA01	High-speed on-chip oscillator select bit High-speed on-chip oscillator selected
			right-speed on-only oscillator selected

(7) Set system clock division select bits 1.



(8) Set system clock division select bit 0.

System Clock Control Register 0			
b7 b0	CM0	[Address 0006h]	
	CM06	System clock division select bit 0	
		CM16 and CM17 enabled	

(9) Disable writing to registers CM0, CM1, OCD, FRA0, FRA1, and FRA2.

Protect Register			
b7	b0	PRCR	[Address 000Ah]
		PRC0	Protect bit 0
			Writing to registers CM0, CM1, OCD, FRA0, FRA1, and FRA2 disabled

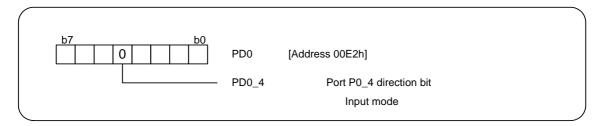


4.2 Comparator Setting

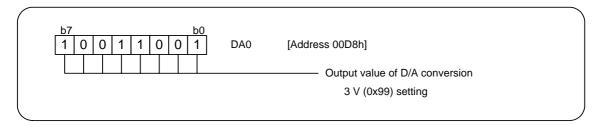
(1) Set the protect register.

(
	b7	b0	PRCR	[Address 000Ah]	
			PRC2	Protect bit 2	
				Writing to PD0 register enabled	

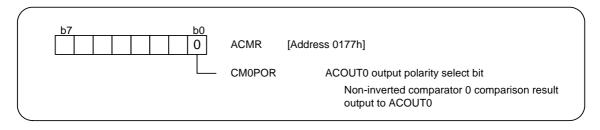
(2) Set the port P0 direction register.



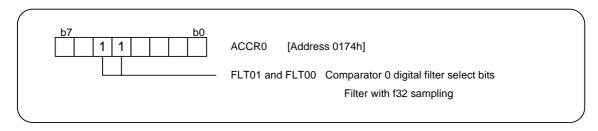
(3) Set the D/A0 register.



(4) Set the ACOUT0 output polarity select bit.



(5) Set the comparator 0 digital filter select bit.

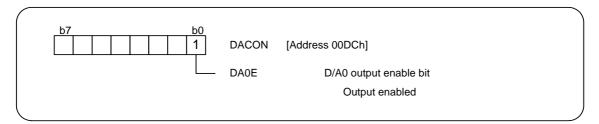




(6) Set the comparator 0 reference input select bit.



(7) Set the D/A0 output to enable.



(8) Set the comparator 0 operation enable bit.



(9) Wait until the comparator stabilizes (10 µs maximum)

(10) Read the comparator 0 interrupt flag (CM0F_ACCR0) (dummy read to initialize the interrupt flag)

(11) Set the ACOUT0 output enable bit.



(12) Set the comparator 0 interrupt enable bit.

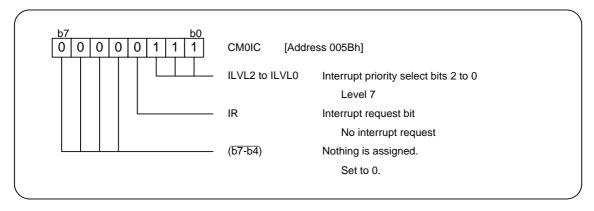




(13) Initialize the comparator 0 interrupt flag.



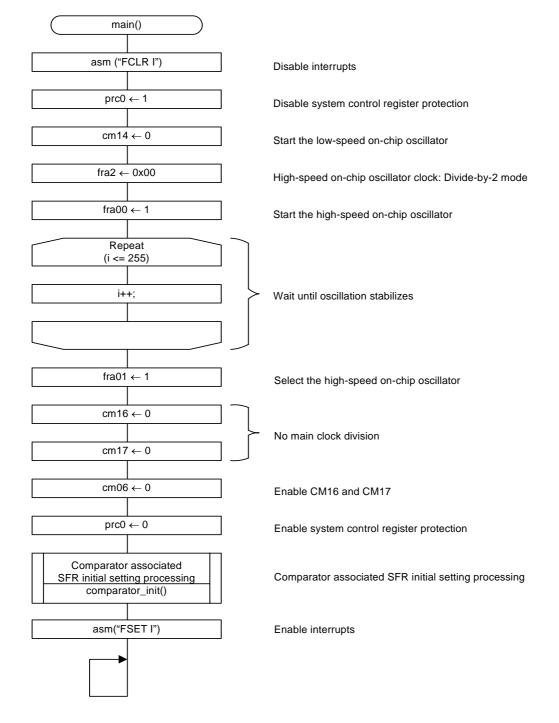
(14) Set the comparator 0 interrupt control register.





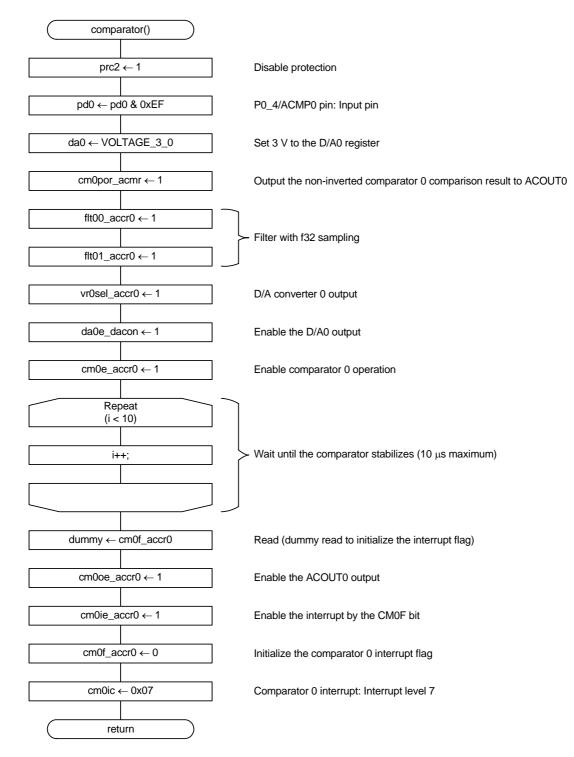
5. Flowchart

5.1 Main Function



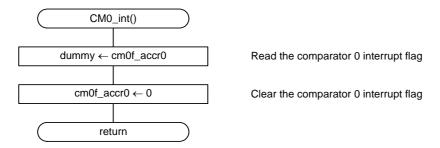


5.2 Comparator Associated SFR Initial Setting Processing





5.3 Comparator 0 Interrupt Handling





6. Sample Programming Code

A sample program can be downloaded from the Renesas Technology website. To download, click "Application Notes" in the left-hand side menu of the R8C/Tiny Series page.

7. Reference Documents

Hardware Manual R8C/2F Group Hardware Manual The latest version can be downloaded from the Renesas Technology website.

Technical Update/Technical News The latest information can be downloaded from the Renesas Technology website.



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REVISION HISTORY	
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R8C/2F Group Comparator

Rev.	Date	Description					
itev.	Dale	Page	ge Summary				
1.00	Oct 31, 2007	-	First Edition issued				



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