Application Note

Tracking ADC

AN-CM-309

Abstract

This application note describes the implementation of a simple tracking ADC based on digital rheostats of the SLG47004. No external components and no special tuning procedure are required for the proposed ADC structure. Also, the circuit has much better PSRR and temperature drift than a capacitor based counter type ADC.
The proposed ADC can be used for monitoring slow-changing signals like temperature, battery voltage, and others.

This application note comes complete with design files which can be found in the References section.

Contents

Figures

Tables

1 Terms and Definitions

ACMP	Analog comparator
ADC	Analog to digital converter
DAC	Digital to analog converter
IC	Integrated circuit
OpAmp	Operational amplifier

2 References

For related documents and software, please visit:

GreenPAK™ Programmable Mixed-Signal Products | Renesas

Download our free GreenPAK Designer software [1] to open the .gp files [2] and view the proposed circuit design. Use the GreenPAK development tools [3] to freeze the design into your own customized IC in a matter of minutes. Find out more in a complete library of application notes [4] featuring design examples as well as explanations of features and blocks within the GreenPAK IC.

[1] GreenPAK Designer Software, Software Download and User Guide

[2] AN-CM-309 Tracking ADC.gp, GreenPAK Design File

[3] GreenPAK Development Tools, GreenPAK Development Tools Webpage

[4] GreenPAK Application Notes, GreenPAK Application Notes Webpage

[5] SLG47004, Datasheet

Author: Vladyslav Kozlov

3 Introduction

The growing development of digital ICs like microcontrollers, microprocessors, FPGA, and others, allows using complex digital processing techniques instead of analog signal conditioning. This tendency made ADC a widely used component of mixed-signal circuits.

There are a lot of types of ADC: successive-approximation ADC, sigma-delta ADC, direct-conversion ADC, capacitor charge/discharge based ADC, ADC with voltage-to-frequency converters, and others. All these ADC types have different accuracy, frequency, and cost characteristics. The proposed structure of ADC is the tracking ADC.

4 Tracking ADC Principle

The main components of the tracking ADC are:

- DAC. Current project uses buffered voltage reference output and digital potentiometer as DAC.
- ACMP.
- Counter with Up/Down control input. In the SLG47004 this counter is embedded into the digital rheostats macrocells.

The operation principle of the tracking ADC is shown in Figure 1. When conversion starts, the counter begins to change the resistance of digital potentiometer depending on the level at Up/Down input. At each (Oscillator) step the voltage at the inverting input of ACMP increases (or decreases). The conversion ends when ACMP changes its output. After the end of the conversion it's possible to calculate sampled input voltage:

$$Vin = \frac{Vref}{Ntaps} \cdot N,$$

where Vin – input voltage at inverting input of ACMP; $Vref$ – reference voltage; $Ntaps$ – maximum number of potentiometer taps; N – the value of counter after the end of conversion.

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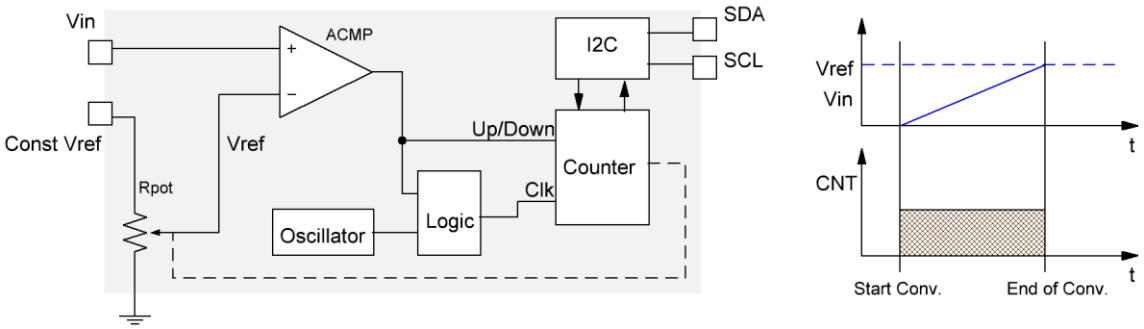

Figure 1: Basic Structure and Operation Principle of the Tracking ADC

Figure 2 shows the internal design of the tracking ADC based on the SLG47004.

Pulse at "Start Conversion" input begins conversion process. There are two options for initial rheostats value:

- If "Auto-Reload" input is floating, every new conversion starts from the rheostats default value of 512. This default value corresponds to Vref/2 voltage at dividers output.
- If "Auto-Reload" input is connected to ground, every new conversion starts from the previous rheostat value. This option can speed up the conversion time for slow-changing processes.

The stop condition occurs when ACMP changes its input from Low to High the 3rd time.

The User can hold a logic level High at “Start Conversion” input to track input voltage level. In this case the rheostat will keep on switching and changing Vref voltage near Vin voltage level. Note that “In Progress/Done” output will change its level to logic Low after ACMP changes its input from Low to High the 3rd time, even if logic level High is being kept at the “Start Conversion” input.

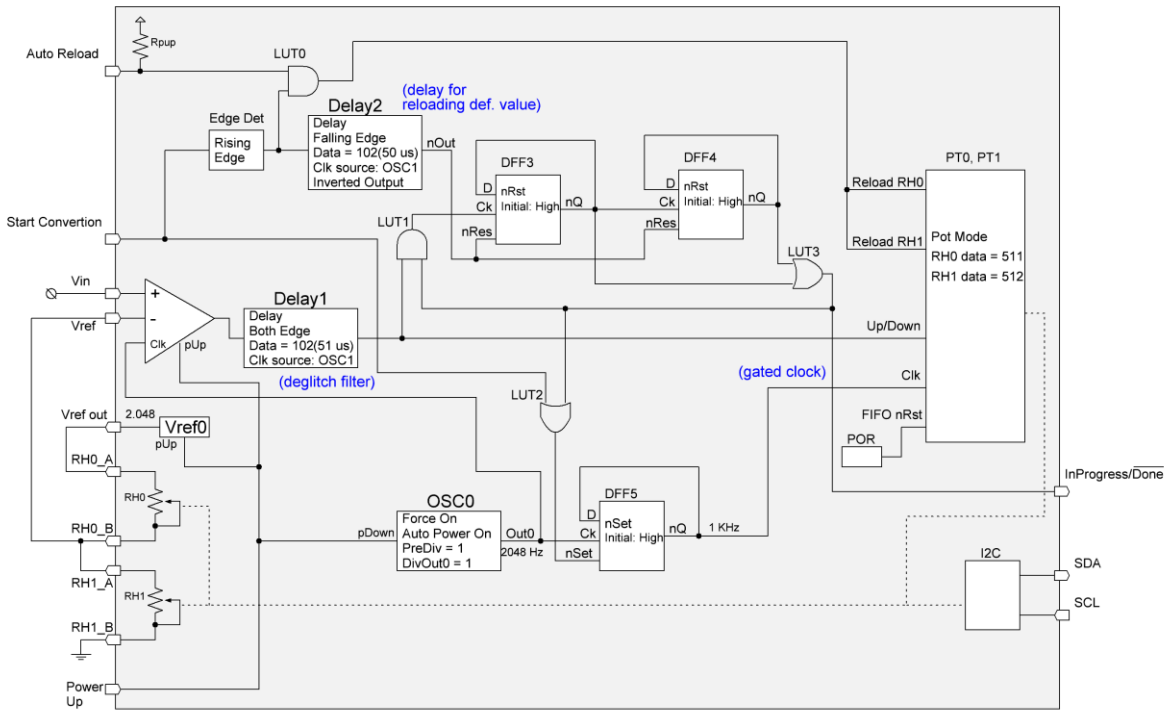

Figure 2: Internal Design of the Tracking ADC Based on SLG47004

5 Internal Blocks Configuration

Figure 3 shows the design of the project in GreenPAK Designer Software.

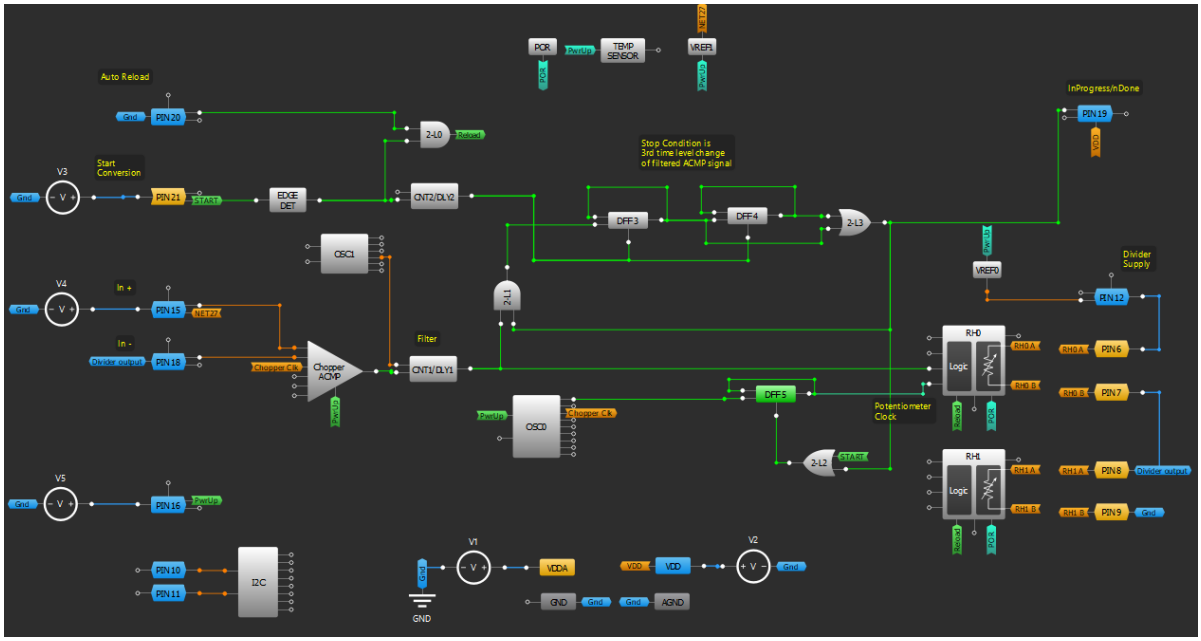

Figure 3: Project Design in GreenPAK Designer Software

5.1 Chopper ACMP Configuration

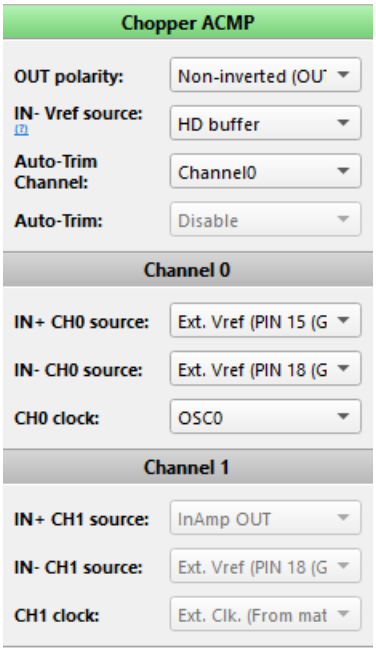

Figure 4: Chopper ACMP Configuration

5.2 Oscillators Configurations

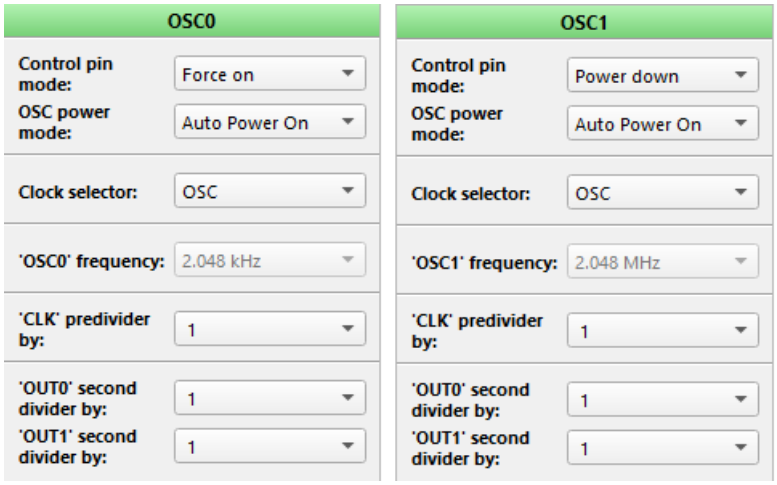

Figure 5: Oscillators Configurations

5.3 Digital Rheostats Configurations

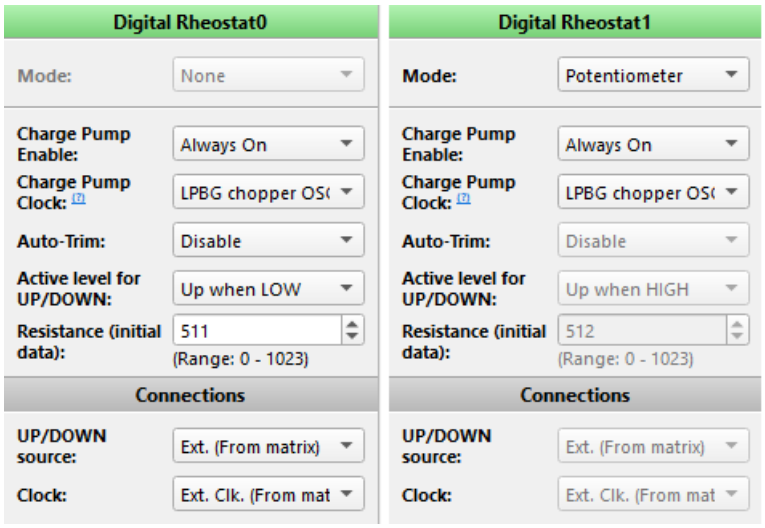

Figure 6: Digital Rheostats Configurations

5.4 LUTs Configurations

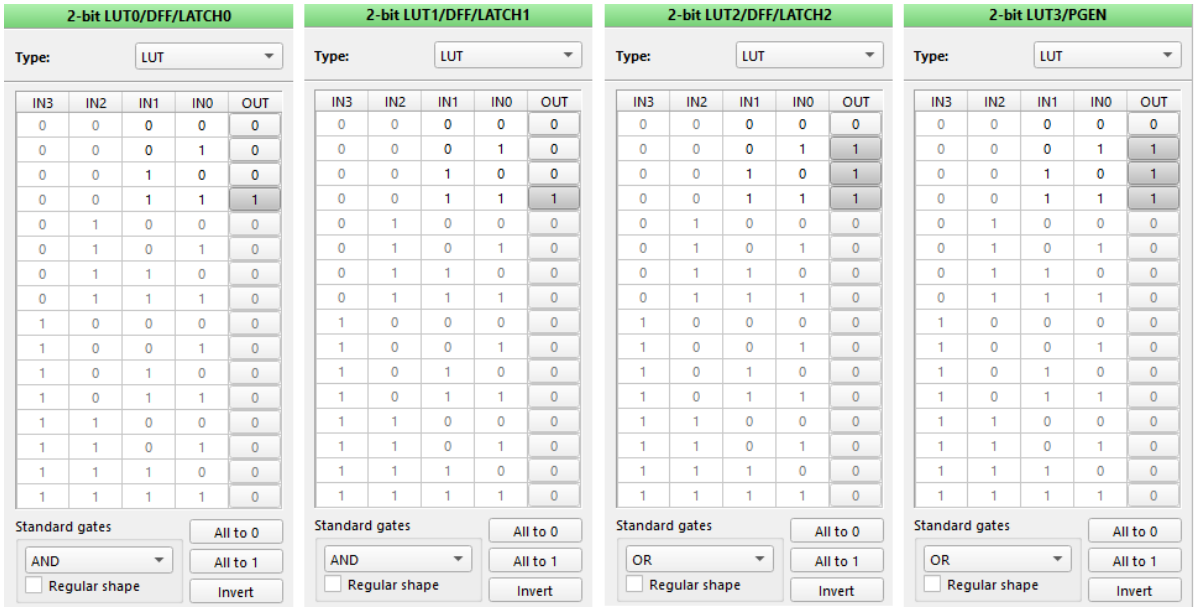

Figure 7: LUTs Configurations

5.5 DFFs Configurations

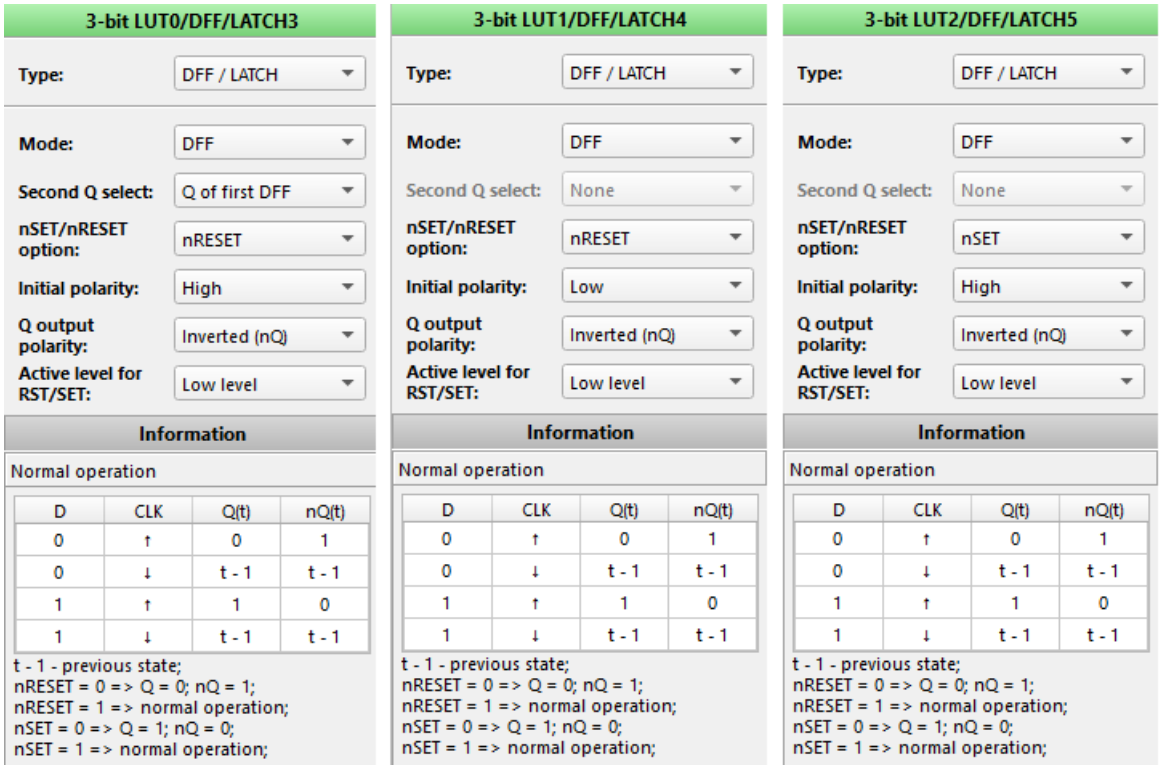

Figure 8: DFFs Configurations

5.6 Filter/Edge Detector Configuration

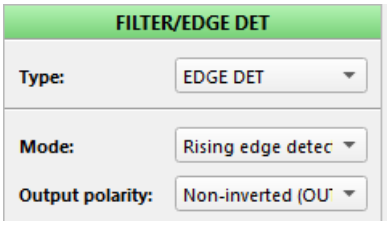

Figure 9: Filter/Edge Detector Configuration

5.7 Vref0 Configuration

To configure the Vref0 macrocell, the ACMP0L should also be configured.

Figure 10: ACMP0L and Vref0 Configurations

5.8 IO Pins Configurations

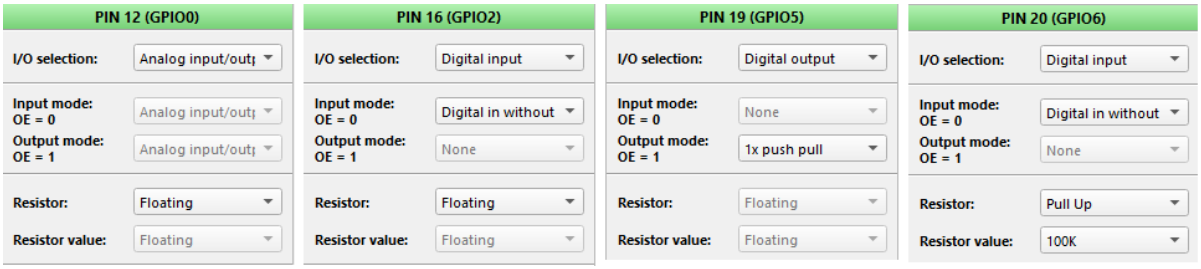

Figure 11: IO Pins Configurations

5.9 I²C Macrocell Configuration

I²C Macrocell uses default settings.

6 Design Verification Using Software Simulation and Hardware Prototype

Figure 12 shows the results of software simulation of the tracking ADC with disabled auto-reload feature. It can be seen that after a start pulse, the clock signals come to the digital potentiometer. At each clock the potentiometer changes the wiper position (the 3rd common terminal) and the reference voltage approaches the input voltage. When the reference voltage at wiper terminal becomes equal to the input voltage, the ACMP changes its level. After the 3rd rising edge of the ACMP signal the process ends. The same process is demonstrated in Figure 13.

If auto-reload feature is disabled, the process begins from the current potentiometer state. But if auto-reload feature is enabled, the digital potentiometer starts counting from the default value defined by the User. The operation of the tracking ADC with enabled auto-reload feature is shown in Figure 14.

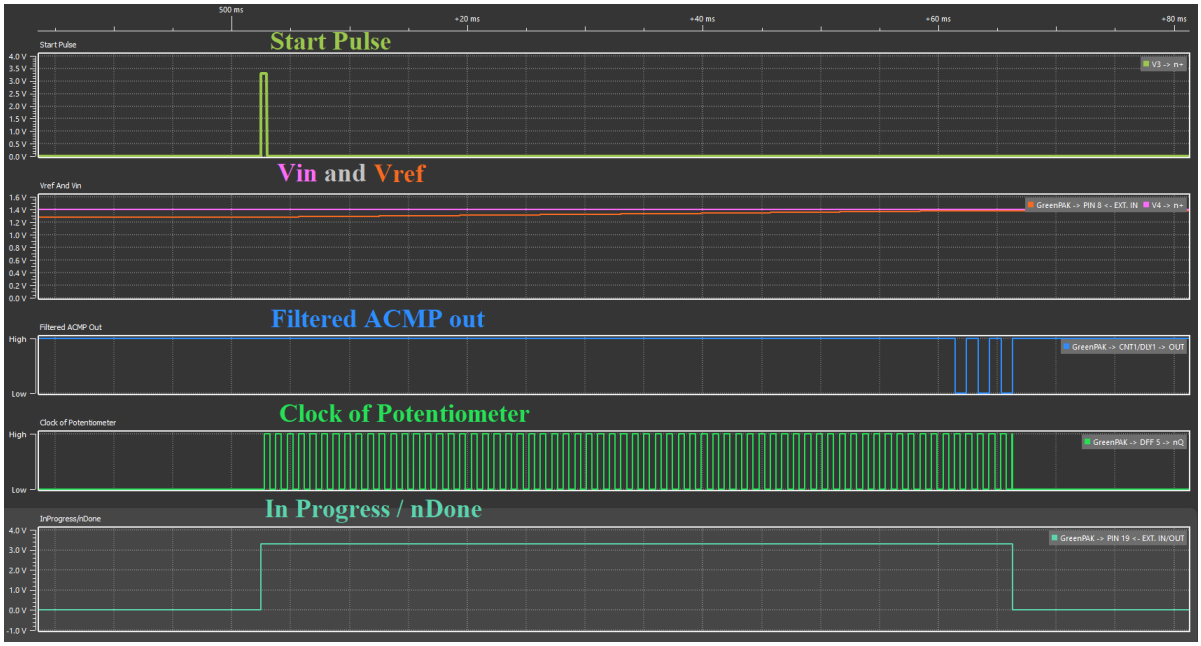

Figure 12: Software Simulation of ADC Operation with Disabled Auto-Reload Feature

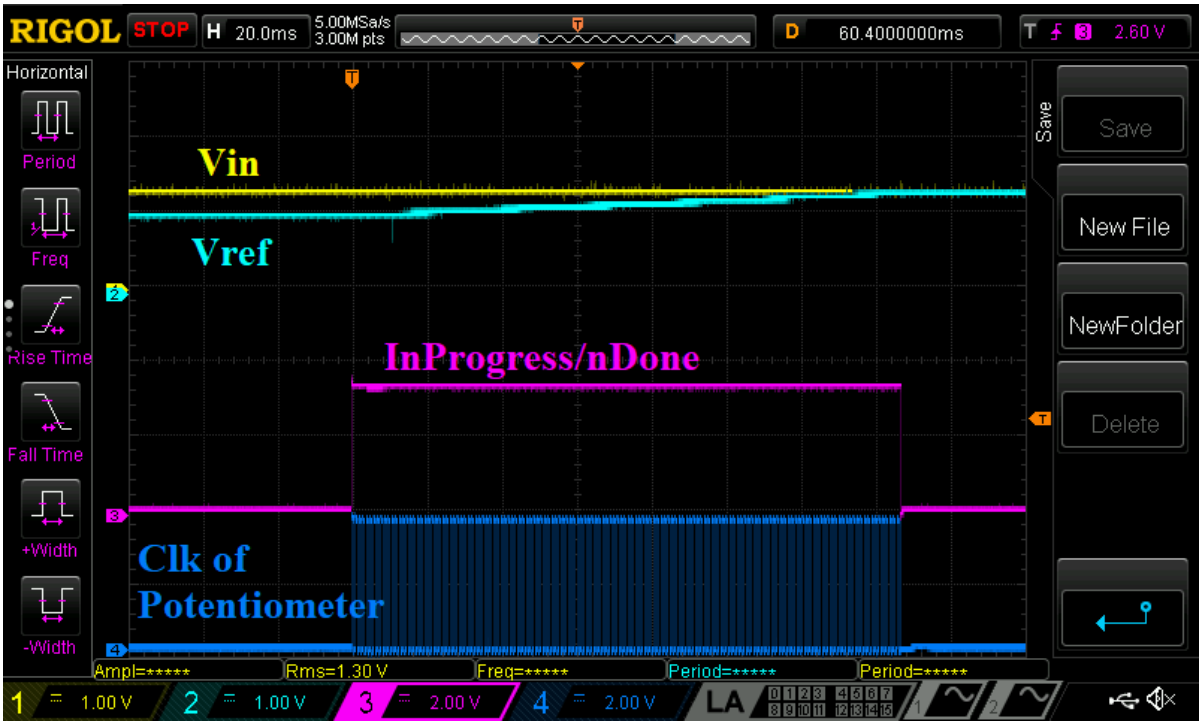

Figure 13: Waveforms of ADC Operation with Disabled Auto-Reload Feature

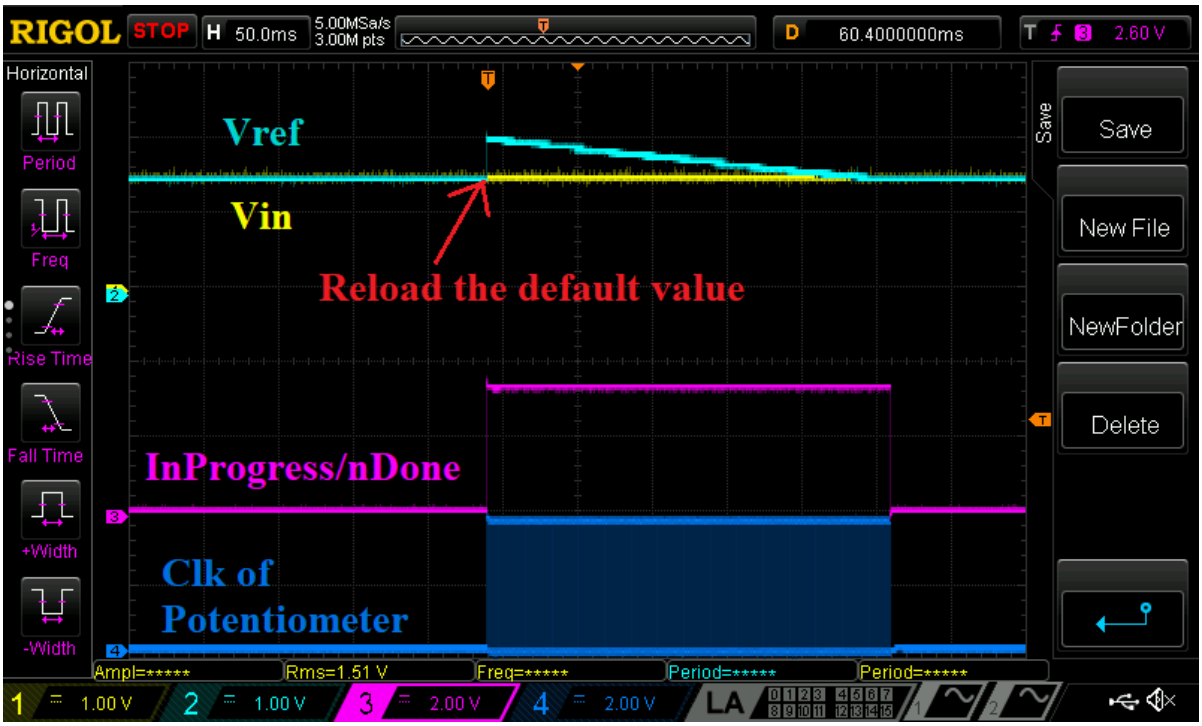

Figure 14: Waveforms of ADC Operation with Enabled Auto-Reload Feature

7 Accuracy and Timing Characteristics

The most essential error sources of ADC are non-linearity (DNL and INL), gain error, and offset error. The output voltage considering errors caused by the rheostats DNL and INL can be estimated using formula (1). The digital rheostats of the SLG47004 have DNL and INL = ±1 LSB (max).

$$Vout = \frac{Vref}{R_{RH} \pm \frac{1LSB_{INL}}{1024} R \pm \frac{2LSB_{DNL}}{1024} R} \cdot \frac{R_{RH}}{1024} \cdot \left(N \pm 1LSB_{DNL} \pm \frac{1LSB_{INL}}{1024 - N} \right), \quad (1)$$

where $Vout$ – output voltage; $Vref$ – reference voltage of divider; R_{RH} – maximum rheostat resistance; N – number of bits that corresponds to sampled voltage.

According to formula (1), the maximum error caused by the rheostats DNL and INL is ~2LSB. The next DC error source is the input offset voltage of the comparator. In the case of 2.048 V voltage reference of divider:

$$V_{offsetLSB} = V_{offsetACMP} \frac{1024}{2.048},$$

where $V_{offsetLSB}$ and $V_{offsetACMP}$ – comparator offset in LSB and in volts.

In the case of Chopper ACMP $V_{offsetLSB}$ = 0.15 LSB (0.3 mV maximal offset).

The absolute value of Vref is another additional error source. The Vref with accuracy of ±1 % causes a gain error of 10 LSB. Eventually, full-scale error is **12.15 LSB max**.

Note that both gain and offset errors can be easily compensated by software, unlike DNL and INL errors.

Temperature drift of the system depends mainly on the temperature drift of internal Vref. It is equal to 40 µV/°C. It should be noted that the temperature change doesn't affect the potentiometer ratio.

Maximum time of the conversion depends on the maximum allowed switching frequency of rheostats. The switching frequency of the rheostats is 1 kHz max in regular mode. Maximum time of the conversion: $T_{Conv} = \frac{1}{f_{max}} (512 + 5)$ =0.517s or ~2Hz

8 Conclusions

This application note describes the design of a simple tracking ADC based on the unique analog blocks within the SLG47004. Another popular type of ADC for the devices that don't have dedicated embedded ADC is the capacitor based or the Wilkinson ADC. The main principle of that ADC is the measurement of the time of an external capacitor charging (discharging). The comparison of these two ADC types can be found in Table 1.

Table 1: The Comparison of Tracking ADC and Capacitor Based (Wilkinson) ADC

Parameter	Tracking ADC	Capacitor Based ADC
External components	-	One capacitor
The full-scale error without calibration, % of full range	1.2 % (max)	>10 % for mainstream capacitors >1 % for best in class ceramic capacitors
Temperature drift, ppm	20 ppm/°C	From 30 ppm/°C to 2500 ppm/°C for ceramic capacitors
Sample time, ms	517 (max)	>7 (limited by the ACMP propagation error)

The data from Table 1 shows that the tracking ADC has much better accuracy performance while the Wilkinson is much faster.

Revision History

Revision	Date	Description
1.0	03-Nov-2020	Initial Version

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