Application Note

Analog Front End for a Pressure Sensor

AN-CM-308

Abstract

The application note describes the design procedure for Wheatstone bridge sensors. A unique Auto-Trim feature of the SLG47004 is used to achieve the best precision of this analog interface. The application note contains a complete schematic of an analog front-end for a low-cost pressure sensor.

This application note comes complete with design files which can be found in the References section.

Contents

Figures

Tables

1 Terms and Definitions

AFE	Analog front end
IC	Integrated circuit
OpAmp	Operational amplifier
RH	Digital rheostat

2 References

For related documents and software, please visit:

AnalogPAK™ | Renesas

Download our free GreenPAK Designer software [1] to open the .gp files [2] and view the proposed circuit design. Use the GreenPAK development tools [3] to freeze the design into your own customized IC in a matter of minutes. Find out more in complete library of application notes [4] featuring design examples as well as explanations of features and blocks within the GreenPAK IC.

[1] GreenPAK Designer Software, Software Download and User Guide

[2] AN-CM-308 Analog Front End for Pressure Sensor.gp, GreenPAK Design File

[3] GreenPAK Development Tools, GreenPAK Development Tools Webpage

[4] GreenPAK Application Notes, GreenPAK Application Notes Webpage

[5] SLG47004, Datasheet

Author: Vladyslav Kozlov

3 Introduction

In the following application note the SLG47004 is used as the analog front-end (AFE) for a Wheatstone bridge pressure sensor. Two configurable OpAmps and one internal OpAmp, all within the SLG47004 are used to create an instrumentation amplifier. Digital rheostats RH0 and RH1 of the SLG47004 are used to tune the gain of the AFE and to compensate offset voltages of sensor and OpAmps. Also, the trim procedure helps to minimize an error caused by mismatch between external resistors. The Auto-Trim function of the SLG47004 simplifies the process of gain tuning and offset compensation and allows saving hardware resources, as well as minimize the cost of the AFE.

The SLG47004 allows two different ways of interfacing ADCs with and without internal reference sources:

- In the case when an external ADC has a separate analog reference pin, the common way is to supply all analog blocks (sensor, ADC, DAC for compensating offset) from one voltage source. The measurements are ratiometric. Variations in supply voltage don't affect accuracy.
- In the case when an ADC has an internal reference source only, the supply voltage for the sensor and DAC must be stable and constant. That's why, for this case, an internal buffered Vref of the SLG47004 must be used.

4 AFE Without Internal Voltage Reference Source

4.1 Hardware Setup of AFE Without Internal Voltage Reference

Figure 1 shows a schematic of the analog front end for MCU with ADC, which has an external analog reference option. Sensor, ADC reference, DAC (R_{div1}, RH0, R_{div2} divider for offset compensation), and Chopper ACMP reference are powered from one voltage source: Van. Characteristics of the components can be found in Table 1. A pressure sensor from Honeywell (NSCSDRN060MD) is used in this example.

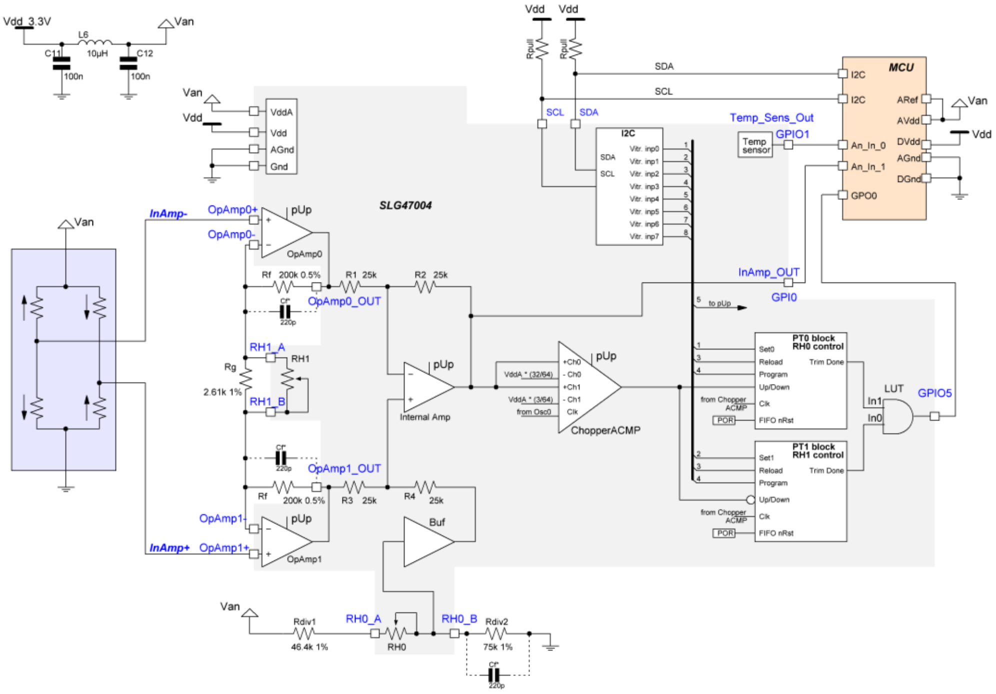


Figure 1: Analog Front-End for a Wheatstone Bridge Sensor

In Figure 1 V_{an} is the supply voltage for analog components. V_{an} is filtered V_{DD} voltage. The output of the sensor with no pressure is equal to ($V_{an}/2 \pm V_{os\_bridge}$), where V_{os_bridge} is the bridge offset voltage. Since the force to the sensor can be applied in both directions, the output of the sensor can be higher or lower than zero point ($V_{an}/2 \pm V_{os\_bridge}$). So the AFE must amplify the output signal differentially between the sensor zero point and its actual output.

The optional C_f capacitance is needed to cancel the switching noise of digital rheostats. The value of C_f can be changed.

The output voltage of AFE is:

$$V_{Out} = \left(V_{InAmp+} - V_{InAmp-}\right) \cdot Gain + Vref, \text{ (1)}$$

where

$$Gain = 1 + \frac{2Rf}{Rg \,||\, RH1}$$

Rf – are user-defined resistors, Rf = 200 KΩ and 0.5% tolerance in the current project;

Rg – is user-defined gain resistor;

$Vref$ – is the reference voltage for the instrumentation amplifier.

4.2 Precision Characteristics of Components

Precision characteristics of the components are shown in Table 1.

Table 1: Precisive Characteristics of Components

Parameter	Description	Value	Unit
Sensor Characteristics			
ΔP	Pressure Range	±6.0	kPa
KV_{out}	Full Scale Span Coefficient	±2.46 (min), ±2.60 (typ), ±2.8 (max)	mV/V
K_{os_out}	Null Offset Coefficient	±0.075	mV/V
Sensor Characteristics at 3.3 V DC			
ΔV_{out}	Output Voltage Span	±8.1 (min), ±8.58 (typ), ±9.2 (max)	mV
V_{os_bridge}	Null Offset	±0.248 (max)	mV
dV_{os_bridge}/dT	Offset Temperature Drift (T = 0 to 50 °C)	±0.6 (max)	%FSS
OpAmps Characteristics			
$V_{os_{OpAmp}}$	Input Offset Voltage	1.0 (max)	mV
$dV_{os_{OpAmp}}/dT$	Offset Drift with Temperature	5 (max)	µV/°C
ΔR_{int}	Mismatch Between Internal R1, R2, R3, R4 Resistors	0.05	%
Digital Rheostats Characteristics			
$RH1, RH2$	Digital Rheostats Resistance	80 (min), 100 (typ), 120 (max)	kOhm
N_{taps}	Number of Taps	1024	
f_{ChACMP}	Chopper Comparator Switching Frequency	10	kHz

Parameter	Description	Value	Unit
V_{Ch_offset}	Chopper Comparator Offset when Set is Active	300 (max)	µV
DNL	Differential Non-Linearity (max)	1	LSB
αR(T)	Nominal Resistance Temp Coefficient	100	ppm/°C
HD Buffer Characteristics			
$V_{os\_HD\_Buf}$	HD Buffer Offset	±3 (max), T = 25 °C	mV
$\Delta V_{OUT}(I)$	HD Buffer Load Regulation at I_{Load} = 2mA	2	mV
External Resistors Characteristics			
ΔR_{ext}	Resistors Tolerance	0.5 and 1	%
$\alpha R_{ext}(T)$	Resistance Temp Coefficient	50	ppm/°C

4.3 Internal GreenPAK Design and Macrocells Configurations

4.3.1 Internal Design of the Project

Figure 2 shows the internal design of the project in GreenPAK Designer Software.

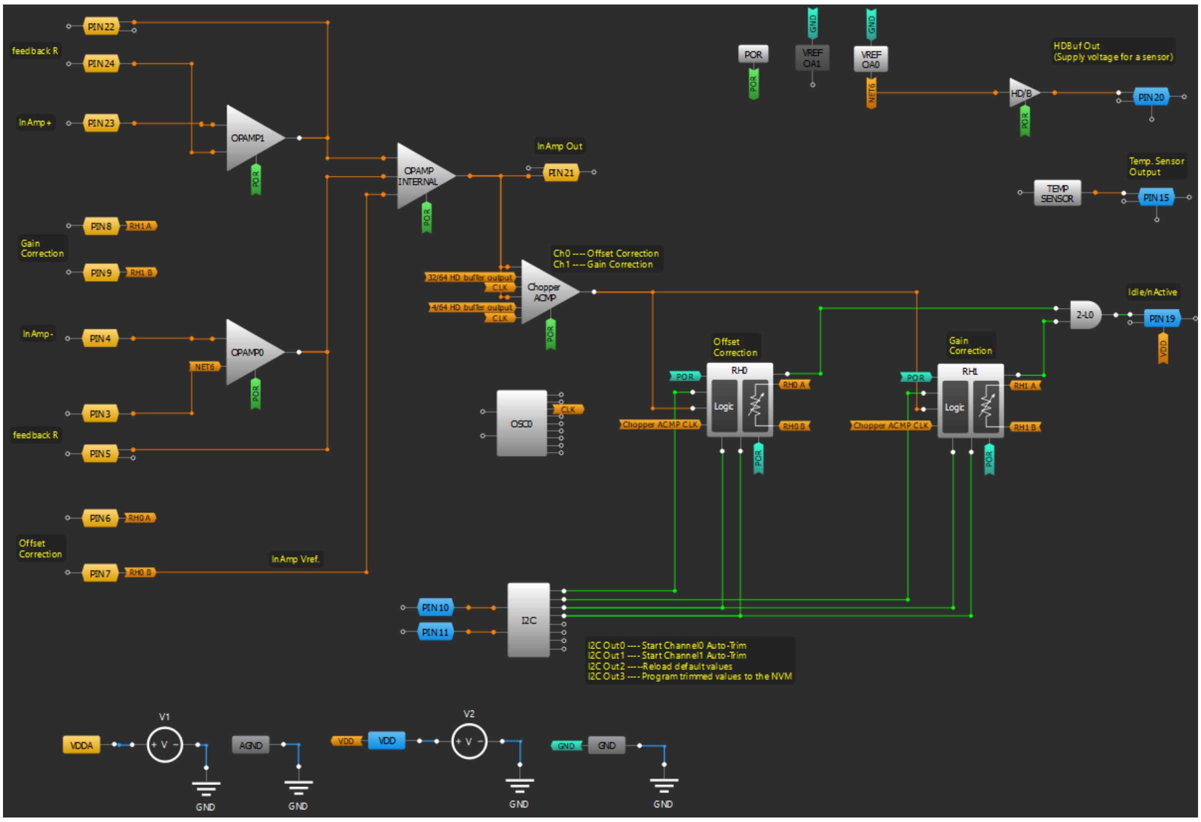
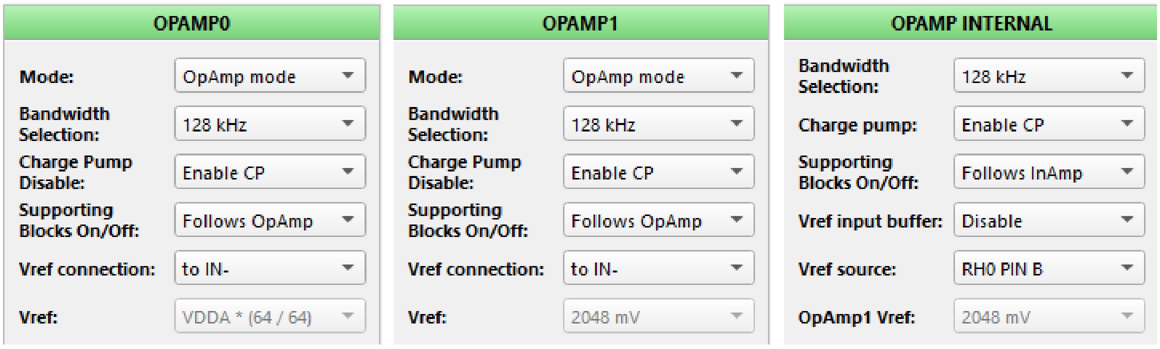


Figure 2: Internal Design of the Project

4.3.2 OpAmps Configurations

OpAmps configurations are shown in Figure 3.



OPAMP0

Mode: OpAmp mode
Bandwidth Selection: 128 kHz
Charge Pump Disable: Enable CP
Supporting Blocks On/Off: Follows OpAmp
Vref connection: to IN-
Vref: VDDA * (64 / 64)

OPAMP1

Mode: OpAmp mode
Bandwidth Selection: 128 kHz
Charge Pump Disable: Enable CP
Supporting Blocks On/Off: Follows OpAmp
Vref connection: to IN-
Vref: 2048 mV

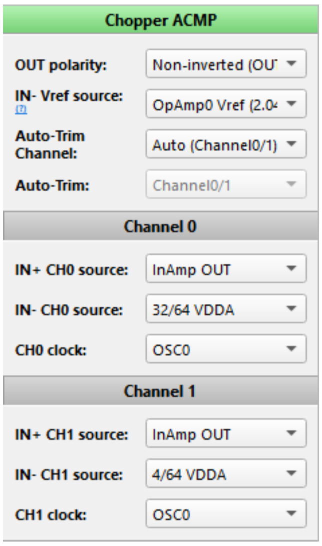
OPAMP INTERNAL

Bandwidth Selection: 128 kHz
Charge pump: Enable CP
Supporting Blocks On/Off: Follows InAmp
Vref input buffer: Disable
Vref source: RH0 PIN B
OpAmp1 Vref: 2048 mV

Figure 3: OpAmps Configurations

4.3.3 Chopper ACMP Configuration

Channel0 of Chopper ACMP is used for offset correction. Channel1 of Chopper ACMP is used for tuning gain of AFE. Chopper ACMP configuration is shown in Figure 4.



Chopper ACMP

OUT polarity: Non-inverted (OU
IN- Vref source: OpAmp0 Vref (2.0
Auto-Trim Channel: Auto (Channel0/1)
Auto-Trim: Channel0/1

Channel 0

IN+ CH0 source: InAmp OUT
IN- CH0 source: 32/64 VDDA
CH0 clock: OSC0

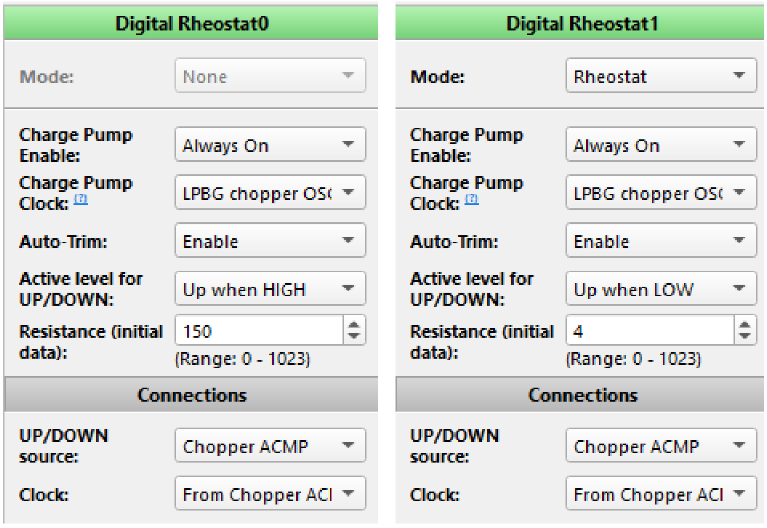
Channel 1

IN+ CH1 source: InAmp OUT
IN- CH1 source: 4/64 VDDA
CH1 clock: OSC0

Figure 4: Chopper ACMP Configuration

4.3.4 Digital Rheostats Configurations

Digital Rheostats configurations are shown in Figure 5.



Digital Rheostat0

Mode: None

Charge Pump Enable: Always On

Charge Pump Clock: LPBG chopper OS(

Auto-Trim: Enable

Active level for UP/DOWN: Up when HIGH

Resistance (initial data): 150 (Range: 0 - 1023)

Connections

UP/DOWN source: Chopper ACMP

Clock: From Chopper ACI

Digital Rheostat1

Mode: Rheostat

Charge Pump Enable: Always On

Charge Pump Clock: LPBG chopper OS(

Auto-Trim: Enable

Active level for UP/DOWN: Up when LOW

Resistance (initial data): 4 (Range: 0 - 1023)

Connections

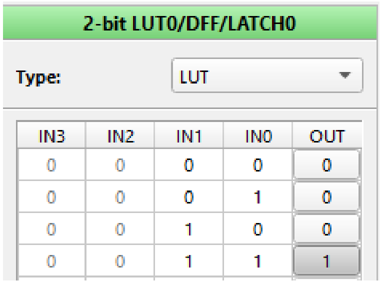
UP/DOWN source: Chopper ACMP

Clock: From Chopper ACI

Figure 5: Digital Rheostats Configurations

4.3.5 LUT Configuration

LUT configuration is shown in Figure 6.



2-bit LUT0/DFF/LATCH0

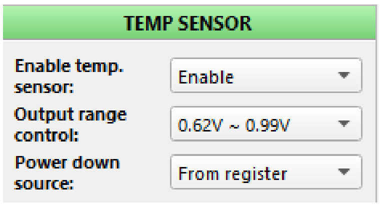
Type: LUT

IN3	IN2	IN1	IN0	OUT
0	0	0	0	0
0	0	0	1	0
0	0	1	0	0
0	0	1	1	1

Figure 6: LUT Configuration

4.3.6 Temperature Sensor Configuration

The temperature sensor configuration is shown in Figure 7.



TEMP SENSOR

Enable temp. sensor: Enable

Output range control: 0.62V ~ 0.99V

Power down source: From register

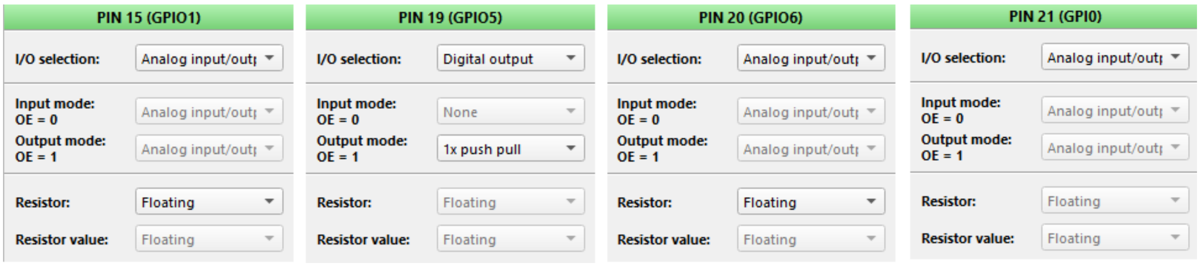
Figure 7: Temperature Sensor Configuration

4.3.7 Oscillator0 and I^{2}C Macrocells Configurations

Oscillator0 and I^{2}C Macrocells use default configurations.

4.3.8 GPIOs Configurations

GPIOs configurations are shown in Figure 8.



PIN 15 (GPIO1)
I/O selection: Analog input/out
Input mode: OE = 0: Analog input/out
Output mode: OE = 1: Analog input/out
Resistor: Floating
Resistor value: Floating

PIN 19 (GPIO5)
I/O selection: Digital output
Input mode: OE = 0: None
Output mode: OE = 1: 1x push pull
Resistor: Floating
Resistor value: Floating

PIN 20 (GPIO6)
I/O selection: Analog input/out
Input mode: OE = 0: Analog input/out
Output mode: OE = 1: Analog input/out
Resistor: Floating
Resistor value: Floating

PIN 21 (GPIO0)
I/O selection: Analog input/out
Input mode: OE = 0: Analog input/out
Output mode: OE = 1: Analog input/out
Resistor: Floating
Resistor value: Floating

Figure 8: GPIOs Configurations

4.4 Gain Resistor Calculation

To calculate the value of the gain resistor R_g the minimum and maximum gain of the instrumentation amplifier must be assessed. Considering the possible output span of the sensor $V_{an} \cdot KV_{out}$ (from 8.12 mV to 9.24 mV for $V_{an} = 3.3$ V), the gain of AFE can be found from the equation:

$$(Van \cdot KVout) \cdot Gain = \frac{Van}{2} - Gain\_ref\_ChopACMP, \quad (2)$$

where $Gain\_ref\_ChopACMP$ – is the reference voltage of ChopperACMP for gain tuning (see Channel1 In- reference source of Chopper ACMP, Section 4.3.3). $Gain\_ref\_ChopACMP$ = V_{DDA}*(3/64) or 0.155 V for $V_{an} = 3.3$ V.

For the schematic shown in Figure 1 $V_{DDA} = V_{an}$. So, the equation (2) can be rewritten as

$$(Van \cdot KVout) \cdot Gain = \frac{Van}{2} - \left(Van \cdot \frac{3}{64}\right)$$

or

$$Gain = \left(\frac{1}{2} - \frac{3}{64}\right) \cdot \frac{1}{KVout} \quad (3)$$

From equation (3) it's seen that variations in V_{an} voltage don't affect the gain of system:

$$Gain_{max} = \left(\frac{1}{2} - \frac{3}{64}\right) \cdot \frac{1}{2.46} \cdot 1000 = 184.2,$$

$$Gain_{min} = \left(\frac{1}{2} - \frac{3}{64}\right) \cdot \frac{1}{2.80} \cdot 1000 = 161.8.$$

Now it's possible to build the graph for the function Gain = f(n), where n – is the code of the rheostat from 1 to 1024:

$$Gain(n) = 1 + \frac{2Rf}{Rg \cdot \left(\frac{80 \cdot 10^3 \cdot n}{1024}\right) \cdot \frac{1}{Rg + \left(\frac{80 \cdot 10^3 \cdot n}{1024}\right)}} \quad (4)$$

Note that the chip to chip variation of RH maximum resistance is from 80 kΩ to 120 kΩ. The 80 kΩ value should be used for gain resistor calculation.

By varying the value of R_g it's possible to match the span of AFE gain from Gain_min to Gain_max, see Figure 9. If there is no R_g value to match the desired range, then R_f value should be increased. For the current schematic R_f = 200 kΩ and R_g = 2.61 kΩ.

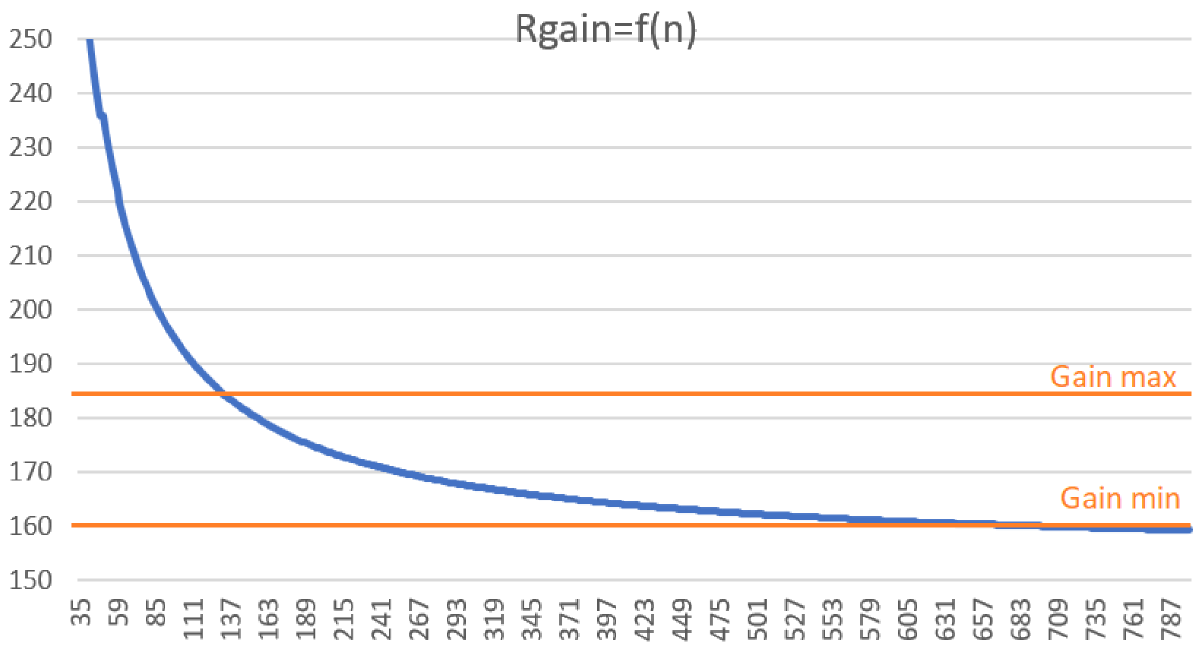


Figure 9: Gain of AFE as a Function of Digital Rheostat's Code, R_{gain} = f(n)

4.5 Vref Divider Resistors Calculation

To calculate the values of DAC resistors (Rdiv1, RH0, Rdiv2 divider) the maximum range of Vref (V_{comp} value) should be calculated. Considering the biggest possible gain of the AFE (Gain_max = 184.2) and the biggest possible input offset (see Figure 10):

$$V_{os\_input} = V_{os_{OpAmp0}} + V_{os_{OpAmp1}} + V_{os_{bridge}} \text{ ,}$$

$$V_{os\_input} = 1\ mV + 1\ mV + 0.248\ mV = 2.25\ mV$$

the Vref can be changed by the value of V_{comp}:

$$V_{comp} = \pm\left(Gain_{Max} \cdot V_{os\_input}\right),$$

$$V_{comp} = \pm(184.2 \cdot 00225) = 0.414\ V$$

To find the value of Rdiv1, Rdiv2, the next equation system should be solved:

$$\begin{cases} \dfrac{Van}{R_{div1} + RH0_{max} + R_{div2}}(R_{div2}) = \dfrac{Van}{2} - Vcomp \\ \dfrac{Van}{R_{div1} + R_{div2}} R_{div2} = \dfrac{Van}{2} + Vcomp \end{cases}$$

where $RH0_{max}$ – maximum resistance of the rheostat, in the worst case $RH0_{max}$ = 80 kΩ;

Van – is the voltage applied to the divider.

For the current schematic the nearest standard values of resistors are R_{div2} = 75 kΩ, R_{div1} = 46.4 kΩ.

4.6 Offset Error Sources and Offset Compensation

To set zero point for the AFE (zero pressure) the voltage from divider (Rdiv1, RH0, Rdiv2) is used. The output from the divider must be connected to the instrumentation amplifier through the buffer to eliminate the impact of DAC output resistance.

By changing the value of RH0 not only sensor offset, but OpAmps input offset voltages can be compensated. See the equation below.
Let’s add offset voltages to the equation (1):

$$V_{Out} = \left(V_{IN+} + V_{os_{OpAmp0}} - V_{IN-} + V_{os_{OpAmp1}} + V_{os_{bridge}}\right) \cdot Gain +$$

$$+V_{os\_IntOpAmp} + V_{os\_Input\_Buffer} + Vcm\_error + \left(Vref - V_{comp}\right)$$

where $V_{os_{OpAmp0}}$, $V_{os_{OpAmp1}}$, $V_{os\_IntOpAmp}$ – are input offset voltages of the SLG47004 amplifiers;

$V_{os\_Input\_Buffer}$ – is buffer input offset voltage;

$V_{os_{bridge}}$ – is offset voltage of the sensor;

Vcm_error – is common-mode voltage error caused by inequality of internal R1, R2, R3, R4 resistors, and external R_f resistors. This voltage will be compensated after the trim procedure.

V_{comp} – is the shift voltage from the divider for offset voltages compensation.

Note that signs of offset voltages were selected to show the worst-case error, see Figure 10.

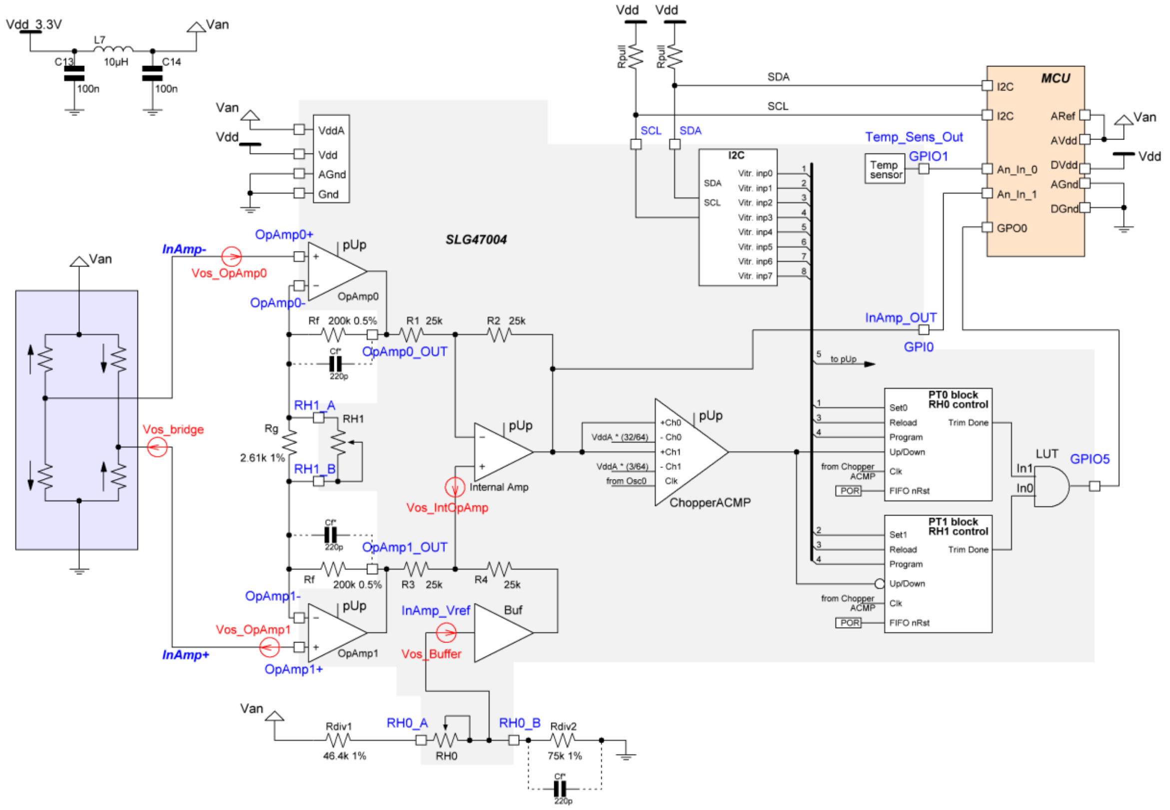


Figure 10: AFE with Offset Sources Placed to Show the Worst Case

4.7 Tuning Gain of AFE

Since the sensors span can be in the range from ±8.1 mV to ±9.2 mV for V_{an} = 3.3 V, the gain of the instrumentation amplifier must be tuned to cover the full output range of the AFE.

The linear output swing of the SLG47004 OpAmps is from GND + 100 mV to V_{DD} - 100 mV. It's proposed to use the output range from V_{DDA}*(32/64) to (V_{DDA} - V_{DDA}*(3/64)) for positive sensor output and from V_{DDA}*(32/64) to V_{DDA}*(3/64) for negative sensor output. V_{DDA}*(3/64) is the threshold for internal Chopper ACMP, which is used for gain tuning. V_{DDA}*(3/64) = 0.155 V for V_{DDA} = 3.3 V.

4.8 Algorithm for Tuning Gain and Compensating Offset of the System

The initial value of RH0 and RH1 are 100 KΩ (80 KΩ in the worst case), code = 1024.

- 1st step: offset compensation. Load the sensor with zero load (no load). Send to the SLG47004 I^2C command to set the V_{irt} Input0 (pulse to Set0 input of PT0 block) to logic High level. This will start the Auto-Trim procedure for RH0. Then I^2C master should clear the V_{irt} Input0 of the SLG47004, which is connected to Set0 input. During the Auto-Trim procedure the SLG47004 changes the value of RH0 until the output voltage of AFE reaches V_{DDA}/2. After the end of the Auto-Trim procedure (logic level of Idle/nActive output of PT block becomes High) the system is ready for the next step.
- 2nd step: gain tuning. Load the sensor with a defined load. Send to the SLG47004 I^2C command to set V_{irt} Input1 (pulse to Set1 input of PT block) to logic High level. This will start the Auto-Trim procedure for RH1. Then I^2C should clear the V_{irt} Input1 of the SLG47004, which is connected to Set1 input. During this Auto-Trim procedure the SLG47004 changes the value of RH1 until the output voltage of AFE reaches (V_{DDA}*(3/64)). After the end of the Auto-Trim procedure (logic level of Idle/Active output of PT block becomes High) the system is ready for the next step.
- 3rd step: offset compensation. This step is the same as the 1st step.

Optionally, if higher accuracy is required, the User can add more offset/gain calibration steps considering the following limitations:

- The Auto-Trim procedures of total offset compensation and system gain error must be done iteratively starting and finishing with the total offset compensation.
- Total system offset (sensor offset + OpAmp1 offset + OpAmp2 offset) must not be greater than $V_{sensor\_output\_range}$/2.

Expected Gain errors after each tuning iteration are shown in Table 2.

Table 2: Expected Gain of AFE during Auto-Trim Procedure

	Gain	Gain Error, %
Etalon gain	174.2	-
1st iteration (offset trim, then gain tuning)	170.9	1.89%
2nd iteration (offset trim, then gain tuning)	173.4	0.49%
3rd iteration (offset trim, then gain tuning)	174.4	0.09%

After the 3rd iteration the gain error is associated with the step error of digital rheostat.

4.9 Offset Compensation Accuracy

Assume that the Auto-Trim is done at temperature = 25 °C. The gain of the instrumentation amplifier is 273.3, RH resistance is 100 kΩ for code = 1024. Table 3 shows the accuracy of setting zero point (offset compensation).

Table 3: Accuracy of Setting Zero Point

Parameter	Value, V	Error in % of output sensor range
Step near set point ($V_{out}[N_{RH0}] – V_{out}[N_{RH0}-1]$) (Note 1)	0.0006	0.04 %
Step near set point considering rheostat DNL (Note 2)	0.0012	0.08 %
Step error considering DNL and ACMP offset (Note 3)	0.0015	0.1 %

Note 1 The minimum achievable error of the Auto-Trim system is one trim step (± 1 of digital rheostat code, see Figure 11).

Note 2 Multiply 'Step near set point' value ($V_{out}[N_{DR}]$- $V_{out}[N_{DR}-1]$) by 2 (DNL error).

Note 3 Add the typical Chopper ACMP offset of 300 μV to the previous value.

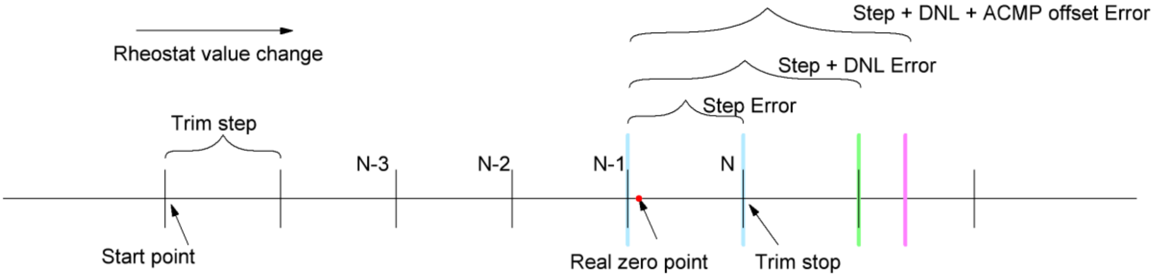


Figure 11: Error Sources of Offset Compensation Process

In the case of 10-bit ADC, the maximum error of the trimmed system is:

$$Verror \cdot \frac{1024}{Van} = 0.47\ LSB\ of\ ADC$$

Please note that this error value is independent of V_{an} voltage.

5 AFE with Internal Voltage Reference Source

5.1 Hardware Setup of AFE with Internal Voltage Reference

The SLG47004 allows powering all analog components of the AFE (sensor, DAC, and reference for Chopper ACMP) from an internal voltage source, see Figure 12. For this purpose, the SLG47004 has a special high drive buffer (HD Buffer macrocell).

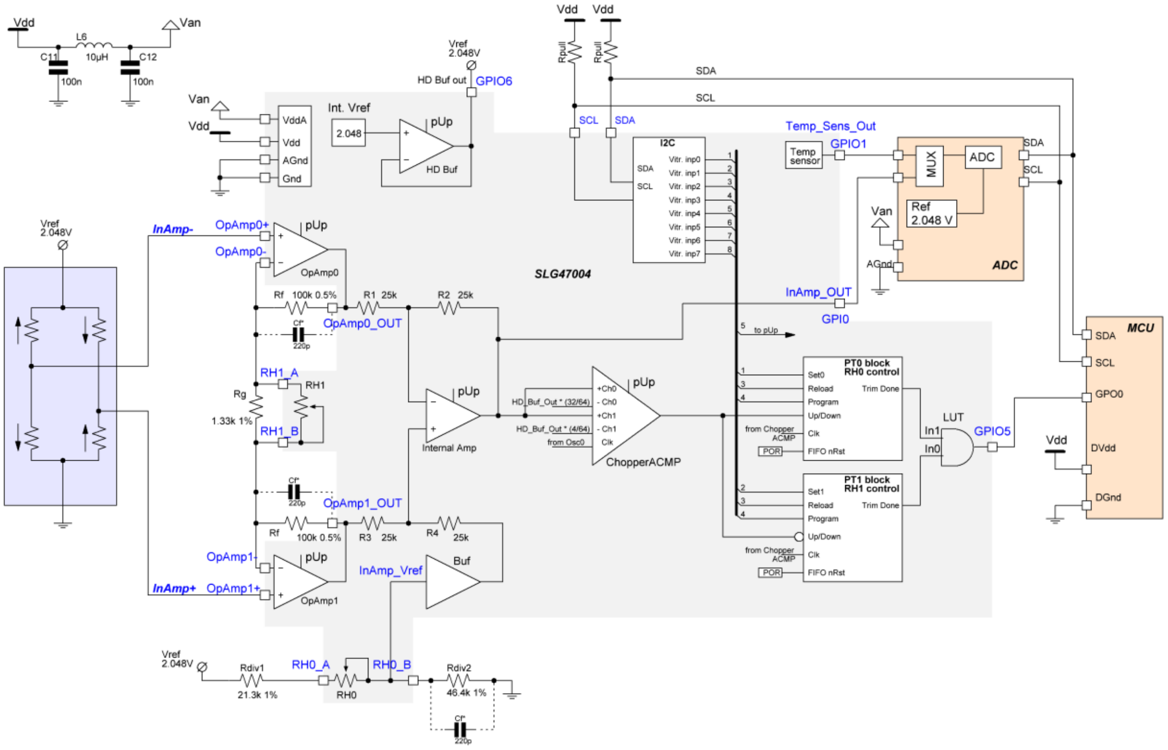


Figure 12: Analog Front-End with Internal Voltage Reference

5.2 Precision Characteristics of Sensor at 2.048 V Supply Voltage

Characteristics of the pressure sensor at 2.048 V supply voltage are shown in Table 4. All other precision characteristics from Table 1 remain unchanged.

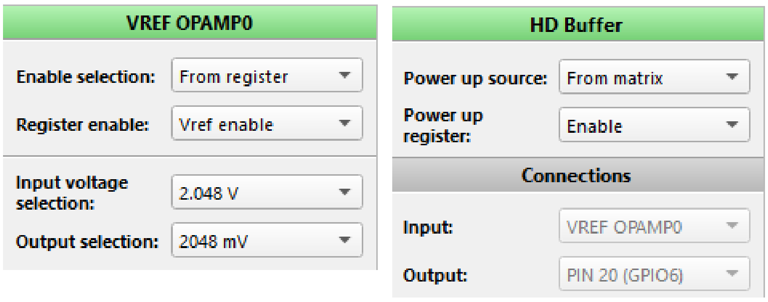
Table 4: Characteristics of Sensor at 2.048 V Supply Voltage

Parameter	Description	Value	Unit
ΔP	Pressure Range	±6.0	kPa
KV_{out}	Output Voltage Span	±5.04 (min), ±5.32 (typ), ±5.73 (max)	mV
K_{os_out}	Null Offset	±0.154 (max)	mV
dV_{os_bridge}/dT	Offset Temperature Drift (T = 0 to 50 °C)	±0.6 (max)	%FSS

5.3 Internal Macrocells Configurations

5.3.1 HD Buffer and OpAmp0 Vref Configurations

The HD Buffer shares the voltage reference with OpAmp0 Macrocell. Note that Vref can be connected (or disconnected) to OpAmp0 or HD Buffer macrocells independently. The configurations of HD Buffer and OpAmp0 Vref are shown in Figure 13.



VREF OPAMP0

Enable selection: From register

Register enable: Vref enable

Input voltage selection: 2.048 V

Output selection: 2048 mV

HD Buffer

Power up source: From matrix

Power up register: Enable

Connections

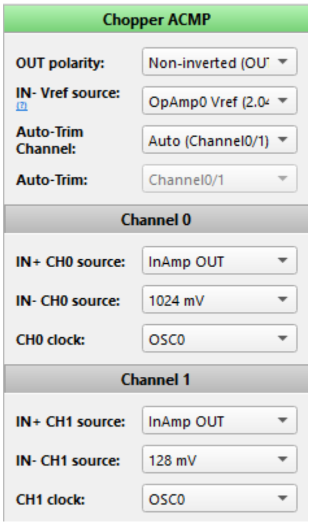
Input: VREF OPAMP0

Output: PIN 20 (GPIO6)

Figure 13: OpAmp Vref and HD Buffer Configurations

5.3.2 Chopper ACMP Configuration for AFE with 2.048 V Voltage Reference

Chopper ACMP configuration is shown in Figure 14.



Chopper ACMP

OUT polarity: Non-inverted (OU

IN- Vref source: OpAmp0 Vref (2.0

Auto-Trim Channel: Auto (Channel0/1)

Auto-Trim: Channel0/1

Channel 0

IN+ CH0 source: InAmp OUT

IN- CH0 source: 1024 mV

CH0 clock: OSC0

Channel 1

IN+ CH1 source: InAmp OUT

IN- CH1 source: 128 mV

CH1 clock: OSC0

Figure 14: Chopper ACMP Configuration for AFE with 2.048 V Voltage Reference

5.4 Gain Resistor and DAC Divider Calculations for AFE with 2.048 V Voltage Reference

Considering the output span of the sensor (from 5.04 mV to 5.73 mV at V_{an} = 2.048 V), the output voltage range of AFE must be ($\frac{Vref}{2} - Gain\_ref\_ChopACMP$).

$$Gain\_ref\_ChopACMP = 2.048 \cdot \left(\frac{4}{64}\right) = 0.128 \text{ mV}.$$

Using equation (3),

$$Gain_{max} = \left(\frac{1}{2} - \frac{4}{64}\right) \cdot \frac{1}{2.46} \cdot 1000 = 177.8,$$

$$Gain_{min} = \left(\frac{1}{2} - \frac{4}{64}\right) \cdot \frac{1}{2.80} \cdot 1000 = 156.3.$$

Gain resistor R_g = 1.33 kΩ, R_f = 100 kΩ. The range of offset compensation is V_{comp} = ±(177.9*0.00215) = 0.382 V. The divider resistors R_{div1} = 21.3 kΩ, R_{div2} = 46.4 kΩ. The offset of the HD Buffer is 3 mV.

6 Software Simulation and Hardware Prototype Testing

Figure 15, Figure 16, Figure 17, and Figure 18 show the Auto-Trim process. Figure 15, Figure 16, and Figure 17 show the case when the duration of the pulse at Set input of RH is shorter than the duration of the Auto-Trim process. For this case, the stop condition for the Auto-Trim process is after the 2nd time there is a change at Up/Down input at the rising edge of the Clock input. Please refer to the datasheet [5] to get more information about the Auto-Trim process.

If the User holds the Set input at high level, the Auto-Trim system will continue to operate and the output will follow the reference point, see Figure 18.

The maximum time of the first Auto-Trim iteration is $RH\_code/f_{Auto\text{-}Trim} = 511/2048 = 250$ ms.

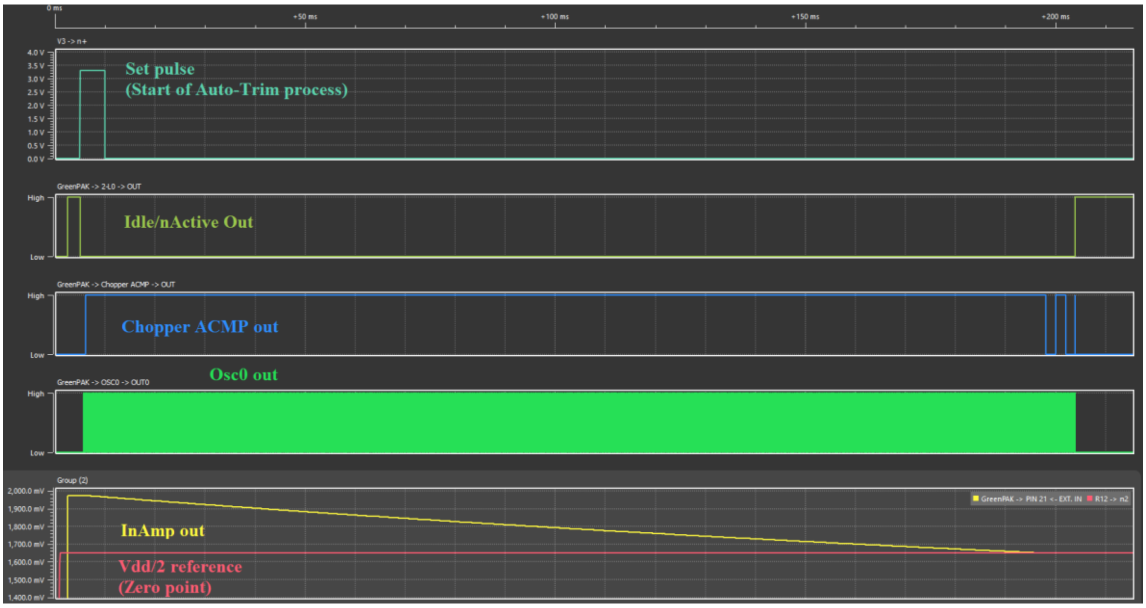


Figure 15: Software Simulation Results of Offset Correction Process

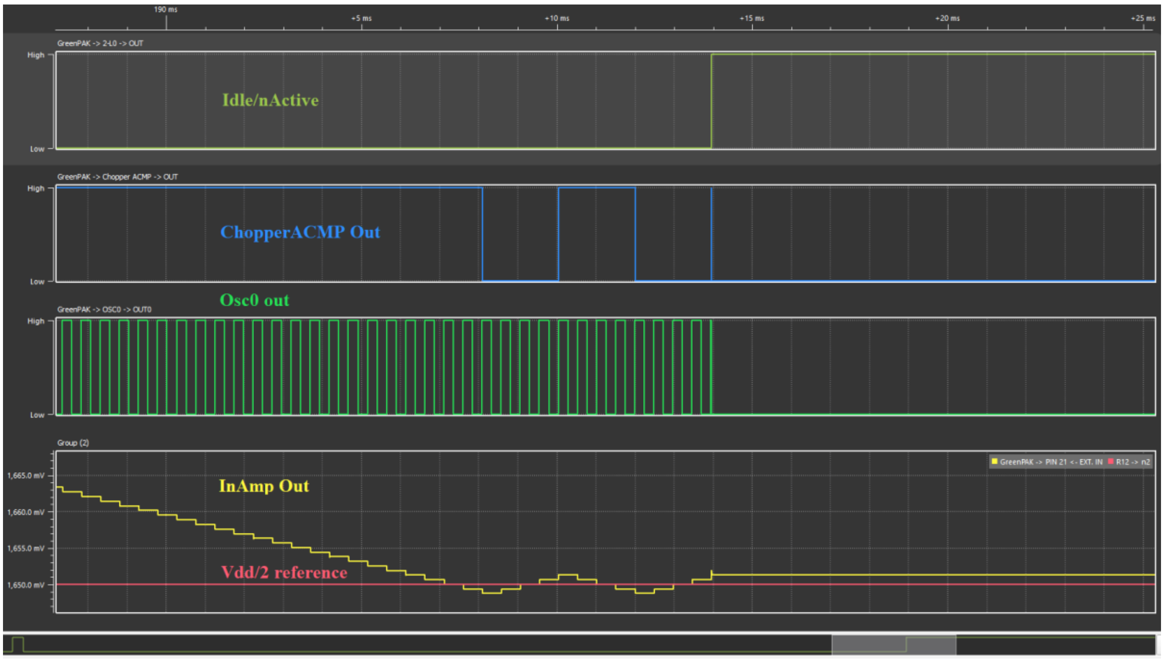


Figure 16: Software Simulation Results of Offset Correction Process, Enlarged

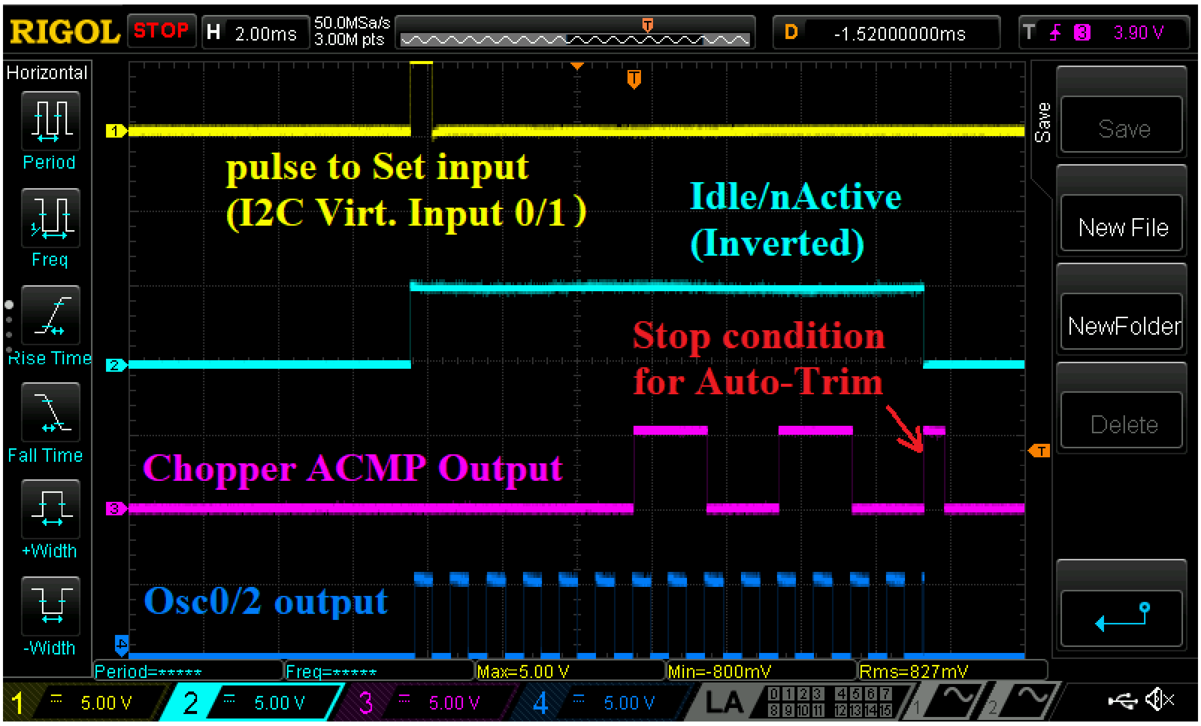


Figure 17: Auto-Trim Procedure with Short Pulse at Set Input of RH

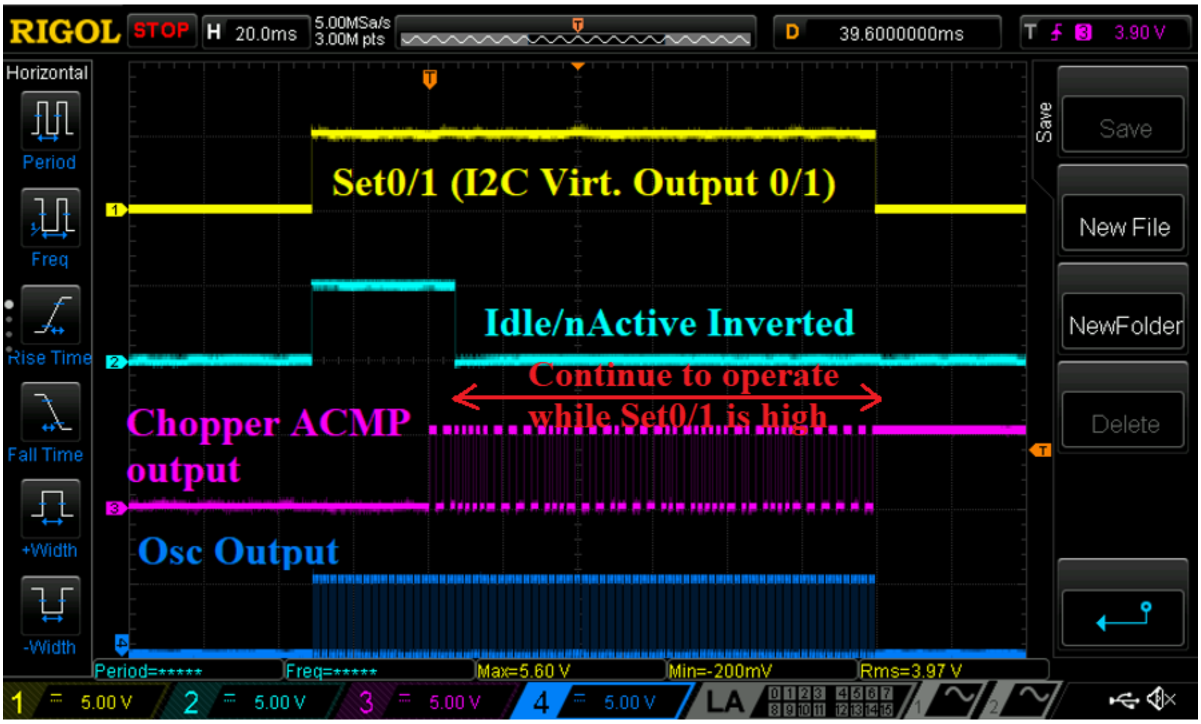


Figure 18: Auto-Trim Procedure with Long Pulse at Set Input of RH

7 Conclusions

The application note describes the design procedure of the analog front-end for a Wheatstone bridge pressure sensor. A unique Auto-Trim feature of the SLG47004 is used to compensate for the offset of operational amplifiers and sensor, and to tune the gain of the AFE.

It was shown how to calculate gain and DAC resistors to cover the full output range and full trim range of the instrumentation amplifier.

To achieve the best precision, it's recommended to use iterative procedures of offset compensation and then gain tuning. The first and last procedure should be offset compensation. Practical results show that the best precision is achieved after the 3rd iteration. For the sensor and AFE described in this application note, the gain and offset errors after the Auto-Trim procedures are ≈0.1% of the sensor range.

Revision History

Revision	Date	Description
1.0	03-Nov-2020	Initial Draft

IMPORTANT NOTICE AND DISCLAIMER

RENESAS ELECTRONICS CORPORATION AND ITS SUBSIDIARIES (“RENESAS”) PROVIDES TECHNICAL SPECIFICATIONS AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS OR IMPLIED, INCLUDING, WITHOUT LIMITATION, ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, OR NON-INFRINGEMENT OF THIRD-PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for developers who are designing with Renesas products. You are solely responsible for (1) selecting the appropriate products for your application, (2) designing, validating, and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, or other requirements. These resources are subject to change without notice. Renesas grants you permission to use these resources only to develop an application that uses Renesas products. Other reproduction or use of these resources is strictly prohibited. No license is granted to any other Renesas intellectual property or to any third-party intellectual property. Renesas disclaims responsibility for, and you will fully indemnify Renesas and its representatives against, any claims, damages, costs, losses, or liabilities arising from your use of these resources. Renesas' products are provided only subject to Renesas' Terms and Conditions of Sale or other applicable terms agreed to in writing. No use of any Renesas resources expands or otherwise alters any applicable warranties or warranty disclaimers for these products.

(Disclaimer Rev.1.01)

Corporate Headquarters

TOYOSU FORESIA, 3-2-24 Toyosu,
Koto-ku, Tokyo 135-0061, Japan
www.renesas.com

Trademarks

Renesas and the Renesas logo are trademarks of Renesas Electronics Corporation. All trademarks and registered trademarks are the property of their respective owners.

Contact Information

For further information on a product, technology, the most up-to-date version of a document, or your nearest sales office, please visit www.renesas.com/contact-us/.

© 2026 Renesas Electronics Corporation. All rights reserved.