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M32C/83Group

[CAN] CAN Interrupt

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1. Abstract

This document describes about CAN interrupt for M32C/83 group.

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2. Types of Interrupts

The CAN module of the M32C/83 group can use the following interrupts:

- CAN receive interrupt
- CAN transmit interrupt
- CAN bus error interrupt
- CAN error-passive interrupt
- CAN bus-off interrupt
- CAN wakeup interrupt

All of the above interrupts, except the CAN wakeup interrupt, are assigned to the same interrupt vector. This interrupt vector can be selected from three: CAN interrupt 0, CAN interrupt 1, and CAN interrupt 2. Timer A3 or $\overline{\text{INT1}}$ are used for the CAN wakeup interrupt.

Table 1 shows the CAN interrupt registers that need to be set in order to use CAN interrupt 0, CAN interrupt 1, or CAN interrupt 2.

Figure 1 shows the block diagram of CAN interrupts.

Table 1. Registers for CAN interrupt

	CAN interrupt 0	CAN interrupt 1	CAN interrupt 2
Interrupt control i register	CAN0IC(009D ₁₆)	CAN1IC(007F ₁₆)	CAN2IC(0081 ₁₆)
Interrupt request register i	IIO9IR:bit7(00A9 ₁₆)	IIO10IR:bit7(00AA ₁₆)	IIO11IR:bit7(00AB ₁₆)
Interrupt enable register i	IIO9IE:bit7(00B9 ₁₆)	IIO10IE:bit7(00BA ₁₆)	IIO11IE:bit7(00BB ₁₆)

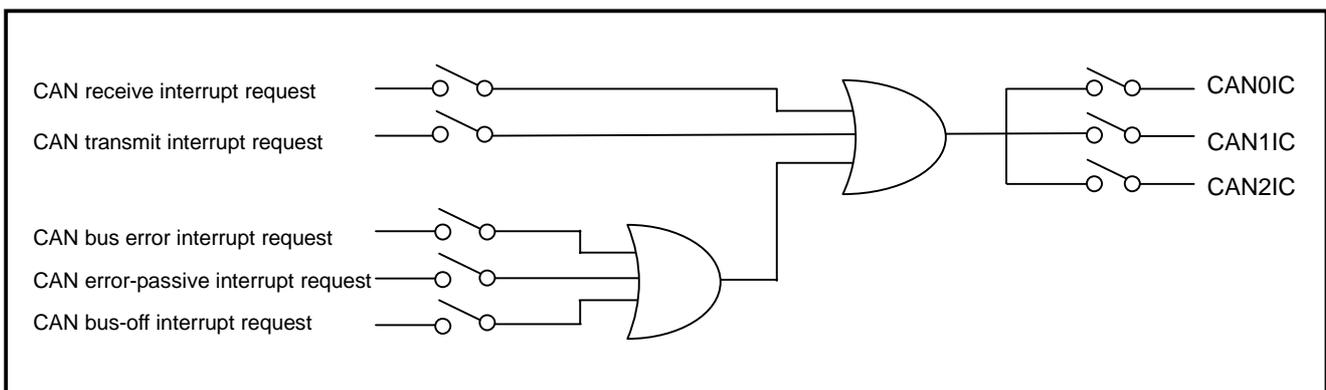


Figure 1. Block diagram of CAN Interrupts

3. CAN Receive Interrupt

To use the CAN module's receive interrupt of the M32C/83 group, the following registers need to be set.

- CAN interrupt control i register (CANiIC)(i = 0, 1, 2)
- Interrupt request register i (IIOiIR)(i = 9,10,11)
- Interrupt enable register i (IIOiIE)(i = 9,10,11)
- CAN0 slot interrupt mask register (C0SIMKR)

Figure 2 shows the setting procedure of CAN receive interrupt.

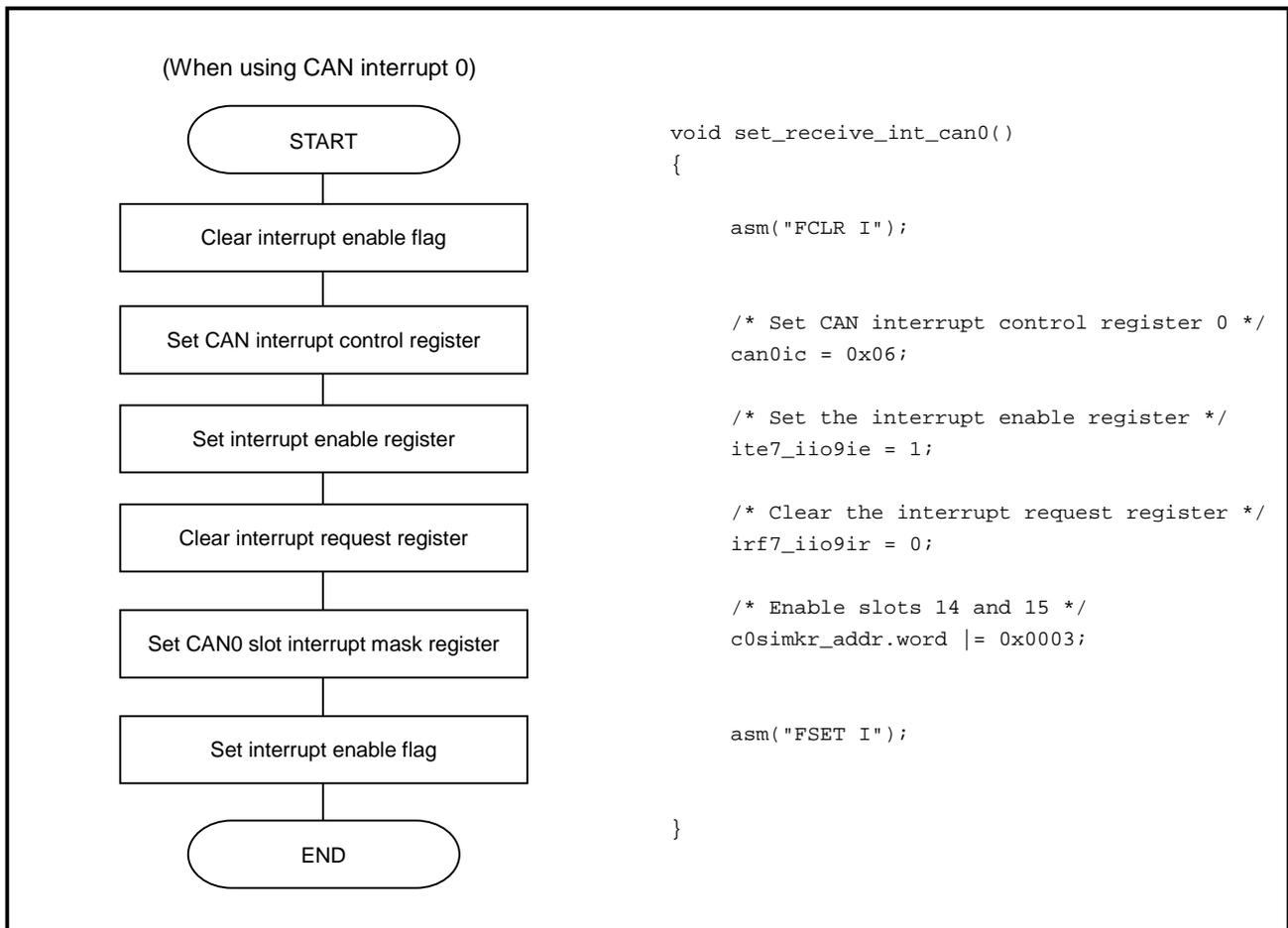


Figure 2. Setting procedure of CAN receive interrupt

4. CAN Transmit Interrupt

To use the CAN module's transmit interrupt of the M32C/83 group, the following registers need to be set.

- CAN interrupt control i register (CANiIC)(i = 0, 1, 2)
- Interrupt request register i (IIOiIR)(i = 9,10,11)
- Interrupt enable register i (IIOiIE)(i = 9,10,11)
- CAN0 slot interrupt mask register (C0SIMKR)

Figure 3 shows the setting procedure of CAN transmit interrupt.

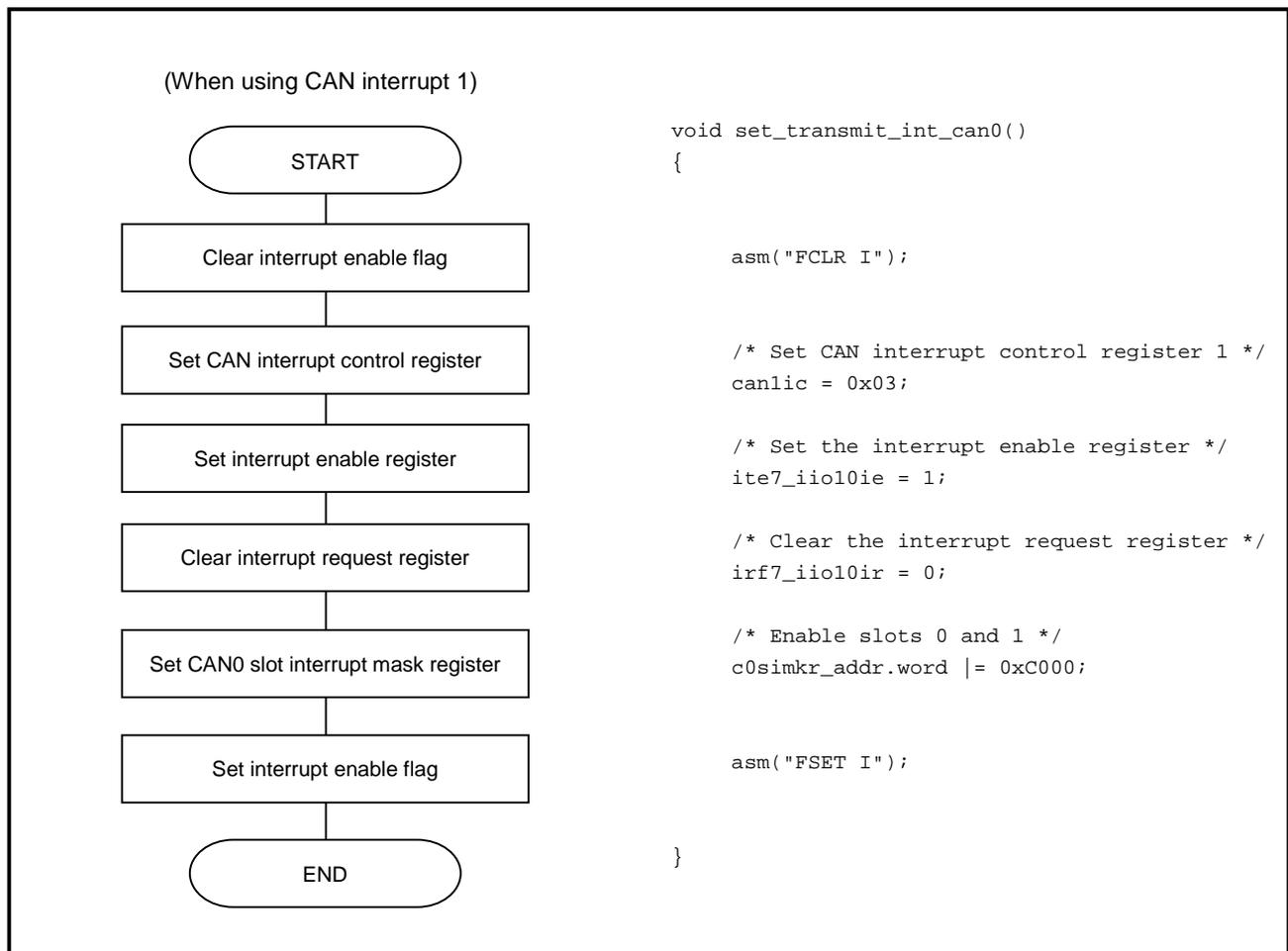


Figure 3. Setting procedure of CAN transmit interrupt

5. CAN Error Interrupt

The M32C/83 group has the following three sources of error-related interrupts

These error interrupts can be individually enabled or disabled.

- Occurrence of a bus error
- Transition from error-active to error-passive state
- Transition from error-passive to bus-off state

To use CAN error interrupts of the M32C/83 group, the following registers need to be set.

- CAN interrupt control i register (CANiIC)(i = 0, 1, 2)
- Interrupt request register i (IIOiIR)(i = 9,10,11)
- Interrupt enable register i (IIOiIE)(i = 9,10,11)
- CAN0 error interrupt mask register (C0EIMKR)
- CAN0 error interrupt status register (C0EISTR)

Figure 4 shows the setting procedure of CAN error interrupt.

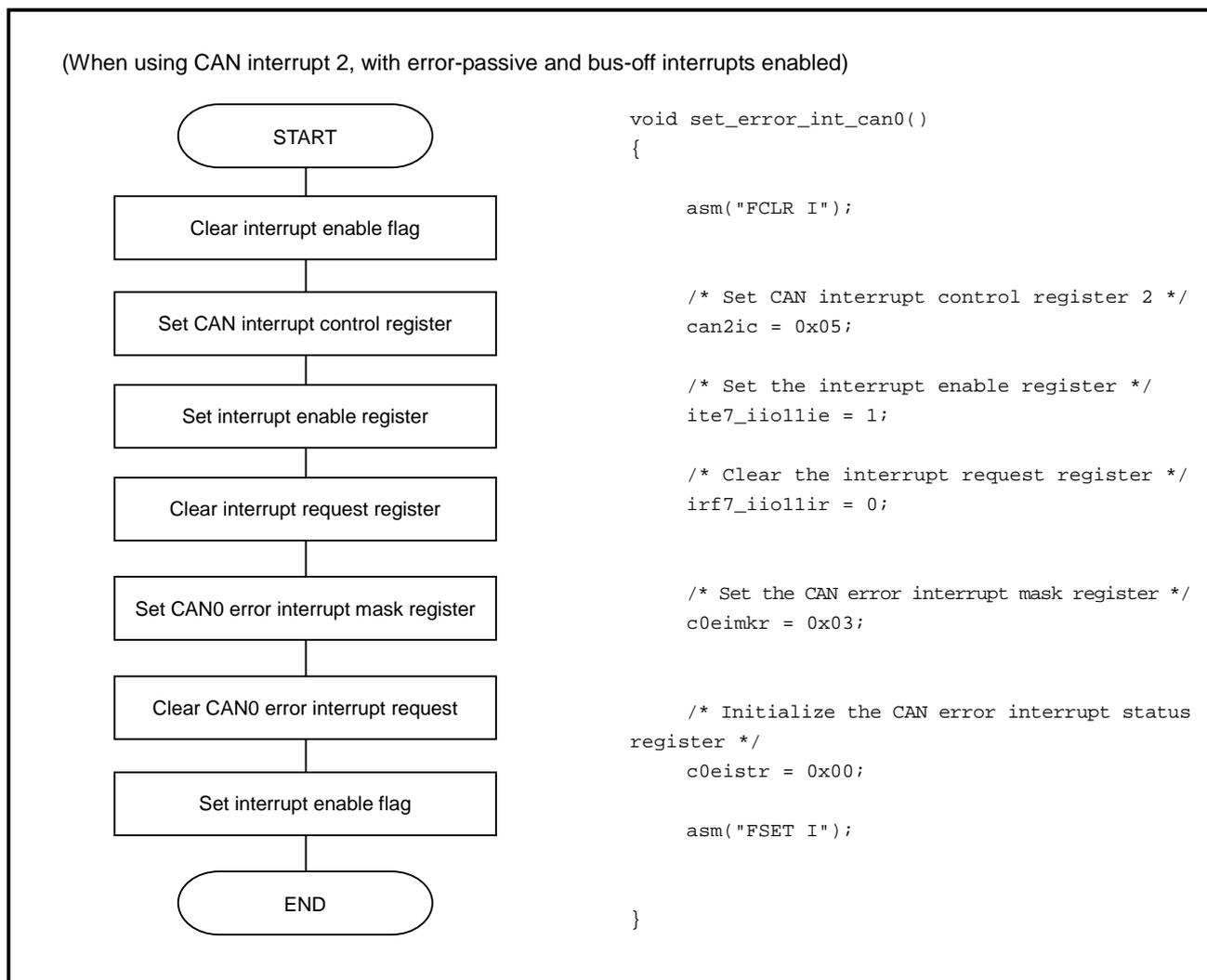


Figure 4. Setting procedure of CAN error interrupt

6. CAN Wakeup Interrupt

CAN wakeup interrupt of the M32C/83 group uses timer A3 interrupt (event counter mode) when using P7_7 as CAN input port and $\overline{\text{INT1}}$ when using P8_3 as CAN input port.

Figures 5 and 6 show the setting procedure of CAN wakeup interrupt.

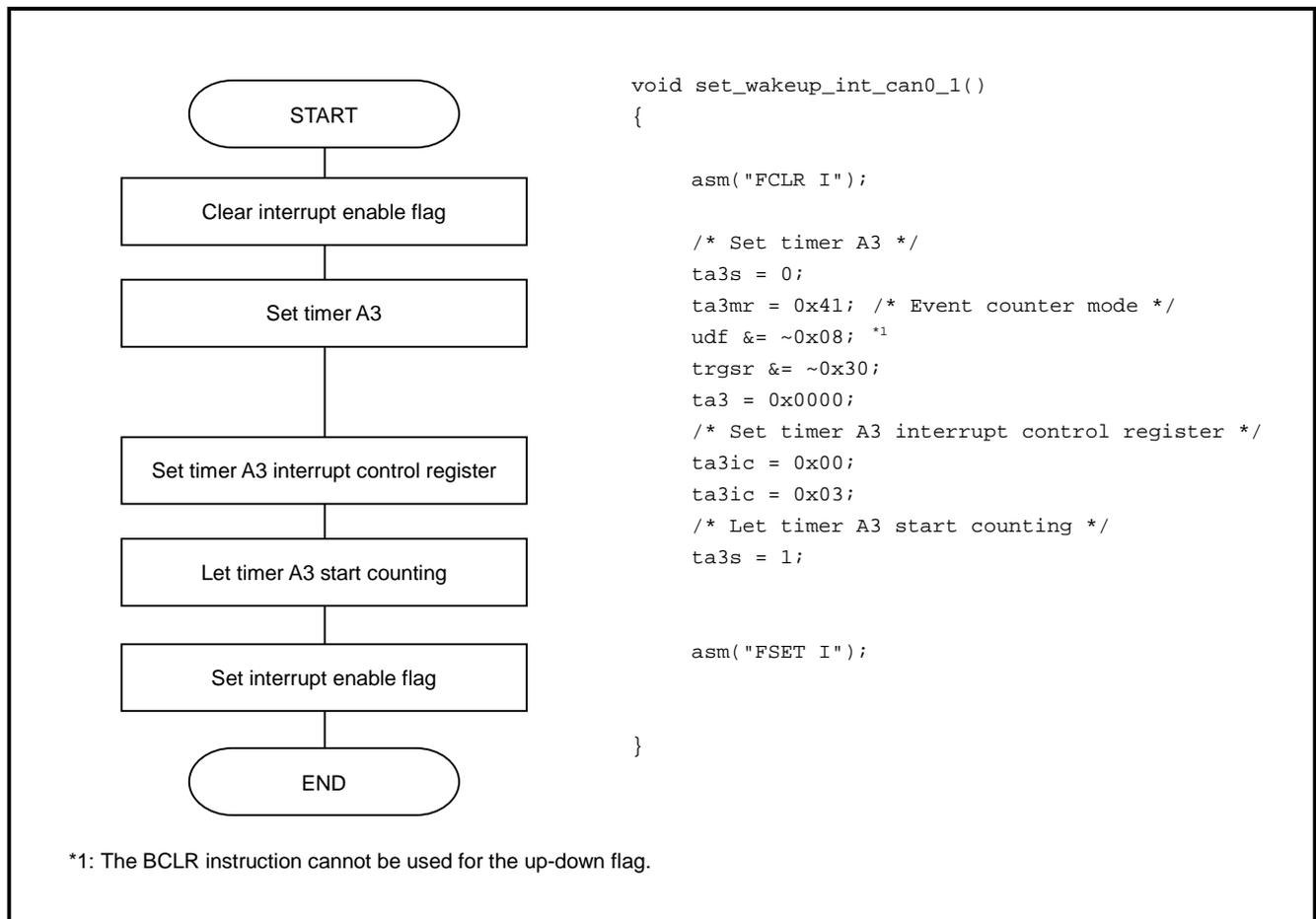


Figure 5. Setting procedure of CAN wakeup interrupt when using P7_7 as CAN input port

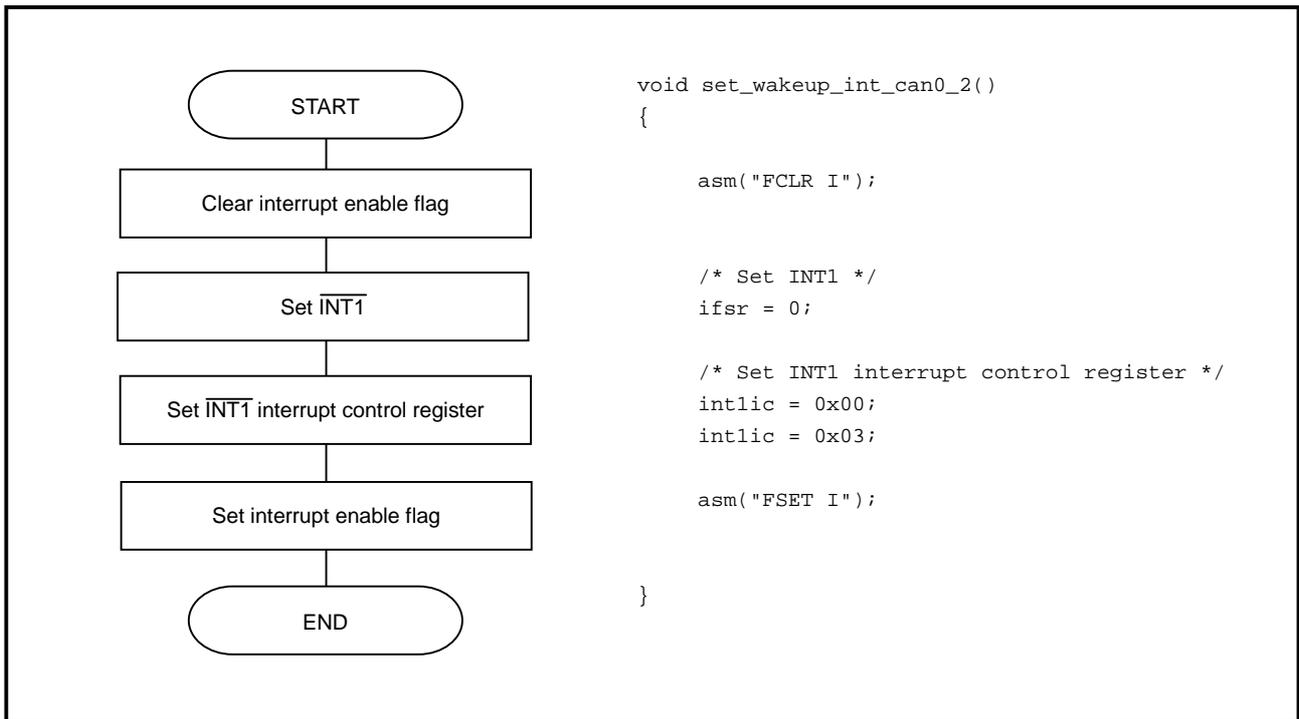


Figure 6. Setting procedure of CAN wakeup interrupt when using P8_3 as CAN input port

7. Precaution about Sample Program in This Document

7.1. Symbol description of each register

Symbol of each register which is included in the sample program of this document complies with the description of C-language SFR header file for Renesas standard M32C/83 group.

7.2. Structure of Sample Program

Structure which is included in the sample program of this document is following configuration.

```
/* Definition of a standard data frame */
typedef struct{
    unsigned short id;
    unsigned char dlc;
    unsigned char data[8];
}can_std_data_def;

/* Definition of a standard remote frame */
typedef struct{
    unsigned short id;
    unsigned char dlc;
}can_std_remote_def;

/* Definition of an extend data frame */
typedef struct{
    unsigned long id;
    unsigned char dlc;
    unsigned char data[8];
}can_ext_data_def;

/* Definition of an extend remote frame */
typedef struct{
    unsigned long id;
    unsigned char dlc;
}can_ext_remote_def;
```

7.3. Infinite loop of “while”

In some part of the sample program an infinite loop is formed with “while”, however, it is described in this way so that the description could be simplified. In actual programming, each while-loop must have a time limit. At over-time it should come out of the loop.

8. Reference

- M32C/83 group Data Sheet
- M32C/83 group Hardware Manual

When using this document, be sure to download the latest manual from following Renesas technology home page.

9. Home Page and Contact for Technical Support.

- Renesas technology corporation semiconductor home page
<http://www.renesas.com>
- Contact for technical support about CAN MCU
E-mail : csc@renesas.com

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