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M32C/83Group

[CAN] CAN Configuration

REJ05B0149-0100Z
Rev.1.00
July 24, 2003

1. Abstract

This document describes about CAN configuration for M32C/83 group.

The following is contents of this document.

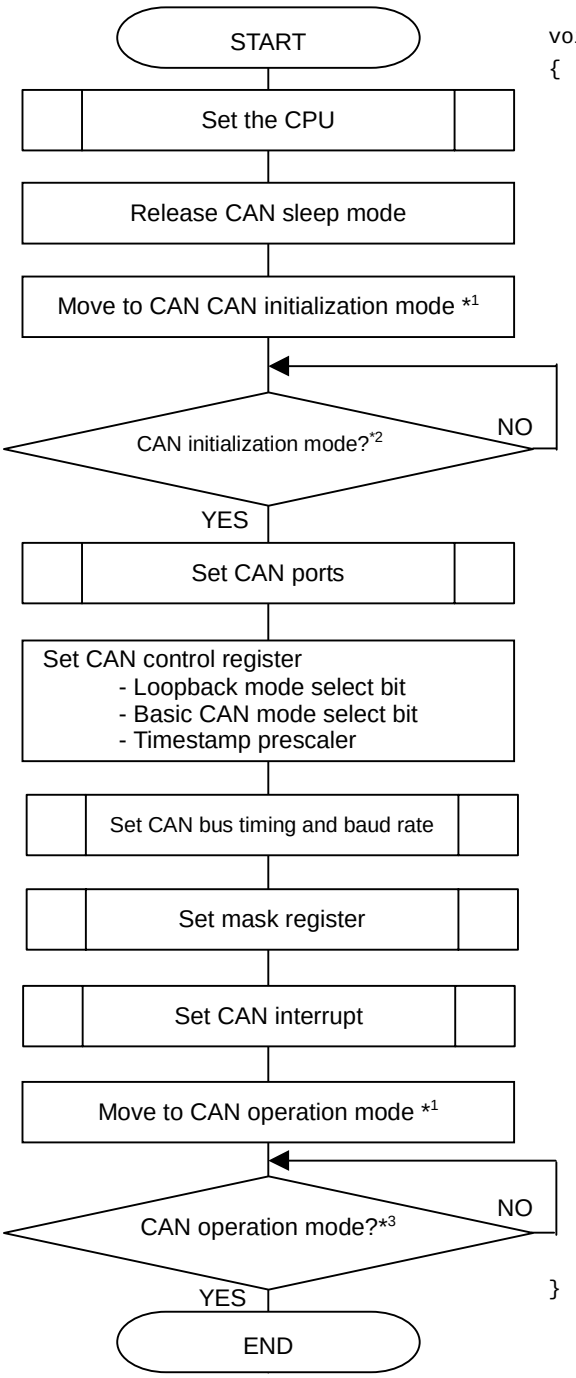
Table of contents

2. CAN Configuration Procedure

CAN configuration refers to initializing the microcomputer to make it capable of CAN communication. In CAN configuration, you set the CAN bit timing and the mode of the CAN module. CAN configuration must be performed while the CAN module is in CAN initialization mode.

2.1. CAN Configuration

Figure 1 shows the setting procedure of CAN configuration.




```
void config_can0()
{
     /* Set the CPU */ Refer to Figure 2
     initial_cpu_for_can();

     /* Release CAN sleep mode */
     c0slpr = 1;

     /* Move to CAN initialization mode */
     c0ctlr0_addr.word = 0x0011;


     /* Check CAN initialization mode */
     while(! state_reset_c0str){}

     /* Set CAN ports */ Refer to Figure 3
     set_p77_as_canin();
     set_p76_as_canout();

     /* Set CAN control register */
     loopback_c0ctlr = 0;
     basiccan_c0ctlr= 0;
     tspre_c0ctlr = 0;

     /* Set CAN baud rate */ Refer to Figure 4
     set_bitrate_can0();

     /* Set CAN mask register */ Refer to Figure 5
     set_mask_can0();

     /* Set the CAN interrupt control register */
     set_receive_int_can0();

     /* Move to CAN operation mode */
     c0ctlr0_addr.word &= ~0x0011;


     /* Check CAN operation mode */
     while(state_reset_c0str){}

}
```

*1: When the CAN module moves to CAN initialization mode while it is transmitting, it immediately stops sending a frame and its CAN output port gets the recessive level.

*2: When the CAN module moves to CAN initialization mode from CAN operation mode, always be sure to check the CAN reset status flag. Although this confirmation step is written as an infinite loop here, give it a time-out time equal to or greater than 2 clock cycles in actually programming.

*3: When the CAN module moves to CAN operation mode from CAN initialization mode, always be sure to check the CAN reset status flag. Although this confirmation step is written as an infinite loop here, give it a time-out time equal to or greater than 2 clock cycles in actually programming.

Figure 1 Setting procedure of CAN configuration

2.2. Setting the CPU

To access the CAN module's SFR area, the CPU must be set as follows:

- CPU main clock divide-by ratio: Non-divide mode
- SFR area access: 2-wait mode

Figure 2 shows the setting procedure of CPU initialization to access the CAN module's SFR.

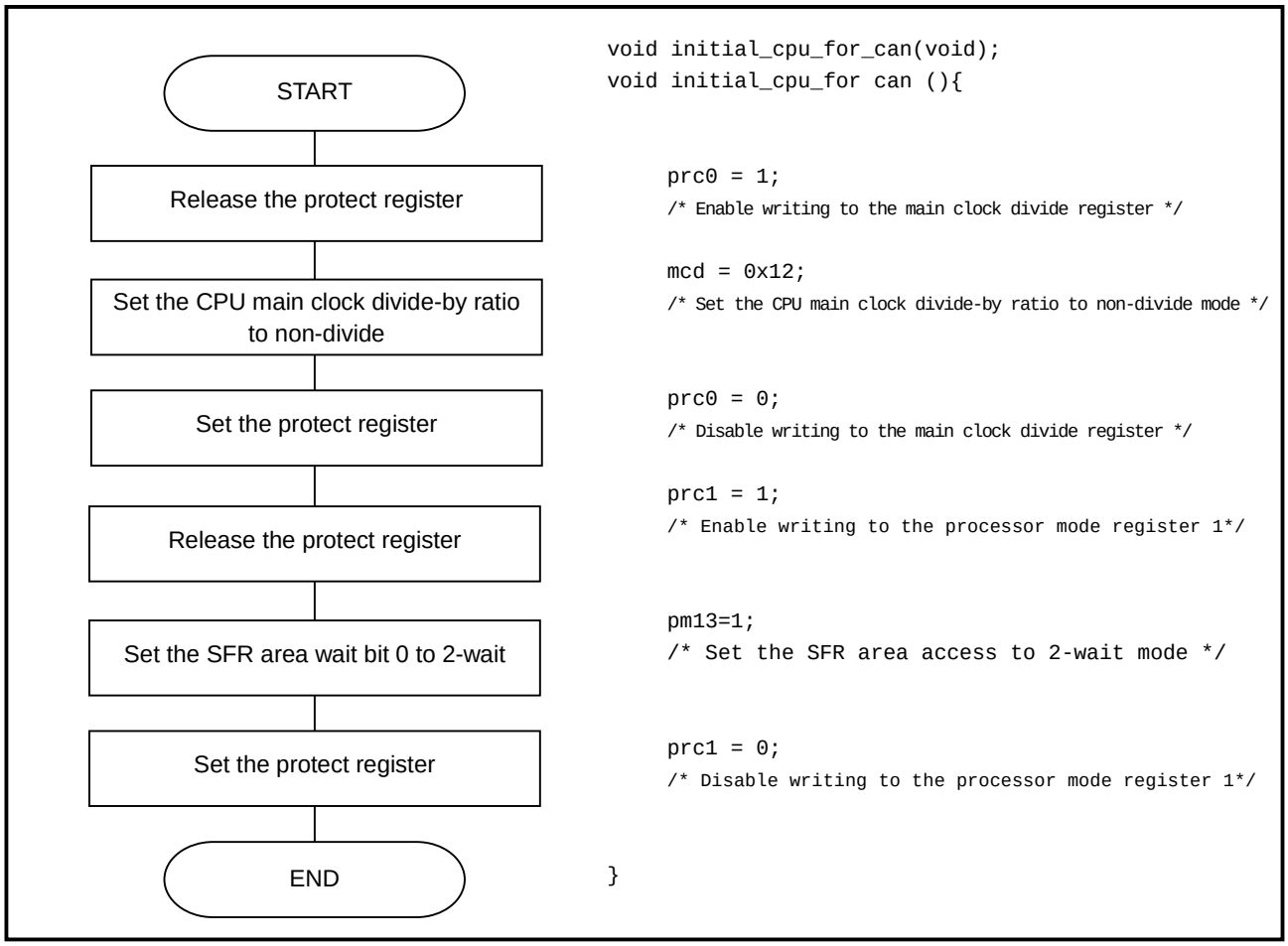


Figure 2 Setting procedure of CPU initialization

2.3. CAN Input / Output Ports

The CAN input ports are assigned to P7_7 and P8_3 and the CAN output ports are assigned to P7_6 and P8_2. The following registers are used to select the input/output ports used.

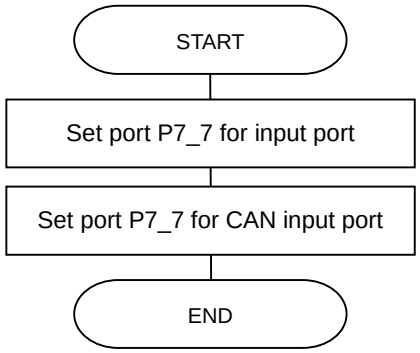
- Port direction register (PD7, PD8)
- Input function select register (IPS)
- Function select register A1 (PS1)
- Function select register A2 (PS2)
- Function select register B1 (PSL1)
- Function select register B2 (PSL2)
- Function select register C (PSC)

Table 1 shows the setting value of each registers and Figure 3 shows the setting procedure of CAN input/output ports.

Table 1 Setting value for CAN I/O ports

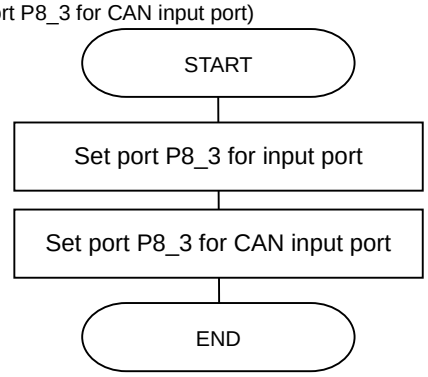
Registers to set	Symbol	Address	Bit	CAN input port		CAN output por	
				$P7_7$	$P8_3$	$P7_6$	$P8_2$
Port $P7_6$ direction register	PD7	$03C3_{16}$	Bit6	-	-	1	-
Port $P7_7$ direction register			Bit7	0	-	-	-
Port $P8_2$ direction register	PD8	$03C6_{16}$	Bit2	-	-	-	1
Port $P8_3$ direction register			Bit3	-	0	-	-
Input function select register	IPS	0178_{16}	Bit3	0	1	-	-
Function select register A1	PS1	$03B1_{16}$	Bit6	-	-	1	-
			Bit7	0	-	-	-
Function select register A2	PS2	$03B4_{16}$	Bit2	-	-	-	1
Function select register B1	PSL1	$03B3_{16}$	Bit6	-	-	0	-
Function select register B2	PSL2	$03B6_{16}$	Bit2	-	-	-	1
Function select register C	PSC	$03AF_{16}$	Bit6	-	-	1	-

(To set port P7_7 for CAN input port)



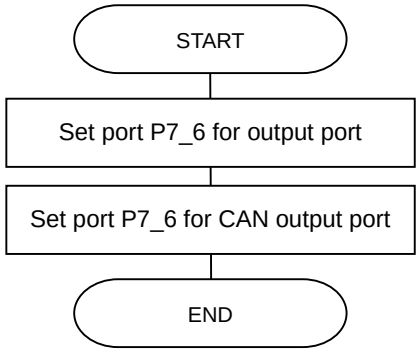

```
void set_p77_as_canin()
{

     /* Set I/O port */
     pd7_7 = 0;

     /* Set input function select register */
     ps1_7 = 0;
     ips3_ips = 0;
}
```

To set port P8_3 for CAN input port)



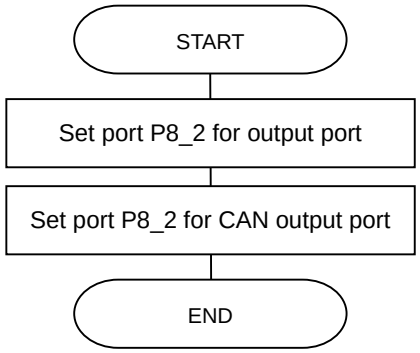

```
void set_p83_as_canin()

{
     /* Set I/O port */
     pd8_3 = 0;

     /* Set input function select register */
     ips3_ips = 1;

}
```

To set port P7_6 for CAN output port)




```
void set_p76_as_canout()
{
     /* Set I/O port */
     pd7_6 = 1;
     pd7_6 – 1;
     /* Set function select register */
     ps1_6 = 1;
     psl1_6 = 0;
     psc_6 = 1;
}
```

To set port P8_2 for CAN output port)




```
void set_p82_as_canout()
{
     /* Set I/O port */
     p8_2 = 1;
     pd8_2 = 1
     /* Set function select register */
     ps2_2 = 1;
     psl2_2 = 1;

}
```

Figure 3 Setting procedure of CAN I/O port

2.4. Setting CAN Bit Timing and CAN Baud rate

Figure 4 shows the setting procedure of CAN bit timing and CAN baud rate.

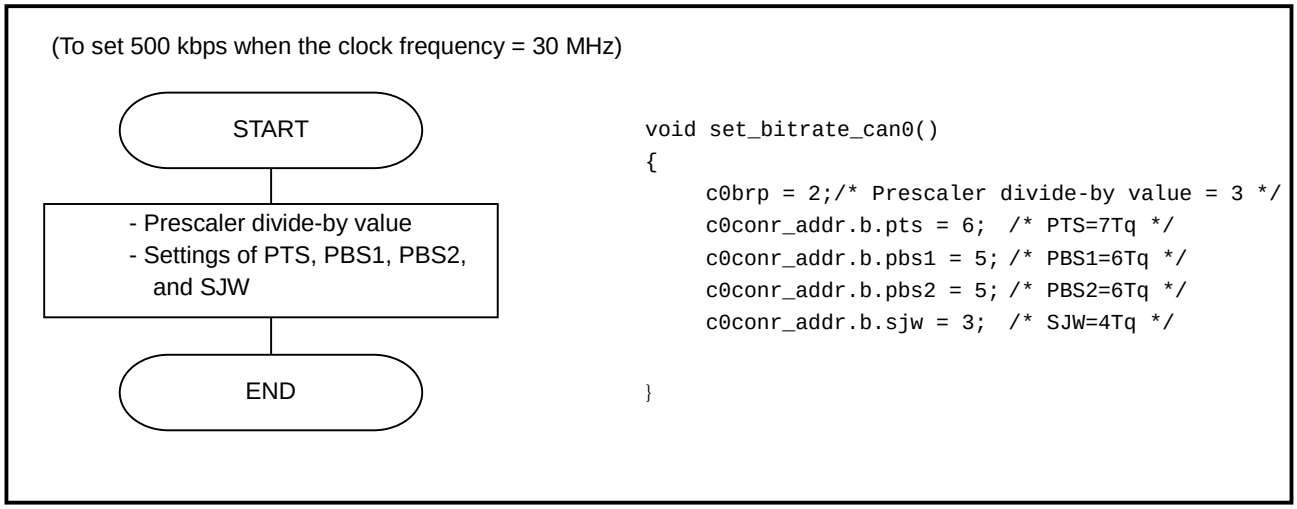
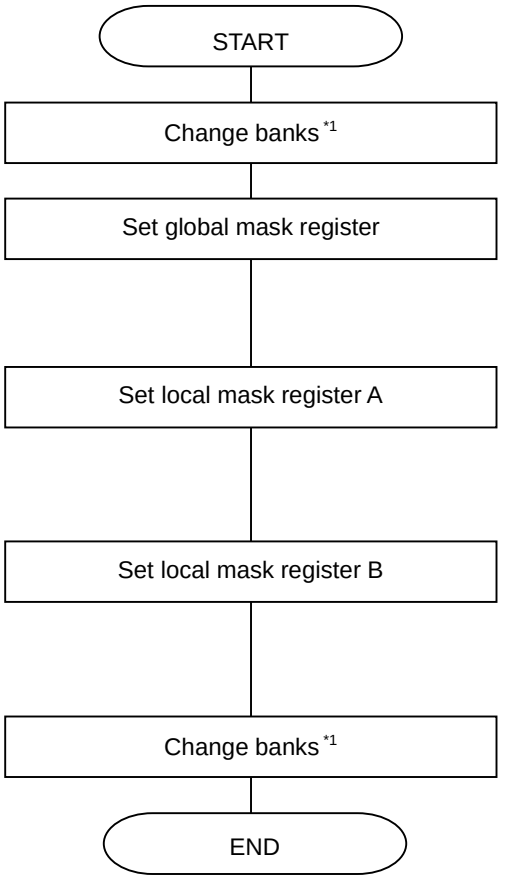


Figure 4 Setting procedure of CAN bit timing and CAN baude rate

2.5. CAN Mask Register

Figure 5 shows the setting procedure of CAN mask register.

(When using Basic CAN mode)




```
void set_mask_can0()
{
     /* Select CAN0 mask register bank */
     banksel_c0ctlr = 1;
     /* Message slots 0–13 receive only the receive IDs
     that have been set */
     c0gmr0 = 0x1F;
     c0gmr1 = 0x3F;
     c0gmr2 = 0x0F;
     c0gmr3 = 0xFF;
     c0gmr4 = 0x3F;
     /* Message slot 14 receives only the receive ID
     that has been set */
     c0lmar0 = 0x1F;
     c0lmar1 = 0x3F;
     c0lmar2 = 0x0F;
     c0lmar3 = 0xFF;
     c0lmar4 = 0x3F;
     /* Message slot 15 receives only the receive ID
     that has been set */
     c0lmbr0 = 0x1F;
     c0lmbr1 = 0x3F;
     c0lmbr2 = 0x0F;
     c0lmbr3 = 0xFF;
     c0lmbr4 = 0x3F;
     /* Select CAN0 message slot control register bank */
     banksel_c0ctlr = 0;
}
```

*1: Make sure the CAN0 bank select bit is set to 1 before accessing the CAN0 mask registers and cleared to 0 after accessing the CAN0 mask registers. This helps to eliminate the need to set the CAN0 bank select bit to 0 each time you access CAN0 message slot i control registers (i = 0–15).

Figure 5 Setting procedure of CAN mask register

3. Precaution about CAN Configuration

3.1. Initialized Registers and Registers holding the value

When the CAN module moves to CAN initialization mode, some of the CAN-related registers are initialized and others hold their values.

Table 2 shows the values of the CAN-related registers at the time moving to CAN initialization mode.

Table 2 Register value of when moving to the CAN initialization mode

Register value	Symbol	Initial value *1	Register values when moving to CAN initialization mode *2	Registers that can be set during CAN initialization mode *3
CAN0 message slot buffer	C0SLOTi_j i=0,1 j=0 - 15	Indeterminate	Holding the value	√
CAN0 control register 0	C0CTLR0	- - - - 0000 - - 01 $0x01_2$	- - - - 00XX - - X1 $X - X1_2$	√
CAN0 status register	C0STR	-000 0-01 0000 0000_2	-00X X-X1 XXXX $XXXX_2$	-
CAN0 extended ID register	C0IDR	0000_{16}	Holding the value	√
CAN0 configuration register	C0CONR	$000-_{16}$	Holding the value	√
CAN0 timestamp register	C0TSR	0000_{16}	0000_{16}	-
CAN0 transmit error count register	C0TEC	00_{16}	00_{16}	√
CAN0 receive error count register	C0REC	00_{16}	00_{16}	-
CAN0 slot interrupt status register	C0SISTR	0000_{16}	Holding the value	-
CAN0 slot interrupt mask register	C0SIMKR	0000_{16}	Holding the value	√
CAN0 error interrupt mask register	C0EIMKR	- - - - -000 $_2$	Holding the value	√
CAN0 error interrupt status register	C0EISTR	- - - - -000 $_2$	Holding the value	-
CAN0 mask registers (global, local A/B)	C0GMRi C0LMARi C0LMBRi (i=0 - 4)	i=0 - - -0 0000_2 i=1 - -00 0000_2 i=2 - - - - 0000_2 i=3 0000 0000_2 i=4 - -00 0000_2	Holding the value	√
CAN0 message slot i control register	C0MCTLi (i=0 - 15)	00_{16}	Holding the value	√
CAN0 slot buffer select register	C0SBS	00_{16}	Holding the value	√
CAN0 control register 1	C0CTLR1	$XX00\ 00XX_2$	Holding the value	√
CAN0 sleep control register	C0SLPR	$XXXXXXX0_2$	Holding the value	√
CAN0 acceptance filter support register	C0AFS	0100_{16}	Holding the value	√

*1 -: The dash (-) denotes an undefined bit.

*2 0 = Cleared to 0, 1 = Set to 1, X = Holding the value, - = Undefined

*3 √ = Can be set, - = Cannot be set

4. Precaution about Sample Program in This Document

4.1. Symbol description of each register

Symbol of each register which is included in the sample program of this document complies with the description of C-language SFR header file for Renesas standard M32C/83 group.

4.2. Structure of Sample Program

Structure which is included in the sample program of this document is following configuration.

```
/* Definition of a standard data frame */
typedef struct{
    unsigned short id;
    unsigned char dlc;
    unsigned char data[8];
}can_std_data_def;

/* Definition of a standard remote frame */
typedef struct{
         unsigned short id;
         unsigned char dlc;
}can_std_remote_def;

/* Definition of an extend data frame */
typedef struct{
         unsigned long id;
         unsigned char dlc;
         unsigned char data[8];
}can_ext_data_def;

/* Definition of an extend remote frame */
typedef struct{
         unsigned long id;
         unsigned char dlc;
}can_ext_remote_def;
```

4.3. Infinite loop of "`while`"

In some part of the sample program an infinite loop is formed with "`while`", however, it is described in this way so that the description could be simplified. In actual programming, each while-loop must have a time limit. At over-time it should come out of the loop.

5. Reference

- M32C/83 group Data Sheet
- M32C/83 group Hardware Manual

When using this document, be sure to download the latest hardware manual from following Renesas technology home page.

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REVISION HISTORY	M32C/83 Group [CAN] CAN Configuration

Rev.	Date	Description	
		Page	Summary
1.00	July 24, 2003	-	First edition issued

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